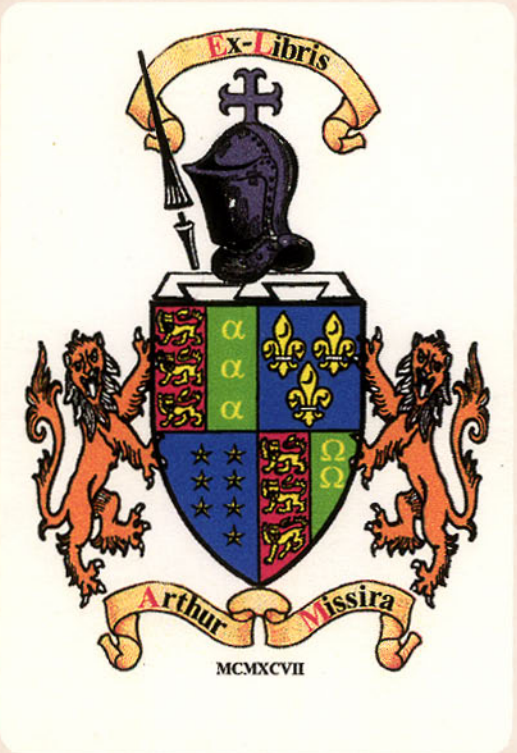
Raytheon LINEAR

Semiconductor
Division

Raytheon

Linear Integrated Circuits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Raytheon

Linear Integrated Circuits

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Industry
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Industry Part Number	Raytheon Direct Replacement	Raytheon Similar Replacement
AD101 AH	LM101 AT	
AD301 AH	LM301 AH	
AD451		RC4151
AD452		RC4152
AD453		RC4153
AD504 J		OP-05
AD504 K	OP-05 C	OP-05
AD504 L	OP-05 A	OP-05
AD504 M		OP-05
AD504 S	OP-05 E	
AD510 J		OP-07
AD510 JH	OP-05 E	
AD510 K		OP-07
AD510 KH	OP-05 A	
AD510 L		OP-07
AD510 LH	OP-05	
AD510 S		OP-07
AD510 SH	OP-05 C	
AD517 JH		OP-07 DT
AD517 KH		OP-07 CT
AD517 LH		OP-07 ET
AD517 SH		OP-07 AT
AD537		RC4153
AD539		RC4200/A
AD565 JD/BIN	DAC-4565 DDC, DAC-4565 JDC	
AD565 SD/BIN	DAC-4565 SDC	
AD580		REF-03 TM, REF-03 TC, REF-03 CTC, REF-03 CNB
AD581		REF-01, REF-01 A, REF-01 C, REF-01 D, REF-01 E, REF-01 H
AD584 J		
AD584 K		

Industry Part Number	Raytheon Direct Replacement	Raytheon Similar Replacement
AD584 L		
AD584 S		
AD584 T		
AD741	RC741	
AD741 C	RC741	
AD741 J		RC741
AD741 K		RC741
AD741 L		RC741
AD741 S	RC741 S	
AD1408-7 D	DAC-08 CDC	
AD1408-8 D	DAC-08 EDC	
AD1508-9 D	DAC-08 DM, DAC-08 ADM	
AD6012 ADC	DAC-6012 ADC	
AD6012 ADM	DAC-6012 ADM	
AD6012 DC	DAC-6012 DC	
AD6012 DM	DAC-6012 DM	
AD7520		DAC-10
AD7530		DAC-10
AD7533		DAC-10
AD9685/AD9687		RC4805
ADDAC-08	DAC-08 D	
ADDAC-08 AD	DAC-08 AD	
ADDAC-08 C	DAC-08 CD	
ADDAC-08 E	DAC-08 ED	
ADDAC-08 H	DAC-08 HD	
ADDAC-6012	DAC-6012	
ADDAC-6012 A	DAC-6012 A	
ADOP-07 AH	OP-07 A, OP-07 AT	
ADOP-07 CH	OP-07 C, OP-07 CT	
ADOP-07 CN	OP-07 CNB	
ADOP-07 DH	OP-07 D, OP-07 DT	
ADOP-07 DN	OP-07 DNB	
ADOP-07 EH	OP-07 E, OP-07 ET	
ADOP-07 EN	OP-07 ENB	

Industry Part Number	Raytheon Direct Replacement	Raytheon Similar Replacement
ADOP-07 H	OP-07, OP-07 T	
AM685	RC4805	
AM686	RC4805	
AM6012 ADC	DAC-6012 ADC	
AM6012 ADM	DAC-6012 ADM	
AM6012 DC	DAC-6012 DC	
AM6012 DM	DAC-6012 DM	
AMDAC-08 AQ	DAC-08 ADM	
AMDAC-08 CN	DAC-08 CDB	
AMDAC-08 CQ	DAC-08 CDC	
AMDAC-08 EN	DAC-08 EDB	
AMDAC-08 EQ	DAC-08 EDC	
AMDAC-08 Q	DAC-08 DM	
CA101 A	LM101 A	
CA111	LM111	
CA124	LM124, LM124 DC	
CA139	LM139 DC	
CA301	LM301	
CA301 A	LM301 A	
CA311	LM311	
CA324	LM324	
CA339	LM339	
CA358	LM358	
CA555	RC555	
CA723	RC723	
CA741	RC741	
CA747	RC747	
CA1458	RC1458	
CA1558	RC1558	
CA3302	RC3302	
CA3401	RC3401	
CMP-05	RC4805	
DAC-HF-10 BMC		DAC-10 FDC, DAC-10 GDC
DAC-HF-10 BMM		DAC-10, BDM, DAC-10 CDM
DAC-HF-12 BBM		DAC-6012 ADM, DAC-6012 DM
DAC-HF-12 BMC		DAC-6012 ADC, DAC-6012 DC
DAC-ICC10 BC	DAC-10 FDC	

Industry Part Number	Raytheon Direct Replacement	Raytheon Similar Replacement
DAC-IC8 BC		DAC-08 ADM, DAC-08 DM
DAC-IC8 UP		DAC-08 EDC, DAC-08 CDC, DAC-08 EDB DAC-08 CDB
DAC-08 AQ	DAC-08 ADM	
DAC-08 CN	DAC-08 CDB	
DAC-08 CP	DAC-08 CDB	
DAC-08 CQ	DAC-08 CDC	
DAC-08 EN	DAC-08 EDB	
DAC-08 EP	DAC-08 EDB	
DAC-08 EQ	DAC-08 EDC	
DAC-08 HN	DAC-08 HDB	
DAC-08 HP	DAC-08 HDB	
DAC-08 HQ	DAC-08 HDC	
DAC-08 Q	DAC-08 DC, DAC-08 DM	
DAC-10 B	DAC-10 BDC	
DAC-10 BX	DAC-10 BDM	
DAC-10 C	DAC-10 CDC	
DAC-10 CX	DAC-10 CDM	
DAC-10 F	DAC-10 FDC	
DAC-10 FX	DAC-10 FDC	
DAC-10 G	DAC-10 GDC	
DAC-10 GX	DAC-10 GDC	
DAC-312 BR		DAC-6012 DR
DAC-312 EP	DAC-6012 ADC	
DAC-312 ER	DAC-6012 ADC	
DAC-312 FR		DAC-6012 DC
DAC-0800 LCJ	DAC-08 EDC	
DAC-0800 LCN	DAC-08 EDB	
DAC-0800 LD	DAC-08 DC	
DAC-0801 LCJ	DAC-08 CDC	
DAC-0801 LCN	DAC-08 CDB	
DAC-0802 LCJ	DAC-08 HDC	
DAC-0802 LCN	DAC-08 HDC	
DAC-1020 LCN		DAC-10 FDC
DAC-1020 LD		DAC-10 BDM
DAC-1021/22 LCN		DAC-10 GDC
DAC-1021/22 LD		DAC-10 CDM

Industry Part Number	Raytheon Direct Replacement	Raytheon Similar Replacement
DAC-1208 AD-1		DAC-4565 DDC
DAC-1220 LCN		DAC-6012 ADC
DAC-1220 LD		DAC-6012 ADM
DAC-1221/22 LCN		DAC-6012 DC
DAC-1221/22 LD		DAC-6012 DM
DAC-1280 HDC-1		DAC-4565 JDC, DAC-4565 SDC
HA1-4741-2	HA1-4741-2	
HA1-4741-5	HA1-4741-5	
HA1-4741-8	HA1-4741-8	
HA3-4741-5	HA3-4741-5	
LH0044		OP-07C
LH0044 A		OP-07
LH0044 AC		OP-07 A
LH0044 B		OP-07 D
LH0044 C		OP-07 E
LH0070-0		REF-01
LH0070-1		REF-01 A
LH0070-2		REF-01 C
LH2101 A	LH2101 A	
LH2101 J	LH2101 DC	
LH2111	LH2111	
LH2111 J	LH2111 J	
LH2201 J	LH2201 DC	
LH2211 J	LH2211 J	
LH2301 J	LH2301 DC	
LH2311 J	LH2311 J	
LM101 A	LM101 A, LM111 ADE, LM101 AH	
LM111	LM111 DE, LM111 H, LM111	
LM124	LM124	
LM124 J	LM124 J	
LM136-5.0		REF-02
LM136A-5.0		REF-02A
LM139	LM139	
LM139 J	LM139 J	
LM148	LM148 J, LM148	
LM158-2.5		REF-03 TM
LM258-2.5		REF-03 TC

Industry Part Number	Raytheon Direct Replacement	Raytheon Similar Replacement
LM301	LM301 AN, LM301 ADE, LM301 AH	
LM301 A	LM301 A	
LM311	LM311, LM311 N LM311 DE, LM311 H	
LM324	LM324	
LM325/326		RC4195 NB, RC4195 DE, RC4195 T
LM336-5.0		REF-02 C, REF-02 D
LM336A-5.0		REF-02 E
LM339	LM339, LM339 N	
LM339 J	LM339 J	
LM348	LM348	RC4156, RC4157
LM358	LM358 N	
LM358-2.5		REF-03 CNB
LM358B-2.5		REF-03 CTC
LM360		RC4805
LM393	LM393 N	
LM555	RC555	
LM556	RC556	
LM723	RC723, RC723 DE RC723 N	
LM725	RC725	
LM741	RC741	
LM747	RC747, RC747 S	
LM2900	LM2900	
LM2901	LM2901	
LM2902	LM2902	
LM3301	RC3301	
LM3302	RC3302	
LM3401	RC3401	
LM3900	LM3900	
MC1404 AU5		REF-02 H
MC1404 AU10		REF-01 H
MC1404 U5	REF-02 CDE	REF-02 C, REF-02 D
MC1404 U10	REF-01 CDE, REF-01 DDE	REF-01 C, REF-01 D
MC1408 L6	DAC-08 CDC	
MC1408 L8	DAC-08 ADM	

Industry Part Number	Raytheon Direct Replacement	Raytheon Similar Replacement
MC1408 P6	DAC-08 CDB	
MC1455	RC555	
MC1456		RC4131
MC1458	RC1458	
MC1468		RC4195 NB, RC4195 DE, RC4195 T
MC1494		RC4200/A
MC1500 AG-5	REF-02 AT	
MC1500 AG-10	REF-01 AT	
MC1500 AU2		REF-03 TM
MC1500 U2		REF-02 TC
MC1504 AU5		REF-02
MC1504 AU10		REF-01
MC1555	RC555	
MC1568		RC4195 NB, RC4195 DE, RC4195 T
MC1723 CG	RC723 T	
MC1723 CL	RC723 DC	
MC1741	RC741	
MC1741 CG	RC741 T	
MC1741 CP1	RC741 DN	
MC1747	RC747	
MC1747 CG	RC747 T	
MC1747 CL	RC747 D	
MC3301	RC3301	
MC3302	RC3302	
MC3401	RC3401	
MC3403	RC3403 A	
MC3412	DAC-4565	
MC3412 L	DAC-4565 DDC, DAC-4565 JDC	
MC3416		RC4444
MC3416 L	RC4444 R	
MC3556	RC556	
MC4558	RC4558	RC4559
MC4558 CP1	RC4558 NB	
MC4741	RC4156	RC4157
MC1-4741-2	HA1-4741-2	
MC3-4741-5	HA3-4741-5	

Industry Part Number	Raytheon Direct Replacement	Raytheon Similar Replacement
MP-5501	REF-01	
MP-5501 A	REF-01 A	
MP-5501 C	REF-01 C	
MP-5501 D	REF-01 D	
MP-5501 E	REF-01 E	
MP-5501 H	REF-01 H	
MP-5502	REF-02	
MP-5502 A	REF-02 A	
MP-5502 C	REF-02 C	
MP-5502 D	REF-02 D	
MP-5502 E	REF-02 E	
MP-5502 H	REF-02 H	
MP-5505	OP-05	
MP-5505 A	OP-05 A	
MP-5505 C	OP-05 C	
MP-5505 E	OP-05 E	
MP-5507 A	OP-07 A	
MP-5507 B	OP-07	
MP-5507 C	OP-07 C	
MP-5507 D	OP-07 D	
MP-5507 E	OP-07 E	
MP-5527	OP-27	
MP-5527 A	OP-27 A	
MP-5527 B	OP-27 B	
MP-5527 C	OP-27 C	
MP-5527 E	OP-27 E	
MP-5527 F	OP-27 F	
MP-5527 G	OP-27 G	
MP-5537 A	OP-37 A	
MP-5537 B	OP-37 B	
MP-5537 C	OP-37 C	
MP-5537 E	OP-37 E	
MP-5537 F	OP-37 F	
MP-5537 G	OP-37 G	
MP-7520/30/33		DAC-10 BDM, DAC-10 CDM, DAC-10 FDC, DAC-10 GDC
MP-7523		DAC-08 ADM, DAC-08 DM, DAC-08 EDC, DAC-08 CDC

Industry Part Number	Raytheon Direct Replacement	Raytheon Similar Replacement
MP-7531/41		DAC-6012 ADM, DAC-6012 DM, DAC-6012 ADC, DAC-6012 DC
NE555	RC555	
NE556	RC556	
NE5532	RC5532	
NE5532 A	RC5532 A	
NE5534	RC5534	
NE5534 A	RC5534 A	
OP-02	RC741	
OP-04	RC747, RC747 S	
OP-05	OP-05	
OP-05 A	OP-05 A	
OP-05 C	OP-05 C	
OP-05 E	OP-05 E	
OP-06	RC725	
OP-07	OP-07	
OP-07 A	OP-07 A	
OP-07 C	OP-07 C	
OP-07 D	OP-07 D	
OP-07 E	OP-07 E	
OP-09	RC4136	
OP-14	RC1458	
OP-27	OP-27	
OP-27 A	OP-27 A	
OP-27 B	OP-27 B	
OP-27 C	OP-27 C	
OP-27 E	OP-27 E	
OP-27 F	OP-27 F	
OP-27 G	OP-27 G	
OP-37 A	OP-37 A	
OP-37 B	OP-37 B	
OP-37 C	OP-37 C	
OP-37 E	OP-37 E	
OP-37 F	OP-37 F	
OP-37 G	OP-37 G	
PM139	LM139	
PM339	LM339	
RC4136	RC4136	
RC4193 CJG	RC4193 DE	

Industry Part Number	Raytheon Direct Replacement	Raytheon Similar Replacement
RC4193 CP	RC4193 NB	
RC4558	RC4558	
RC4559	RC4559	
REF-01	REF-01	
REF-01 A	REF-01 A	
REF-01 C	REF-01 C	
REF-01 D	REF-01 D	
REF-01 E	REF-01 E	
REF-01 H	REF-01 H	
REF-02	REF-02	
REF-02 A	REF-02 A	
REF-02 C	REF-02 C	
REF-02 D	REF-02 D	
REF-02 E	REF-02 E	
REF-02 H	REF-02 H	
μA101 A	LM101A	
μA111	LM111	
μA124	LM124	
μA139	LM139	
μA148	LM148	RC4156, RC4157
μA301A	LM301A	
μA311	LM311	
μA324	LM324	
μA339	LM339	
μA348	LM348	
μA555	RC555	
μA556	RC556	
μA565 JDC	DAC-4565 JDC	
μA565 JJC	DAC-4565 DDC	
μA565 SDC	DAC-4565 SDC	
μA714 EHC	RC714 EH	
μA714 HC	RC714 CH	
μA714 HM	RC714 H	
μA714 LHC	RC714 LH	
μA723	RC723 DE, RC723 N	
μA725	RC725	
μA739		RC4739
μA741	RC741	
μA747	RC747, RC747 S	
μA760		RC4805

Industry Part Number	Raytheon Direct Replacement	Raytheon Similar Replacement
μA0801 CDC	DAC-08 CDC	
μA0801 CPC	DAC-08 CDB	
μA0801 DM	DAC-08 DM	
μA0801 EDC	DAC-08 EDC	
μA0801 EPC	DAC-08 EDB	
μA1458	RC1458	
μA2900	LM2900	
μA2901	LM2901	
μA2902	LM2902	
μA3301	LM3301	
μA3302	LM3302	
μA3401	RC3401	
μA3403	RC3403 A	
μA3900	LM3900	
μA4136	RC4136	
μA4558	RC4558	RC4559
μ301 A	LM301 A	
μ747	RC747 S	
VFC-32 KF		RC4151
VFC-42 BP		RC4152
VFC-52 BP		RC4153
VFQ-1C		RC4151
VFQ-2C		RC4152
VFQ-3C		RC4153
XR2207	XR2207	
XR2211	XR2211	
XR4151	RC4151	RC4152
XR4194 CN	RC4194 DC	
XR4195 CP	RC4195 NB	
4202 K		RC4200/A
4205 K		
4780		RC4151
4781		RC4152
4782		RC4153

Section 4
Product Selection Guide

Standard Linear Products

Raytheon	PMI	FSC	AMD	Motorola	National	RCA	Signetics	T.I.
HA1-4741-2				MC1-4741-2				
HA3-4741-5				MC3-4741-5				
LH2101A			LH2101A		LH2101A		LH2101A	
LH2111			LH211		LH2111			
LM101A		μA101A	LM101A	LM101A	LM101A	CA101A	LM101A	
LM111		μA111	LM111	LM111	LM111	CA111	LM111	
LM124		μA124	LM124	LM124	LM124	CA124	LM124	LM124
LM139	PM139	μA139	LM139	LM139	LM139	CA139	LM139	LM139
LM148		μA148	LM148		LM148		LM148	
LM301A		μ301A	LM301A	LM301A	LM301A	CA301A	LM301A	LM301A
LM311		μA311	LM311	LM311	LM311	CA311	LM311	
LM324		μA324	LM324	LM324	LM324	CA324	LM324	LM324
LM339	PM339	μA339	LM339	LM339	LM339	CA339	LM339	LM339
LM348		μA348	LM348		LM348		LM348	LM348
LM2900		μA2900			LM2900			
LM2901		μA2901		LM2901	LM2901		LM2901	LM2901
LM2902		μA2902		LM2902	LM2902			LM2902
LM3900		μA3900			LM3900			LM3900
RC1458	OP-14	μA1458		MC1458	LM1458	CA1458	MC1458	MC1458
RC3301		μA3301		MC3301	LM3301			
RC3302		μA3302		MC3302	LM3302	CA3302	MC3302	
RC3401		μA3401		MC3401	LM3401	CA3401		
RC3403A		μA3403		MC3403				MC3403
RC4131				MC1456*				
RC4136	OP-09	μA4136						RC4136
RC4156		μA148*		MC4741	LM348*			LM348*
RC4157		μA148/ 348*		MC4741*	LM348*			LM348*
RC4558		μA4558		MC4558				RC4558
RC4559		μA4558*		MC4558*				RC4559
RC4739		μA739*						
RC5532							NE5532	NE5532
RC5532A							NE5532A	NE5532A
RC5534							NE5534	NE5534
RC5534A							NE5534A	NE5534A
RC555		μA555		MC1555	LM555		NB565	NE555
RC556		μA556		MC3556	LM556		NE556	NE556
RC725	OP-06	μA725			LM725			
RC741	OP-02	μA741		MC1741	LM741	CA741	CA741	μA741
RC747	OP-04	μA747		MC1747	LM747	CA747	CA747	
RC747S	OP-04	μA747			LM747			μ747

*Functional Equivalent

Data Conversion Products

Raytheon	PMI	FSC	AMD	Motorola	NSC	Analog Devices	Micro-Power	Datel
DAC-08ADM	DAC-08AQ		AMDAC-08AQ	MC1408L8	DAC-08AQ	AD-1508-9D	MP-7523*	DAC-IC8BC*
DAC-08DM	DAC-08Q	μA0801DM	AMDAC-08Q		DAC-08Q	AD-1508-9D	MP-7523*	DAC-IC8BC*
DAC-08EDC	DAC-08EQ	μA0801EDC	AMDAC-08EQ		DAC-08EQ	AD-1408-8D	MP-7523*	DAC-IC8UP*
DAC08CDC	DAC-08CQ	μA0801CDC	AMDAC-08CQ	MC1408L6	DAC-08CQ	AD-1408-7D	MP-7523*	DAC-IC8UP*
DAC-08EDB	DAC-08EP	μA0801EPC	AMDAC-08EN		DAC-08EP			DAC-IC8UP*
DAC-08CDB	DAC-08CP	μA0801CPC	AMDAC-08CN	MC1408P6	DAC-08CP			DAC-IC8UP*
DAC-10BDM	DAC-10BX				DAC-1020 LD*	AD7520/ 30/33*	MP-7520/ 30/33*	DAC-HF10BMM*
DAC10CDM	DAC-10CX				DAC-1021/ 22LD*	AD7520/ 30/33*	MP-7520/ 30/33*	DAC-HF10BMM*
DAC-10FDC	DAC-10FX				DAC-1020 LCN*	AD7520/ 30/33*	MP-7520 30/33*	DAC-HF10BMC*
DAC-10GDC	DAC-10GX				DAC-1021/ 22LCN*	AD7520/ 30/33*	MP-7520/ 30/33*	DAC-HF10BMC*
DAC-6012ADM			AM6012ADM		DAC-1220LD*	AD6012ADM	MP-7531/ 41*	DAC-HF12BMM*
DAC-6012DM	DAC-312BR*		AM6012DM		DAC-1221/ 22LD*	AD6012DM	MP-7531/ 41*	DAC-HF12BMM*
DAC-6012ADC			AM6012ADC		DAC-1220LCN*	AD6012ADC	MP-7531/ 41*	DAC-HF12BMC*
DAC-6012DC	DAC-312FR*		AM6012DC		DAC-1221/ 22LCN*	AD6012DC	MP-7531/ 41*	DAC-HF12BMC*
DAC-4565DDC		μA565JJC		MC3412L	DAC1208AD-I*	AD565JD/BIN		
DAC-4565JDC		μA565JDC		MC3412L	DAC1280 HCD-I*	AD565JD/BIN		
DAC-4565SDC		μA565SDC			DAC1280 HCD-I*	AD565SD/BIN		

*Functional Equivalent

Other LIC Devices

Raytheon	Teledyne	Analog Devices	EXAR	Motorola	Datel	Burr Brown
RC4151	4780*	AD451*	XR4151		VFQ-1C*	VFC-32KF*
RC4152	4781*	AD452*	XR4151*		VFQ-2C*	VFC-42BP*
RC4153	4782*	AD537*			VFQ-3C*	VFC-52BP*
RC4200/A		AD539*		MC1494*		4202K* & 4205K*
XR2207			XR2207			
XR2211			XR2211			
RC4444				MC3416		

*Functional Equivalent

High Performance Linear Products

Op Amps, Voltage Reference and Voltage Regulators

Raytheon	PMI	FSC	Micro-Power	Analog Devices	Motorola	NSC
RC714H		μA714HM				
RC714EH		μA714EHC				
RC714CH		μA714HC				
RC714LH		μA714LHC				
OP-05	OP-05		MP-5505	AD510LH/AD504M		
OP-05A	OP-05A		MP-5505A	AD510KH/AD504L		
OP-05C	OP-05C		MP-5505C	AD510SH/AD504K		
OP-05E	OP-05E		MP-5505E	AD510JH/AD504S		
OP-07	OP-07		MP-5507B	ADOP-07H		LH0044A*
OP-07A	OP-07A		MP-5507A	ADOP-07AH		LH0044AC*
OP-07C	OP-07C		MP-5507C	ADOP-07CH		LH0044*
OP-07D	OP-07D		MP-5507D	ADOP-07DH		LH0044B*
OP-07E	OP-07E		MP-5507E	ADOP-07EH		LH0044C*
OP-27	OP-27		MP-5527		OP-27	
OP-27A	OP-27A		MP-5527A		OP-27A	
OP-27B	OP-27B		MP-5527B		OP-27B	
OP-27C	OP-27C		MP-5527C		OP-27C	
OP-27E	OP-27E		MP-5527E		OP-27E	
OP-27F	OP-27F		MP-5527F		OP-27F	
OP-27G	OP-27G		MP-5527G		OP-27G	
OP-37A	OP-37A		MP-5537A		OP-37A	
OP-37B	OP-37B		MP-5537B		OP-37B	
OP-37C	OP-37C		MP-5537C		OP-37C	
OP-37E	OP-37E		MP-5537E		OP-37E	
OP-37F	OP-37F		MP-5537F		OP-37F	
OP-37G	OP-37G		MP-5537G		OP-37G	
RC4805	CMP-05	μA760*		AD9685/AD9687*		LM360*
REF-01	REF-01		MP-5501	AD581*	MC1504AU10*	LH0070-0*
REF-01A	REF-01A		MP-5501A	A0581*		LH0070-1*
REF-01C	REF-01C		MP-5501C	A0581*	MC1404U10*	LH0070-2*
REF-01D	REF-01D		MP-5501D	A0581*	MC1404U10*	
REF-01E	REF-01E		MP-5501E	AD581*		
REF-01H	REF-01H		MP-5501H	AD581*	MC1404AU10*	
REF-02	REF-02		MP-5502		MC1504AU5*	LM136-5.0*
REF-02A	REF-02A		MP-5502A			LM136A-5.0*
REF-02C	REF-02C		MP-5502C		MC1404U5*	LM336-5.0*
REF-02D	REF-02D		MP-5502D		MC1404U5*	LM336-5.0*
REF-02E	REF-02E		MP-5502E			LM336A-5.0*
REF-02H	REF-02H		MP-5502H		MC1404AU5*	

*Functional Equivalent

High Performance Linear Products

Op Amps, Voltage Reference and Voltage Regulators

Raytheon	Exar	FSC	T.I.	Analog Devices	Motorola	NSC
REF-03T				AD580*	MC1500AU2*	LM158-2.5*
REF-03T				AD580*	MC1500U2*	LM258-2.5*
REF-03CT				AD580*	MC1400AU2*	LM358B-2.5*
REF-03CNB				AD580*	MC1400U2*	LM358-2.5*
RC4193NB			RC4193CP			
RC4193DE			RC4193CJG			
RC4391NB						
RC4391DE						
RC4194DB						
RC4194DC	XR4194CN					
RC4194TK						
RC4195NB	XR4195CP				MC1468/ MC1568*	LM325/326*
RC4195DE					MC1468/ MC1568*	LM325/326*
RC4195T					MC1468/ MC1568*	LM325/326*
RC723DE		μA723				LM723
RC723N		μA723				LM723

*Functional Equivalent

Package Cross-Reference for High Performance

Package	Raytheon	PMI	Analog Devices
TO-99	"T"	"J"	"H"
Plastic Mini DIP	"NB"	"P"	"N"
8-Pin Ceramic DIP	"DE"	"Z"	"D"

High Performance Operational Amplifiers

Device	Description	Maximum Input Specifications			Typical Input Noise Specifications					Typ. Unity Gain BW (MHz)	Max. Sply Volt. (±V)	Pins	Temp. Range
		Offset Volt. (mV)	Offset Cur. (nA)	Bias Cur. (nA)	1kHz Volt. Density $\left[\frac{nV}{\sqrt{Hz}}\right]$	Low Freq. Corner e_N (Hz)	1kHz Cur. Density $\left[\frac{pA}{\sqrt{Hz}}\right]$	Low Freq. Corner i_N (Hz)	Typ. Slew Rate (V/μS)				
OP-05	Single Inst. Op Amp	0.50	2.8	±3	10	10	0.14	50	0.17	0.6	22	8	M
OP-05A	Single Inst. Op Amp	0.15	2.0	±2	10	10	0.14	50	0.17	0.6	22	8	M
OP-05C	Single Inst. Op Amp	1.3	6.0	±7	10	10	0.14	50	0.17	0.6	22	8	C
OP-05E	Single Inst. Op Amp	0.50	3.8	±4	10	10	0.14	50	0.15	0.6	22	8	C
OP-07	Single Ultra Low Offset Voltage	0.075	2.8	±3	10	10	0.14	50	0.17	0.6	22	8	M
OP-07A	Single Ultra Low Offset Voltage	0.025	2.0	±2	10	10	0.14	50	0.17	0.6	22	8	M
OP-07C	Single Ultra Low Offset Voltage	0.150	6.0	±7	10.5	10	0.15	50	0.17	0.6	22	8	C
OP-07D	Single Ultra Low Offset Voltage	0.150	6.0	±12	10.5	10	0.15	50	0.17	0.6	22	8	C
OP-07E	Single Ultra Low Offset Voltage	0.075	3.8	±4	10.3	10	0.14	50	0.17	0.6	22	8	C
OP-27A	Single Ultra Low Noise	0.025	35	±40	3.0	2.7	0.4	140	2.8	8.0	22	8	M, C
OP-27B	Single Ultra Low Noise	0.060	50	±55	3.0	2.7	0.4	140	2.8	8.0	22	8	M, C
OP-27C	Single Ultra Low Noise	0.100	75	±80	3.2	2.7	0.4	140	2.8	8.0	22	8	M, C
OP-27E	Single Ultra Low Noise	0.025	35	±40	3.0	2.7	0.4	140	2.8	8.0	22	8	M, C
OP-27F	Single Ultra Low Noise	0.060	50	±55	3.0	2.7	0.4	140	2.8	8.0	22	8	M, C
OP-27G	Single Ultra Low Noise	0.100	75	±80	3.2	2.7	0.4	140	2.8	8.0	22	8	M, C
OP-37A	Single High Slew Rate Low Noise	0.025	35	±40	3.0	2.7	0.4	140	17	63	22	8	M, C
OP-37B	Single High Slew Rate Low Noise	0.060	50	±55	3.0	2.7	0.4	140	17	63	22	8	M, C
OP-37C	Single High Slew Rate Low Noise	0.100	75	±80	3.2	2.7	0.4	140	17	63	22	8	M, C
OP-37E	Single High Slew Rate Low Noise	0.025	35	±40	3.0	2.7	0.4	140	17	63	22	8	M, C
OP-37F	Single High Slew Rate Low Noise	0.060	50	±55	3.0	2.7	0.4	140	17	63	22	8	M, C
OP-37G	Single High Slew Rate Low Noise	0.100	75	±80	3.2	2.7	0.4	140	17	63	22	8	M, C
OP-47B*	Low Noise, High Slew Op Amp	0.06	50	±55	3.0	2.7	0.4	140	50	70	22	8	M
OP-47F*	Low Noise, High Slew Op Amp	0.06	50	±55	3.0	2.7	0.4	140	50	70	22	8	C
OP-47G*	Low Noise, High Slew Op Amp	0.10	75	±80	3.2	2.7	0.4	140	50	70	22	8	C
RC714	Single Precision	0.075	2.8	±3	9.6	10	0.12	140	0.17	0.5	22	8	C
RC714C	Single Precision	0.150	6.0	±7	9.8	10	0.13	140	0.17	0.5	22	8	C
RC714E	Single Precision	0.075	3.8	±4	9.6	10	0.12	140	0.17	0.5	22	8	C
RC714L	Single Precision	0.250	20	±30	9.8	10	0.13	140	0.17	0.5	22	8	C
RC3078	Single Micropower	4.5	32	170	19	100	1.0	200	0.04	0.1	7	8	M, C
RC3078A	Single Micropower	3.5	2.5	12	36	100	0.4	200	0.04	0.1	18	8	M, C
RM5534	Single High Performance Low Noise	2.0	200	800	4.0	100	0.6	200	13	10	22	8	M, C
RM5534A	Single High Performance Low Noise	2.0	200	800	3.5	100	0.4	200	13	10	22	8	M, C

Notes: ( ) Denotes guaranteed specifications
M = Military -55°C to 125°C
C = Commercial 0°C to 70°C
* = Preliminary specifications

Voltage References

Device	Nominal Voltage Out	Typical Tempco (ppm/°C)	Temp. Range	Typical ΔV_{OUT} Over Temp. (%)	Typical Line Reg. (%/Volt)	Typical Load Reg. (%/mA)	Typical Load Current (mA)	Input Voltage Range (Voltage)
REF-01A	10.00	3.0	Mil	.06	.006	.005	21	12 to 40
REF-01	10.00	10.0	Mil	.18	.006	.006	21	12 to 40
REF-01C	10.00	20.0	Comm	.14	.009	.006	21	12 to 40
REF-01D	10.00	70.0	Comm	.49	.012	.009	21	12 to 40
REF-01E	10.00	3.0	Comm	.02	.006	.005	21	12 to 40
REF-01H	10.00	10.0	Comm	.07	.006	.006	21	12 to 40
REF-02A	5.00	3.0	Mil	.06	.006	.005	21	7 to 40
REF-02	5.00	10.0	Mil	.18	.006	.006	21	7 to 40
REF-02C	5.00	20.0	Comm	.14	.009	.006	21	7 to 40
REF-02D	5.00	70.0	Comm	.49	.012	.009	21	7 to 40
REF-02E	5.00	3.0	Comm	.02	.006	.005	21	7 to 40
REF-02H	5.00	10.0	Comm	.07	.006	.006	21	7 to 40
REF-03	2.50	10.0	Mil	.7	.001	.010	20	4.5 to 30
REF-03C	2.50	10.0	Comm	.7	.001	.010	20	4.5 to 30
REF-03D	2.50	20.0	Comm	.7	.001	.020	20	4.5 to 30

High Performance Dual & Quad Operational Amplifiers

Device	Description	Maximum Input Specifications			Typical Input Noise Specifications				Typ. Slew Rate ($V/\mu S$)	Typ. Unity Gain BW (MHz)	Max. Sply Volt. (±V)	Pins	Temp. Range
		Offset Volt. (mV)	Offset Cur. (nA)	Bias Cur. (nA)	1kHz Volt. Density $\left[\frac{nV}{\sqrt{Hz}}\right]$	Low Freq. Corner e_N (Hz)	1kHz Cur. Density $\left[\frac{pA}{\sqrt{Hz}}\right]$	Low Freq. Corner i_N (Hz)					
RC2041	Dual High Performance Low Noise	3.0	200	500	5.0	20	0.4	200	3.0	7(4.0)	18	8	C
RC2043	Dual High Performance Low Noise	3.0	200	100	5.0	20	0.4	200	6.0	14(8.0)	18	8	C
RC4560	Dual High Performance	6.0	200	500	10	20	0.5	200	4.0	10(7.0)	18	8	C
RC4562	Dual High Performance	6.0	200	500	6.0	20	0.2	200	7.0	15(8.0)	18	8	C
RC4558	Dual High Gain	6.0	200	500	10	20	0.5	200	1.0	2.5	18	8	M, C
RC4559	Dual High Performance	6.0	100	250	10	20	0.18	200	2(1.5)	4(3.0)	18	8	M, C
RC4739	Dual Low Noise	6.0	200	500	10	20	0.5	400	1.0	4.0	18	14	M, C
RC5532	Dual High Performance Low Noise	4.0	150	800	5.0	100	0.7	200	8.0	10	22	8	M, C
RC5532A	Dual High Performance Low Noise	4.0	150	800	5.0	100	0.7	200	8.0	10	22	8	M, C
RC4556	Dual High Performance	6.0	200	500	10	20	0.5	200	3.0	8(5.0)	18	8	C
RC4136	Quad 741 General	6.0	200	500	10	20	0.2	100	1.5	10	18	14	M, C
RC4156	Quad High Performance	5.0	50	300	9.0	100	0.1	200	1.6 (1.3)	3.5 (2.5)	20	14	M, C
RC4157	Quad High Speed Decompensated	5.0	50	300	9.0	—	0.1	—	8(6.5)	19(15)	20	14	M, C
HA4741-2	Quad General Purpose	3.0	30	200	9.0	80	0.1	250	1.6	3.5	20	14	M, C

Notes: ( ) Denotes guaranteed specifications
M = Military -55°C to 125°C
C = Commercial 0°C to 70°C

MIL-M-Qualified Devices

Ordering P/N M38510-	Raytheon Part Number	QPL Status
10101BCB	MM741DCB	I
10101BCC	MM741DCC	I
10101BGC	MM741TEC	I
10101BPC	MM741DEC	I
10102BAC	MM747CJC	I
10102BCB	MM747DCB	I
10102BCC	MM747DCC	I
10102BIC	MM747TFC	I
10103BCB	MM101ADCB	I
10103BCC	MM101ADCC	I
10103BGC	MM101ATEC	I
10103BPC	MM101ADEC	I
10105BEA	MM2101ADMA	I
10105BEB	MM2101ADMB	I
10105BEC	MM2101DMC	I
10304BCC	MM0111DFC	I
10304BEC	MM0111TEC	I
10304BPC	MM0111DEC	I

Ordering P/N M38510-	Raytheon Part Number	QPL Status
10305BEA	MM2111DMA	I
10305BEC	MM2111DMC	I
11001BCB	MM0148DCB	I
11001BCC	MM0148DCC	I
11003BCA	MM4156DCA	I
11003BCB	MM4156DCB	I
11003BCC	MM4156DCC	I
11004BCA	MM4136DCA	I
11004BCB	MM4136DCB	I
11004BCC	MM4136DCC	I
11201BCB	MM0139DCB	I
11201BCC	MM0139DCC	I
11301BEB	MMDAC-08DMB	I
11301BEC	MMDAC-08DMC	I
11302BEB	MMDAC-08ADMB	I
11302BEC	MMDAC-08ADMC	I

Single Operational Amplifiers

Type	Description	Maximum Input Specifications @ 25°C			Typ[1] Unity Gain BW (MHz)	Typ. Slew Rate (V/μS)	Temp[2] Range	Available Packages						
		Offset Voltage (mV)	Offset Current (nA)	Bias Current (nA)				DC	DE	H	M	N	NB	T
LM101A	General Purpose With Improved Input Characteristics	2.0	10	75	1.0	0.5	M		X	X				
LM301A	General Purpose With Improved Input Characteristics	7.5	50	250	1.0	0.5	C		X	X			X	
OP-05	Single Inst. Op Amp	0.5	2.8	±3.0	0.6	0.17	M		X					X
OP-05A	Single Inst. Op Amp	0.15	2.0	±2.0	0.6	0.17	M		X					X
OP-05C	Single Inst. Op Amp	1.3	6.0	±7.0	0.6	0.17	C		X	X				X
OP-05E	Single Inst. Op Amp	0.5	3.8	±4.0	0.6	0.17	C		X	X				X
OP-07	Ultra Low Offset Voltage	.075	2.8	±3.0	0.6	0.17	M, C		X					X
OP-07A	Ultra Low Offset Voltage	.025	2.0	±2.0	0.6	0.17	M, C		X					X
OP-07C	Ultra Low Offset Voltage	.150	6.0	±7.0	0.6	0.17	C		X	X			X	X
OP-07D	Ultra Low Offset Voltage	.150	6.0	±12	0.6	0.17	C		X	X			X	X
OP-07E	Ultra Low Offset Voltage	.075	3.8	±4.0	0.6	0.17	C		X	X			X	X
OP-27A	Ultra Low Noise	.025	35	±40	8.0	2.8	M, C		X					X
OP-27B	Ultra Low Noise	.060	50	±55	8.0	2.8	M, C		X					X
OP-27C	Ultra Low Noise	.100	75	±80	8.0	2.8	M, C		X					X
OP-27E	Ultra Low Noise	.025	35	±40	8.0	2.8	M, C		X	X				X
OP-27F	Ultra Low Noise	.060	50	±55	8.0	2.8	M, C		X	X				X
OP-27G	Ultra Low Noise	.100	75	±80	8.0	2.8	M, C		X	X				X
OP-37A	High Slew Rate, Low Noise	.025	35	±40	63	17	M, C		X					X
OP-37B	High Slew Rate, Low Noise	.060	50	±55	63	17	M, C		X					X
OP-37C	High Slew Rate, Low Noise	.100	75	±80	63	17	M, C		X					X
OP-37E	High Slew Rate, Low Noise	.025	35	±40	63	17	M, C		X	X				X
OP-37F	High Slew Rate, Low Noise	.060	50	±55	63	17	M, C		X	X				X
OP-37G	High Slew Rate, Low Noise	.100	75	±80	63	17	M, C		X	X				X
OP-47B[4]	Low Noise, High Slew Op Amp	.06	50	±55	70	50	M		X					X
OP-47F[4]	Low Noise, High Slew Op Amp	.06	50	±55	70	50	C		X	X				X
OP-47G[4]	Low Noise, High Slew Op Amp	0.1	75	±80	70	50	C		X	X				X

Notes: 1. Gain bandwidth product for 5534/A series and closed loop bandwidth for OP series.
2. Operating Temperature Range: M = -55°C to +125°C; C = 0°C to +70°C.
3. RM/RC5534A guarantees maximum input noise specification.
4. Preliminary specifications.

Single Operational Amplifiers (Continued)

Type	Description	Maximum Input Specifications @ 25°C			Typ[1] Unity Gain BW (MHz)	Typ. Slew Rate (V/μS)	Temp[2] Range	Available Packages						
		Offset Voltage (mV)	Offset Current (nA)	Bias Current (nA)				DC	DE	H	M	N	NB	T
RC714	Precision	0.075	2.8	±3.0	0.5	0.17	C		X	X				
RC714C	Precision	0.150	6.0	±7.0	0.5	0.17	C		X	X			X	
RC714E	Precision	0.075	3.8	±4.0	0.5	0.17	C		X	X				
RC714L	Precision	0.250	20	±30	0.5	0.17	C		X	X			X	
RC741	General Purpose, Internal Comp	6.0	200	500	1.0	0.5	C	X	X				X	X
RC3078	Programmable Micropower	4.5	32	170	0.1	0.04	C		X				X	X
RM3078A	Programmable Micropower	3.5	2.5	12	0.1	0.04	A		X					X
RC5534	High Performance, Low Noise	4.0	300	1500	10	13	C		X	X			X	
RM5534	High Performance, Low Noise	2.0	200	800	10	13	M		X					X
RC5534A[3]	High Performance, Low Noise	4.0	300	1500	10	13	C		X	X			X	
RM5534A[3]	High Performance, Low Noise	2.0	200	800	10	13	M		X					X

Notes: 1. Gain bandwidth product for 5534/A series and closed loop bandwidth for OP series.
2. Operating Temperature Range: M = -55°C to +125°C; C = 0°C to +70°C.
3. RM/RC5534A guarantees maximum input noise specification.
4. Preliminary specifications.

Dual Operational Amplifiers

Type	Description	Maximum Input Specifications @ 25°C			Typ[1] Unity Gain BW (MHz)	Typ. Slew Rate (V/μS)	Temp[2] Range	Available Packages							
		Offset Voltage (mV)	Offset Current (nA)	Bias Current (nA)				DB	DC	DE	J	M	NB	T	H
LH2101A	High Performance	2	10	75	—	10					X				
LH2301A	High Performance	7.5	50	250	—	10					X				
LM358	Single Supply	7	100	250	1	—	C					X	X		
RC747	Dual 741	6	200	500	1	0.5	C	X	X					X	
RM747	Dual 741	5	200	500	1	0.5	M		X					X	
RC1458	Dual 741	6	200	500	1	0.5	C			X			X		X
RM1558	Dual 741	5	200	500	1	0.5	M			X				X	
RC2041	High Performance, Low Noise	3	200	500	7(4)	3	C					X	X		
RC2043	High Performance, Low Noise	3	200	1000	14(8)	6	C					X	X		
RC4556	High Performance	6	200	500	8(5)	3	C					X	X		
RC4558	Wideband 741	6	200	500	3	1	C			X		X	X		X
RM4558	Wideband 741	5	200	500	3	1	M			X				X	
RC4559	High Performance	6	100	250	4(3)	2(1.5)	C			X		X	X		X
RM4559	High Performance	5	100	250	4(3)	2(1.5)	M			X				X	
RC4560	High Performance	6	200	500	10(7)	4	C					X	X		
RC4562	High Performance	6	200	500	15(8)	7	C					X	X		
RC4739	Low Noise, Wideband 741	6	200	500	3	1	C	X							
RC5532	High Performance, Low Noise	4	150	800	10	8	C			X			X		X
RM5532	High Performance, Low Noise	2	100	400	10	8	M			X				X	
RC5532A[3]	High Performance, Low Noise	4	150	800	10	8	C			X			X		X
RM5532A[3]	High Performance, Low Noise	2	100	400	10	8	M			X				X	

Notes: 1. Gain bandwidth product for 5532A series.
2. Operating Temperature Range: M = -55°C to +125°C; C = 0°C to +70°C.
3. RM/RC5532A guarantees maximum input noise specification.
( ) Denotes guaranteed specifications.

Quad Operational Amplifiers

Type	Description	Maximum Input Specifications @ 25°C			Typ[1] Unity Gain BW (MHz)	Typ. Slew Rate (V/μS)	Temp[1] Range	Available Packages[2]				
		Offset Voltage (mV)	Offset Current (nA)	Bias Current (nA)				DB	DC	J	M	N
HA4741-2	741 General Purpose	3	30	200	3.5	1.6	M		X			
HA4741-5	741 General Purpose	5	50	300	3.5	1.6	C	X	X			
LM124	Single Supply	5	±30	150	1	—	M			X		
LM148	Low Power 741	5	±25	100	1	0.5	M			X		
LM324	Single Supply	7	±50	250	1	—	C			X	X	X
LM348	Low Power 741	6	±50	200	1	0.5	C			X		X
LM3900	Current Mode, Single Supply	—	—	200	2.5	±.5/-20	C					X
RC3401	Current Mode, Single Supply	—	—	300	5	0.6	C	X				
RC3403A	Ground Sensing	6	50	500	1	1.2	C	X	X			
RM3503A	Ground Sensing	4	50	400	1	1.2	M		X			
RC4136	741 General Purpose	6	200	500	3	1	C	X	X			
RM4136	741 General Purpose	4	150	400	3	1.5	M		X			
RC4156	High Performance	5	50	300	3.5 (2.8)	1.6 (1.3)	C	X	X			
RM4156	High Performance	3	30	200	3.5 (2.8)	1.6 (1.3)	M		X			
RC4157	High Speed, Decompensated	5	50	300	19(15)	8(6.5)	C	X	X			
RM4157	High Speed, Decompensated	3	30	200	19(15)	8(6.5)	M		X			

Notes: 1. Operating Temperature Range: M = -55°C to +125°C; C = 0°C to +70°C
( ) Denotes guaranteed specification.

Comparators

Type	Description	Maximum Input Specifications @ 25°C: Offset Voltage (mV)	Bias Current (nA)	Offset Current (nA)	Voltage Gain (V/mV Typ)	Max. Sat. Voltage	Output Leakage Current (nA Typ)	Available Packages: DB	DC	DE	H	J	M	N	T
LH2111	Dual Precision Voltage	3.0	10	100	200	1.5V	0.2					X			
LH2311	Dual Precision Voltage	7.5	50	250	200	1.5V	0.2					X			
LM111	Low Input Current	3.0	10	100	200	1.5V	0.2			X	X				
LM139	Quad Single Supply	±5.0	100	±25	200	400mV	0.1					X			
LM311	Low Input Current	7.5	50	250	200	1.5V	0.2			X	X				
LM339	Quad Single Supply	±5.0	250	±50	200	400mV	0.1					X	X	X	
LM393	Dual Low Power	±5.0	250	±50	200	400mV	0.1						X	X	
LM2901	Quad Single Supply	±7.0	250	±50	100	400mV	0.1							X	
RC2403	Dual Low Power	±10	500	±100	200	400mV	0.1						X	X	
RC3302	Quad Single Supply	±20	500	±100	30	500mV	0.1	X	X						
RC4805	Precision High Speed	0.6	1800	20	15	0.40	—			X				X	X
RM4805	Precision High Speed	0.6	1800	150	20	0.40	—			X					X
RM4805A	Precision High Speed	0.25	1200	80	20	0.40	—			X					X
RC4805E	Precision High Speed	0.25	1200	80	20	0.40	—			X					X

*at I_{SINK} = 15mA

Timers

Type	Description	Supply Voltage (V max)	Supply Current (mA max)	Timing Error: Initial Accuracy (%)	Drift with Temp (ppm/°C)	Drift with Supply Volt. (%/Volt)	Trigger Voltage (V)	Trigger Current (μA Typ)	Available Packages: DB	DC	DE	M	NB	T
RC555	Single	16	6.0	1.0	50	0.1	1.67 typ	0.5			X	X	X	X
RM555	Single	18	5.0	0.50	100	0.05	1.9 max	0.5			X			X
RC556	Dual 555	16	6.0	2.25	150	0.3	5.0*	0.5	X	X				
RM556	Dual 555	18	5.0	1.5	90	0.15	5.0*	0.5		X				

*Typical for 15V supply

Section 5
Quality & Reliability

Quality and reliability of semiconductor components are finite characteristics subject to the same assessment and improvement as any other factors of performance. Quality is the measure of a device's conformance to its specifications, and reliability is the measure of the device's performance over time. The approach to maintaining and improving them must be systematic, because every phase of the manufacturing process has an impact on the final product.

Reliability Concepts

Reliability is a measure or evaluation of the life expectancy of a device, or to state it another way, the length of trouble-free performance that it can offer. There are various parameters of reliability, and these can be summarized by the well-known "bathtub curve" shown in Figure 1.

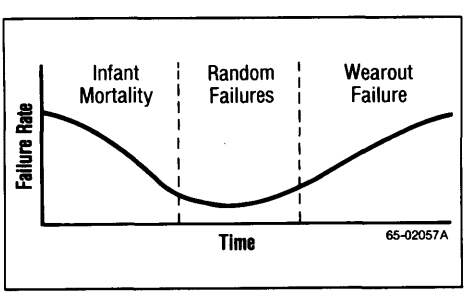


Figure 1. Failure vs. Time

As a device is manufactured, there are numerous random potential failure mechanisms built into the device. These potential failure mechanisms usually exhibit themselves under a relatively moderate stress level, and hence occur early in the life span of the device. This period is termed **Infant Mortality**. The period of early failures can be reduced through good manufacturing control and screening methods. The screening techniques detailed are typical of the types of stress tests to which a product lot is subjected in order to detect the failure modes and to eliminate the suspect devices from the production lot. The follow-up tables (see Tables 1, 2, 3 and 4) for sample tests of the production lot measures the effectiveness the production screening in reducing infant mortality failures.

The period of **Random Failure** mechanisms represents the time when an occasional random failure mechanism can cause a device to fail. This period usually represents a long time with a very low device failure rate and is the major time frame of customer interest. The **Wearout Failure** period is the final period where the device literally wears out due to physical phenomenon that existed at the time of manufacture.

The infant mortality and random failures periods can be described through a series of mathematical equations and probability calculations. The probability of having a failure at a specific point in time can be expressed by the equation:

$$P_o = e^{-xt}$$

where:

x = the failure rate (failures per unit time)
t = time

During the infant mortality period, "x" is changing very rapidly and does not become relatively stable under the random failure period. The failure rate "x" is usually expressed in % failures per 1000 hours and is sometimes expressed as a mean time between failures (MTBF) through the expression:

$$MTBF = \frac{1}{\text{Failure Rate}}$$

Since the data for the failure rate calculations is derived from a sample of devices out of a production lot, a confidence level number is usually stated for the failure rate. A 90% confidence level (CL) has become a common number. The confidence level is demonstrated by the distribution curve shown in Figure 2.

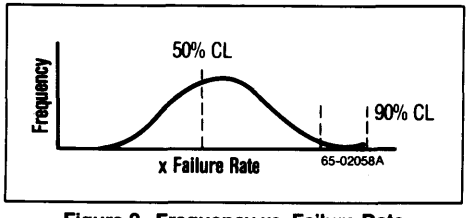


Figure 2. Frequency vs. Failure Rate

The failure rate "x" is calculated by using a Chi square (χ^2) distribution through the equation:

$$\chi = \frac{\chi^2(x, 2r+2)}{2nt}$$

where:

- x = 100-%CL/100
- r = number of rejects
- n = total number of devices
- t = time

The number of failures over a period of time (x) is a very critical factor in determining an accurate failure rate number. If only device failures at room or operating temperatures were counted, it would take a very large number of failures over a long period of time to gather sufficient data. Therefore, accelerated test methods using elevated temperatures are used. Temperature will accelerate the failures in a device and the increase can be expressed in a form of the Arrhenius equation which states the reaction rate increases exponentially with temperature.

$$R = R_o e^{\frac{-E}{kT}}$$

where:

- R = reaction rate as a function of time and temperature
- R_o = constant related to temperature
- T = Kelvin temperature
- E = activation energy (electron volts)

When this equation is plotted, as shown in Figures 3 and 4, it can be used to determine the failure rate at temperatures other than the test temperature of the device.

Quality Improvement

The quality and reliability activity at Raytheon is a thorough-going and continuous activity. It starts with the initial design concepts on a new device design and carries through to the finished production product being shipped to the customer.

Reliability Engineering, working with the Design or Product Engineer, monitors the new device design or process through all stages of development and remains the full and final authority over the qualification status of all products. A new device design, major process change or a new manufacturing facility will never ship a product to the customer until it has been fully documented, released to manufacturing and formally approved by the Reliability Department.

Raytheon has established several RA Qualification plans which are used to approve a new device, process or manufacturing facility. Two of these plans are shown in Tables 5 and 6 for hermetic package devices and plastic package devices.

The Reliability Department continually monitors all product lines through product sampling, the Generic Program and the QCI testing of JAN and other Hi-Rel products to evaluate failure modes and failure rates. The results from these tests are reviewed with Product and Production Engineering and any necessary corrective actions are taken.

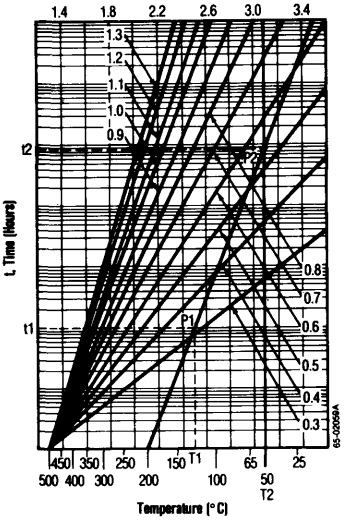


Figure 3. Normalized Time-Temperature Regressions for Various Activation Energy Values (1000/° K)

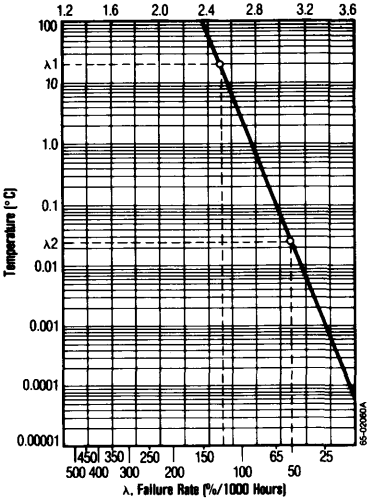


Figure 4. Failure Rate (1000/° K)

Table 1. Group A Electrical Tests[1]

Subgroup[2] [3]	Class B LTPD[4]
Subgroup 1 — Static tests at 25° C	2
Subgroup 2 — Static tests at maximum rated operating temperature	3
Subgroup 3 — Static tests at minimum rated operating temperature	5
Subgroup 4 — Dynamic tests at 25° C	2
Subgroup 5 — Dynamic tests at maximum rated operating temperature	3
Subgroup 6 — Dynamic tests at minimum rated operating temperature	5
Subgroup 7 — Functional tests at 25° C	2
Subgroup 8 — Functional tests at maximum and minimum operating temperatures	5
Subgroup 9 — Switching tests at 25° C	2
Subgroup 10 — Switching tests at maximum rated operating temperature	3
Subgroup 11 — Switching tests at minimum rated operating temperature	5

Notes:

1. The specific parameters to be included for tests in each subgroup shall be as specified in the applicable procurement document. Where no parameters have been identified in a particular subgroup or test within a subgroup, no group A testing is required for that subgroup or test to satisfy group A requirements.
2. A single sample may be used for all subgroup testing. Where the required size exceeds the lot size, 100% inspection shall be allowed (see 30.2.5 of Appendix B of MIL-M-38510).
3. Group A testing by subgroup or within subgroups may be performed in any sequence unless otherwise specified.
4. Maximum accept number allowed is 2.

Table 2. Group B Tests for Class B[1]

Test	MIL-STD-883		Quantity/ (Accept No.) or LTPD
	Method	Condition	
Subgroup 1 (a) Physical dimensions[2]	2016		2 devices (no failures)
Subgroup 2 (a) Resistance to solvents	2015		4 devices (no failures)
Subgroup 3 (a) Solderability[5]	2022 or 2003	Soldering temperature of 245 ±5° C	15
Subgroup 4 (a) Internal visual and mechanical[7]	2014	Failure criteria from design and construc tion requirements of applicable procure ment document	1 device (no failures)
Subgroup 5 (a) Bond strength[4] (1) Thermocompression (2) Ultrasonic or wedge (3) Flip-chip (4) Beam lead	2011	 (1) Test condition C or D (2) Test condition C or D (3) Test condition F (4) Test condition H	15
Subgroup 6[3] (a) Internal water-vapor content	1018	1,000 ppm maximum water content at 100° C	3 devices (0 failure) or 5 devices (1 failure)[6]
Subgroup 7[8] (a) Seal (1) Fine (2) Gross	1014	As applicable	5
Subgroup 8[9] (a) Electrical parameters (b) Electrostatic discharge sensitivity classification (c) Electrical parameters	3015	Group A, subgroup 1 Group A, subgroup 1	15(0)

Notes:

1. Electrical reject devices from the same inspection lot may be used for all subgroups when end-point measurements are not required, except devices being submitted to subgroup 7.
2. Not required for qualification or quality conformance inspection where group D inspection is being performed on samples from the same inspection lot.
3. This test is required only if the package contains a desiccant. Unless handling precautions for beryllia packages are available and followed method 1018, procedure 3 shall be used. See footnote 6 of Table 4 and paragraph 4 of method 1018 regarding delay in implementation of this requirement.

Notes (Continued)

4. Test samples for bond strength may, at the manufacturer's option, unless otherwise specified, be randomly selected prior to or following internal visual (PRESEAL) inspection specified in method 5004, prior to sealing provided all other specifications requirements are satisfied (e.g., bond strength requirements shall apply to each inspection lot, bond strength samples shall be counted even if the bond would have failed internal visual exam). Unless otherwise specified, the LTPD sample size for condition C or D is the number of bond pulls selected from a minimum number of 4 devices, and for condition F or H is the number of dice (not bonds) (see method 2011).
5. All devices submitted for solderability test shall be in the lead finish that will be on the shipped product and which has been through the temperature/time exposure of burn-in except for devices which have been hot solder dipped or undergone tin fusing after burn-in. The LTPD for solderability test applies to the number of leads inspected except in no case shall less than 3 devices be used to provide the number of leads required.
6. Test three devices; if one fails, test two additional devices with no failures.
7. Test samples for internal visual and mechanical shall be selected at any point following the seal operation and following marking see marking etc.
8. This test is not required if either the 100% screen or sample seal test is performed between 3.1.16 and 3.1.20 of method 5004.
9. Unless otherwise specified, test shall be performed for initial qualification and product redesign as a minimum.

Table 3. Group C (Die-Related Tests) (For Class B Only)

Test	MIL-STD-883		Quantity/ (Accept No.) or LTPD
	Method	Condition	
Subgroup 1			
(a) Steady state life test[1]	1005	Test condition to be specified (1,000 hours at 125° C)	5
(b) End-point electrical parameters		As specified in the applicable device specification	
Subgroup 2			
(a) Temperature cycling	1010	Test condition C	15
(b) Constant acceleration	2001	Test condition E min. (for large packages, see 3)	
(c) Seal	1014	As applicable	
(1) Fine			
(2) Gross			
(d) Visual examination	(Note 2)		
(e) End-point electrical parameters		As specified in the applicable device specification	

1. See 40.4 of Appendix B of MIL-M-38510 and 3.1 of method 1005.
2. Visual examination shall be in accordance with method 1010 or 1011.

Table 4 Group D (Package Related Tests) (For All Classes)

Test	MIL-STD-883		Quantity/ (Accept No.) or LTPD
	Method	Condition	
Subgroup 1[1]			
(a) Physical dimensions	2016		15
Subgroup 2[1]			
(a) Lead integrity[7]	2004	Test condition B_2 (lead fatigue)	15
(b) Seal			
(1) Fine	1014	As applicable	
(2) Gross			
Subgroup 3[3]			
(a) Thermal shock	1011	Test condition B as a minimum, 15 cycles minimum	15
(b) Temperature cycling	1010	Test condition C, 100 cycles minimum	
(c) Moisture resistance[8]	1004		
(d) Seal	1014	As applicable	
(1) Fine			
(2) Gross			
(e) Visual examination		Per visual criteria of method 1004 and 1010	
(f) End-point electrical parameters[4]		As specified in the applicable device specification	
Subgroup 4[3]			
(a) Mechanical shock	2002	Test condition B minimum	15
(b) Vibration, variable frequency	2007	Test condition A minimum	
(c) Constant acceleration	2001	Test condition E minimum (see 3), Y_1 orientation only	
(d) Seal	1014	As applicable	
(1) Fine			
(2) Gross			
(e) Visual examination	(Note 5)		
(f) End-point electrical parameters		As specified in the applicable device specification	
Subgroup 5[1]			
(a) Salt atmosphere[8]	1009	Test condition A minimum	15
(b) Seal	1014	As applicable	
Fine			
Gross			
(c) Visual examination		Per visual criteria of method 1009	

Table 4. Group D (Package Related Tests) (For All Classes) (Continued)

Test	MIL-STD-883		Quantity/ (Accept No.) or LTPD
	Method	Condition	
Subgroup 6[1] (a) Internal water-vapor content	1018	5,000 ppm maximum water content at 100° C	3 devices (0 failures) or 5 devices (1 failure)[6]
Subgroup 7[1] (a) Adhesion of lead finish[9] [10]	2025		15
Subgroup 8 (a) Lid torque[1] [2]	2024		5 (0)

Notes:

1. Electrical reject devices from that same inspection lot may be used for samples.
2. Lid torque test shall apply only to packages which use a glass-frit-seal to lead frame, lead or package body (i.e., wherever frit seal establishes hermeticity or package integrity).
3. Devices used in subgroup 3, "Thermal and Moisture Resistance" may be used in subgroup 4, "Mechanical."
4. At the manufacturer's option, end-point electrical parameters may be performed after moisture resistance and prior to seal test.
5. Visual examination shall be in accordance with method 1010 or 1011.
6. Test three devices; if one fails, test two additional devices with no failures. At the manufacturer's option, if the initial test sample (i.e., 3 or 5 devices) fails a second complete sample may be tested at an alternate laboratory that has been issued suitable by the qualifying activity. If this sample passes, the lot shall be accepted provided the devices and data from both submissions is submitted to the qualifying activity along with five additional devices from the same lot.
7. For leadless chip carrier packages only, use test condition D.
8. Lead bend stress initial conditioning is not required for leadless chip carrier packages.
9. The adhesion of lead finish test shall not apply for leadless chip carrier packages.
10. LTPD based on number of leads.

Table 5. Qual Plan for Hermetic Packages Devices

Test	Conditions Per MIL-STD-883	Quantity	Accept #
GROUP B			
Subgroup 3		15	0
Solderability	245 ±5° C		
Subgroup 4		1	0
Internal Visual			
Subgroup 5		15	0
Bond Strength	Condition C and record bond pull strength		
Subgroup 7		77	1
F & G Leak			
GROUP C			
Subgroup 1		100 initial 168 hours	—
Operational Life* (168, 250, 500*, 1000* hr) Electrical Test (25° C DC)	168-hour point will be used to screen out the infant mortality failure. The sample size after the 168 hr. point will be 77.	77 168-1000 hours	1
Subgroup 2		25	1
Temperature Cycle	Condition B, 15 cycles		
Constant Acceleration	Condition C, 100 cycles		
Moisture Resistance	10 Day		
F & G Leak			
Visual			
Electrical Test 25° C			
GROUP D			
Subgroup 2		25	1
Lead Integrity	Condition B_2		
F & G Leak			
Lid Torque			
Subgroup 4		25	1
Mechanical Shock	Condition B		
Vibration	Condition A		
Constant Acceleration	Condition B Min.		
F & G Leak			
Visual Examination			
Electrical Test 25° C			

*Interim Approval
**Final Approval

Table 6. Qualification Plan for Plastic Package Devices

Test	Quantity	Test Conditions	Purpose of Test	LTPD
Operating Life	100	Temperature 125° C Time 1000 Hours Electrical Test at 168 hrs., 500 hrs., 1000 hrs. Bias — per spec requirements NOTE: Samples from this test will continue for 2000 and 3000 hrs. evaluation.	Accelerated Life	7
Steam Pressure	55	Pressure 15 lbs. Temperature 120° C Time 96 hrs. Electrical Test at 48 hrs., (No Metal Deterioration) 96 hrs., 144 hrs., 250 hrs., 500 hrs., 1000 hrs.	Package integrity and moisture resistance	7
85° C/85% RH	55	Temperature 85° C Humidity 85% Time 250 hrs. (No Metal Deterioration) Electrical Test at 160 hrs., 250 hrs., 500 hrs., 1000 hrs.	Accelerated life corrosion resistance	7
Storage Life	32	Temperature 150° C Time 144 hrs. Bias — None Electrical Test at 144 hrs., 500 hrs.	Determine the effect of high temperature storage	7
Temperature Cycle	32	Temperature -55° C to 85° C No. Cycles 100 Electrical Test 25° C, 70° C	Determine the resistance to high and low temperatures	7
Moisture (10 Day)	22	Temperature -10° C to 65° C Humidity 90% RH Time 240 hrs. Electrical Test at 240 hrs. Visual Inspection of Leads	Package integrity to moisture, lead corrosion, etc.	7
Solderability	10	Per 883, Method 2003	To determine the solderability of the lead finish	7
Lead Fatigue	10	Per 883, Method 2004 Condition B	To determine the physical resistance to lead bending fatigue	7
External Visual	5	10-30X Magnification	To evaluate physical construction and processing results to package and lead frame.	

Lab Facilities

Raytheon maintains a fully equipped laboratory to conduct its reliability and environmental testing. The typical types of tests that are performed by this facility include:

- QCI Groups A, B, C and D environment requirements
- Destructive Physical Analysis (DPA)
- SEM Analysis
- X-ray Dispersion Analysis
- Biased 85/85 and Steam Pressure Pot (PCT)
- Reliability Analysis
- Electrical DC and Functional Testing

Plastic Package Devices

In recent years the availability and use of plastic encapsulated devices has become common for use in the commercial marketplace. Raytheon is a major supplier of Linear part types and has in the past and will continue to make significant investments in both the technology and production/manufacturing of plastic encapsulated Linear devices.

The switch from a "hermetic" package to a "plastic" package presents several potential reliability concerns. In the plastic encapsulated device, the entire die is encapsulated in the plastic molding compound. Since the plastic encapsulant is not hermetic, moisture can penetrate into the package over a period of time. This moisture can react with impurities present in the plastic or impurities brought into the package by the moisture to cause an electrical degradation of device parameters.

Recognizing the various potential failure modes associated with plastic encapsulated devices, Raytheon has adopted extensive manufacturing processes and evaluation procedures to assure the quality and reliability of its products.

Raytheon is continuously reviewing and evaluating the latest state-of-the-art materials and procedures to further improve the reliability of the plastic encapsulated products. In addition, Linear plastic encapsulated products are monitored by Quality Assurance (see Table 7) to assure compliance to specification.

These monitor tests along with additional generic evaluations show that *Raytheon's plastic package devices have accelerated failure rates of well below the industry standard and meet an outgoing quality goal of 500 ppm.*

Major Programs

Raytheon is involved with many major programs that require and support a high level of quality and reliability expertise in the design, manufacture and control of its I.C. products. The most significant of these programs is the JAN 38510 which requires a Defense Logistics Supply Center (DLSC) certification of its manufacturing lines, procedures and documentation and qualification approval (QPL) of the JAN devices manufactured on the certified line. The JAN military specs form the foundation of our QA system and all products — JAN and non-JAN — benefit accordingly.

In addition to JAN I.C. products, Raytheon offers several standard screening process flows which provide specific reliability levels and cost savings to fit your application requirements. These are identified in Figure 5 as A+1, A+2, A+3 and 883 and are in addition to custom design and specification control drawing (SCD) products.

A+ Program

The A+ programs are used for packaged devices and are designed to offer various levels of reliability screening intended to improve your expected device reliability, and hence your system reliability. The **A+1** program is used for plastic package devices and provides a temperature test that will screen out the assembly and package related failure modes. The **A+2** adds a burn-in stress test to screen out the chip-oriented infant mortality electrical failure modes. The **A+3** program is used for hermetic package devices and provides a burn-in stress test to screen out the infant mortality electrical failures (Figures 5, 6, and 7).

Table 7. Typical Plastic Process Monitor Tests

Test	Purpose of Test
Autoclave (steam pressure)	To evaluate the resistance of moisture penetration of the package and the effects of moisture on the chip under accelerated conditions of 15 pounds of steam pressure at 120° C.
Biased 85° C/ 85% RH	To evaluate the operate life and and resistance to moisture penetration of the chip and the plastic package under the accelerated conditions of 85° C and 85% relative humidity.
Operating Life	To evaluate the operational field life of the device under accelerated conditions of 125° C.
Temperature Cycle	To evaluate the mechanical strength of the device after stressing from -55° C to +85° C 100 cycles. Electrical testing is performed at 25° C and 100° C.
Resistance to Solvents	To determine that the brand markings will not become illegible on the package parts when subjected to the solvents and test per MIL-STD-883C, Method 2015.
Solderability	To assure the solderability of the lead finish at a solder temperature of 245° C using an RMA flux per Method 2004 of MIL-STD-883.
External Visual	To determine the physical construction and processing results to the package and lead frame at 30X magnification.
Lead Fatigue	To determine the physical resistance to lead bending fatigue per Condition B, Method 2004, of MIL-STD-883.
Thermal Shock	To determine that the device can survive exposure to rapid changes in temperature from -55° C to +125° C per Condition B of Method 1011 of MIL-STD-883.

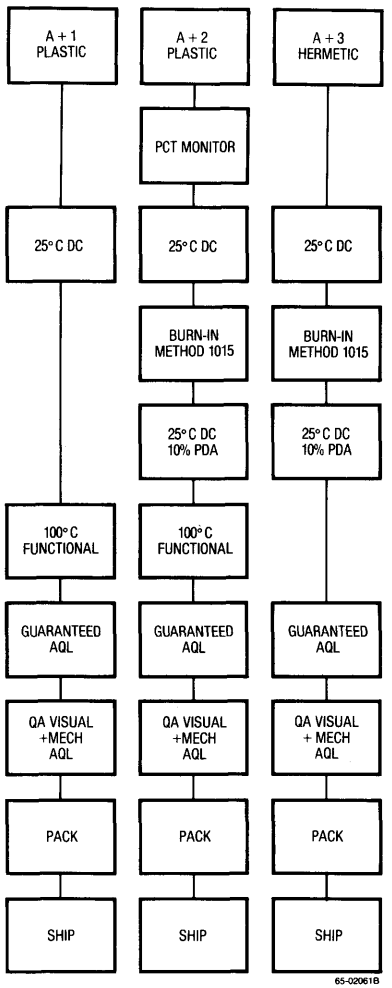


Figure 5. A+ Program Standard Flows

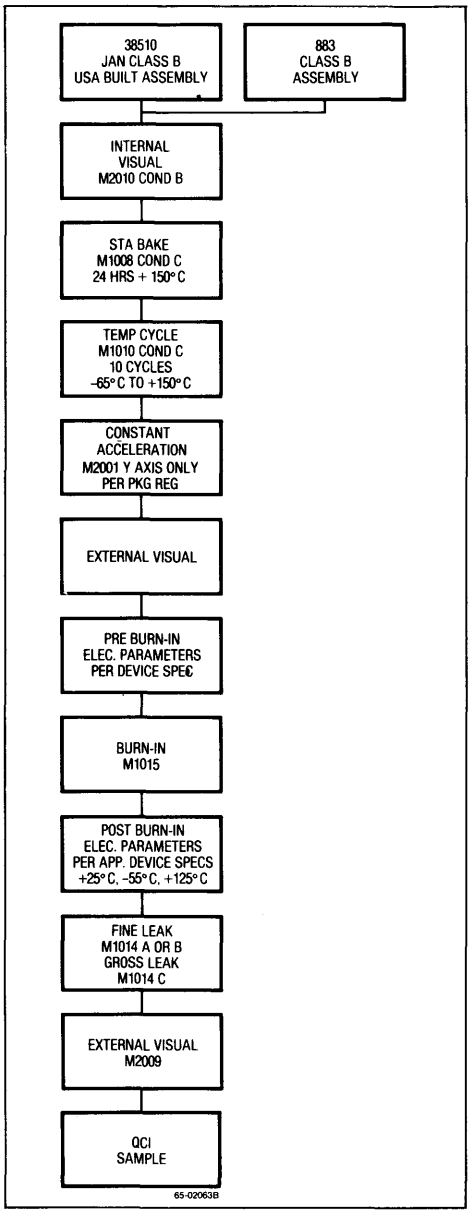


Figure 6. JAN883 Flow

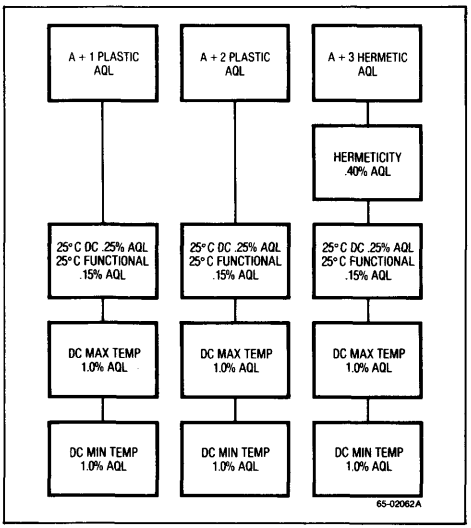


Figure 7. A+ Program AQL

Quality & Reliability

883

The JAN 883 program (often referred to as "JAN look-alikes") offers hermetic products built and tested to the MIL-M-38510 and MIL-STD-883 specification requirements. The parts may differ from JAN 38510 QPL parts only in the assembly location and in the electrical test specification. These parts are as close as one can get to JAN 38510 reliability using a standard process flow (Figure 6).

Generic Data Program

The Generic Data Program monitors on a continuing basis the reliability of all I.C. products in hermetic packages. This program requires that every 3 months several different part types from each microcircuit technology group as detailed in Appendix E of MIL-M-38510 be evaluated to the MIL-STD-883 Test Method 5005 Groups A, B and C test requirements. The data generated from this program provide a basic library of reliability information on many product types and can be used to provide Quality Conformance

Inspection (QCI) data to meet a customer's specific group test data requirements. It is also used as an additional QA monitor check. The specific tests performed for Groups A, B and C are shown in Tables 2, 3, and 4.

JAN MIL-M-38510

A major program to which Raytheon is committed is the JAN MIL-M-38510 program for Linear devices. The program is administered by the Defense Electronics Supply Center (DESC) and the Defense Logistics Agency (DLA) of the Department of Defense. Raytheon maintains DESC certified manufacturing lines that provide an extensive number of qualified JAN QPL Linear device types.

The JAN 38510 program is designed to provide high reliability devices in hermetic packages manufactured to a standard process flow and quality/reliability program as detailed by the MIL-M-38510, MIL-STD-883 and MIL-STD-976 specifications (refer to Tables 8 and 9). The JAN 38510/883 program and specification is the base line, accepted process to which most high reliability non-JAN devices are referenced and manufactured.

A JAN QPL device is identified and branded by a unique part mark system. Tables 8 and 9 explain the part marking system and the package codes.

All JAN parts will be branded with this military designator part number in addition to the electrostatic discharge sensitivity identifier (Δ) date codes, manufacturer's designated symbol (CRP) and identification (RAY).

Table 8. MIL-M-38510 Part Marking

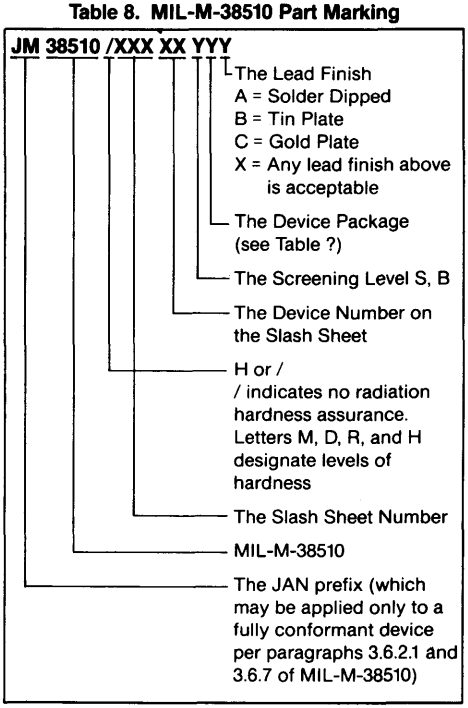


Table 9. JAN Package Codes

38510 Package Designation	Microcircuit Industry Description
A	14-pin 1/4" x 1/4" (metal) flat pack
B	14-pin 3/16" x 1/4" flat pack
C	14-pin 1/4" x 3/4" dual in-line
D	14-pin 1/4" x 3/8" (ceramic) flat pack
E	16-pin 1/4" x 7/8" dual in-line
F	16-pin 1/4" x 3/8" (metal or ceramic) flat pack
G	8-pin TO-99 can or header
H	10-pin 1/4" x 1/4" (metal) flat pack
I	10-pin TO-100 can or header
J	24-pin 1/2" x 1/4" dual in-line
K	24-pin 3/8" x 5/8" flat pack
M	12-pin TO-101 can or header
P	8-pin 1/4" x 3/8" dual in-line
Q	40-pin 8/16" x 2-1/16" dual in-line
R	26-pin 1/4" x 1-1/16" dual in-line
S	20-pin 1/4" x 1/2" flat pack
V	18-pin 3/8" x 15/16" dual in-line
W	22-pin 3/8" x 1-1/8" dual in-line
X	Unassigned — Reserved for identifying special packages whose dimensions are carried in the detail specifications
Y	
Z	

Section 6
Operational Amplifiers

Raytheon has long been a manufacturer of monolithic op amps, and is a supplier of high reliability op amps to the defense industry. Raytheon introduced the world's first quad op amp, and continues to make a complete line of general purpose, audio, single supply, and precision op amps. Raytheon's manufacturing process was created specifically for low noise type op amps. Low noise is not a black art; quality starting materials and chemicals, careful temperature changes, and two extra processing steps to ensure crystal lattice uniformity all contribute to this low noise process.

Important to instrumentation applications is Raytheon's "zener zap" method of trimming rather than laser trimming. Zener zap trimming gives better long term stability and drift, because small segments of resistor are shorted with metal connections, rather than being destructively burned away with laser power. Permanent metal shorts are not subject to contamination and "healing" as laser trimmed resistors are.

Main groupings of products are as follows:

General Purpose — RC741 and LM101 type op amps available in single, dual, and quad layouts, packaged in metal cans and in plastic or ceramic dual in-line packages (DIPs).

Audio — RC5534 types in single or dual configuration, and dual and quad high performance types such as the RC4156 quad op amp.

Single Supply — Singles, duals, and quads including micropower, improved slew rate, and current mode op amps designed to operate on one supply voltage (ground sensing).

Precision — Singles and duals of the OP series, including decompensated high speed OP-37s and 47s, and low cost precision types such as the RC714.

DEFINITIONS

Average Input Bias Current Drift (TC_{IB})
The ratio of change in input bias current to a change in ambient temperature, expressed in nanoamps per degree C (nA/° C).

$$TC_{IB} = \frac{I_B @ T_{(1)} - I_B @ T_{(2)}}{T_{(1)} - T_{(2)}}$$

Where $T_{(1)}$ and $T_{(2)}$ are the upper and lower limits of the specified temperature range.

Average Input Offset Current Drift (TC_{IOS})
The ratio of change in input offset current to a change in ambient temperature, expressed in nanoamps per degree C (nA/° C).

$$TC_{IOS} = \frac{I_{OS} @ T_{(1)} - I_{OS} @ T_{(2)}}{T_{(1)} - T_{(2)}}$$

Where $T_{(1)}$ and $T_{(2)}$ are the upper and lower limits of the specified temperature range.

Average Input Offset Voltage Drift (TC_{VOS})
The ratio of change in input offset voltage to a change in ambient temperature, expressed in microvolts per degree C (μV/° C).

$$TC_{VOS} = \frac{V_{OS} @ T_{(1)} - V_{OS} @ T_{(2)}}{T_{(1)} - T_{(2)}}$$

Where $T_{(1)}$ and $T_{(2)}$ are the upper and lower limits of the specified temperature range.

Channel Separation
The ratio of output voltage of an amplifier to the output voltage of an adjacent amplifier whose gain is 100, and whose inputs are grounded, expressed in decibels (dB). Channel separation is measured at the outputs of adjacent amplifiers:

$$\text{Channel Separation} = 20LOG_{10}\left(\frac{100V_{O(1)}}{V_{O(2)}}\right)$$

Where $V_{O(1)}$ and $V_{O(2)}$ are the independent and dependent amplifier output voltages.

Common Mode Rejection Ratio (CMRR)
The ratio of change of input common mode voltage (both inputs swing together over a specified voltage range) to a change in input offset voltage, expressed in decibels (dB).

$$CMRR = 20LOG_{10}\left(\frac{V_{IN(1)} - V_{IN(2)}}{V_{OS} @ V_{IN(1)} - V_{OS} @ V_{IN(2)}}\right)$$

Where $V_{IN(1)}$ and $V_{IN(2)}$ are the upper and lower limits of the input common mode voltage range.

Distortion (THD)
The large signal harmonic distortion between input and output under closed loop conditions, expressed in percent at a specified frequency.

Gain Bandwidth Product (GBW)
The frequency at which the open loop gain equals unity, expressed in Hertz (Hz).

Input Bias Current (I_B)
The average of the two input currents with the output voltage at the center of its swing with no load, expressed in nanoamps (nA).

Input Noise Current
The peak-to-peak noise current within a specified frequency band, expressed in nanoamps or picoamps (nA or pA).

Input Noise Current Density (I_N)
The rms noise current in a 1 Hertz band centered on a specified frequency, expressed in picoamps per root Hertz (pA/$\sqrt{Hz}$).

Input Noise Voltage
The peak-to-peak noise voltage within a specified frequency band, expressed in nanovolts or microvolts (nV or μV).

Input Noise Voltage Density (e_n)
The rms noise voltage in a 1 Hertz band centered on a specified frequency, expressed in nanovolts per root Hertz (nV/$\sqrt{Hz}$).

Input Offset Current (I_{OS})
The difference between the two input currents with the output voltage at the center of its swing with no load, expressed in nanoamps (nA).

Input Offset Voltage (V_{OS})
The voltage that must be applied between the two inputs to obtain an output voltage in the

DEFINITIONS (Continued)

center of the output swing range, expressed in millivolts or microvolts (mV or μV).

Input Resistance (Common Mode)
The ratio of input voltage change to the resulting change in input bias current, expressed in megaohms or gigaohms (MΩ or GΩ).

$$\text{Common mode } R_{IN} = \frac{V_{(1)} - V_{(2)}}{I_B @ V_{(1)} - I_B @ V_{(2)}}$$

Where $V_{(1)}$ and $V_{(2)}$ are the upper and lower limits of the input voltage range.

Input Resistance (Differential Mode)
The ratio of small signal change in input offset voltage to a change in input current at either input terminal with the other grounded, expressed in megaohms (MΩ).

Input Voltage Range
The range of voltages at the inputs over which the amplifier operates within its common mode rejection ratio specification, expressed in volts (V).

Large Signal Voltage Gain (A_V)
The ratio of a specified output voltage change to the change in input offset voltage required to effect the change under open loop conditions, expressed in volts per millivolt (V/mV).

$$A_V = \frac{V_{O(1)} - V_{O(2)}}{V_{OS(1)} - V_{OS(2)}}$$

Where $V_{O(1)}$ and $V_{O(2)}$ are the specified upper and lower voltage limits for the change at the output.

Long Term Input Offset Voltage Stability
The averaged trend line of V_{OS} vs. time over extended periods after the first 30 days of operation, expressed in microvolts per month (μV/Mo).

Offset Adjustment Range
The change in V_{OS} that can be produced using the specified external offset adjustment circuit, expressed in millivolts (mV).

Open Loop Output Resistance (R_O)
The resistance seen looking into the output with the output at the center of its swing, under small signal conditions, expressed in ohms (Ω).

Output Sink Current
The current flowing into the output for a specified set of input and output conditions, measured in milliamps (mA).

Output Source Current
The current flowing out of the output for a specified set of input and output conditions, measured in milliamps (mA).

Output Voltage Swing
The peak output change, referred to ground, that can be obtained for a specified load resistance, expressed in volts (V).

Overshoot
The positive or negative going excursion that exceeds the final settled condition at the output of a closed loop unity gain amplifier, expressed as a percentage of the output step.

Phase Margin
The difference between the amplifier phase shift and 180° at the frequency where the open loop gain equals unity, expressed in degrees.

$$\text{Phase margin} = 180° - \phi$$

Where ϕ equals the input-output phase shift at $A_V = 1$.

Power Bandwidth
The maximum frequency at which a specified peak voltage sine wave may be obtained, measured in Hertz (Hz).

Power Consumption
The DC power required to operate the amplifier with the output at the center of its swing and zero load current, expressed in milliwatts (mW).

DEFINITIONS (Continued)

Power Supply Rejection Ratio (PSRR)
The ratio of change of supply voltage to a change in input offset voltage, expressed in decibels (dB).

$$PSRR = 20LOG_{10}\left(\frac{V_{S(1)} - V_{S(2)}}{V_{OS} @ V_{S(1)} - V_{OS} @ V_{S(2)}}\right)$$

Where $V_{S(1)}$ and $V_{S(2)}$ are the upper and lower limits of the specified change of supply voltage.

Rise Time
The time required for an output voltage step to change from 10% to 90% of its final value, expressed in nanoseconds (nS).

Short Circuit Current
The maximum output current available from the amplifier with the output shorted to ground, expressed in milliamps (mA).

Slew Rate
The average rate of change of output voltage under large signal overdriven conditions, expressed in volts per microsecond (V/μS).

Supply Current (I_S)
The current required from the power supply to operate the amplifier under quiescent no load conditions, expressed in milliamps (mA).

Supply Voltage (V_S)
The range of power supply voltages over which the amplifier will operate, expressed in volts (V).

Unity Gain Bandwidth
The frequency at which the small signal voltage gain is 3dB below unity when operated as a closed loop unity gain follower, expressed in Hertz (Hz).

Raytheon

General Purpose Quad Operational Amplifier

HA-4741

Features

- Unity gain bandwidth — 3.5MHz (typ)
- High slew rate — 1.6V/μS (typ)
- Low noise voltage — 9nV/√Hz (typ)
- Input offset voltage — 0.5mV (typ)
- Input bias current — 60nA (typ)
- Indefinite short circuit protection
- No crossover distortion
- Internal compensation
- Wide power supply range — ±2V to ±20V

Applications

- Universal active filters
- Audio amplifiers
- Battery powered equipment
- D3 communications filters

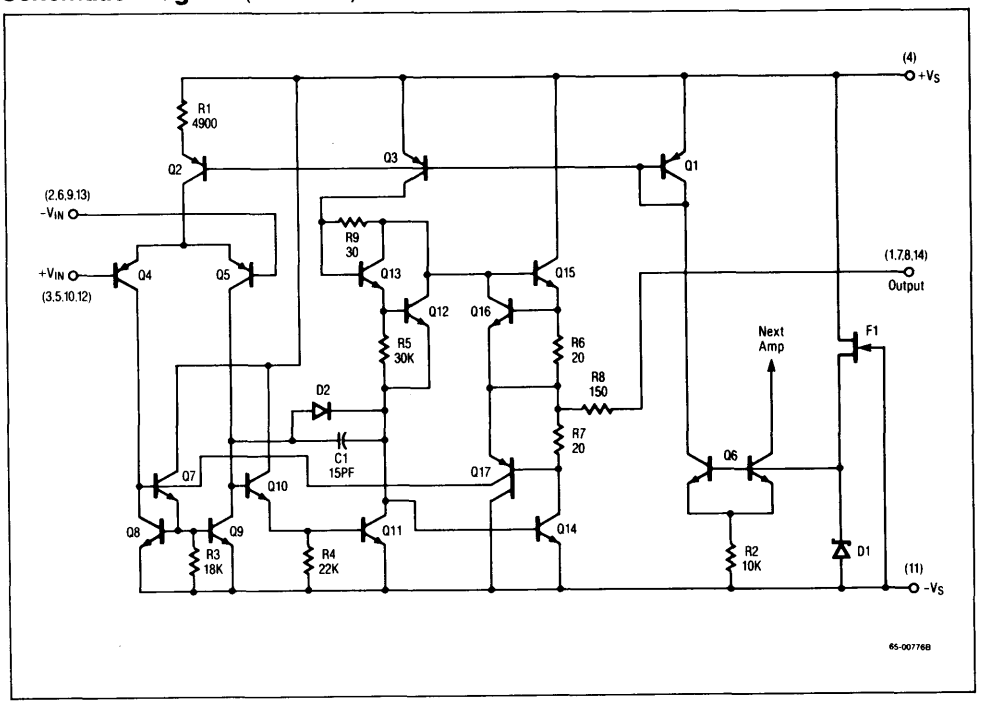
Description

The HA-4741 is a monolithic integrated circuit, consisting of four independent operational amplifiers constructed with the planar epitaxial process.

These amplifiers feature AC and DC performance which exceed that of the 741 type amplifiers. Its superior bandwidth, slew rate and noise characteristics make it an excellent choice for active filter or audio amplifier applications.

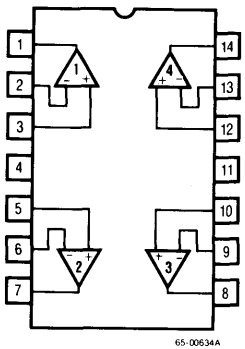
A wide range of supply voltage (±2V to ±20V) can be used to power the HA-4741, making it compatible with almost any system including battery powered equipment.

Schematic Diagram (1/4 Shown)



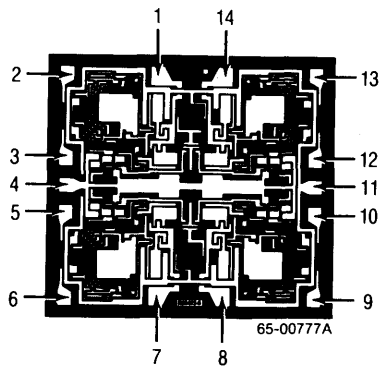
Connection Information

14-Lead
Dual In-Line Package
(Top View)



Pin	Function
1	Output A
2	$-V_{IN}$ A
3	$+V_{IN}$ A
4	$+V_S$
5	$+V_{IN}$ B
6	$-V_{IN}$ B
7	Output B
8	Output C
9	$-V_{IN}$ C
10	$+V_{IN}$ C
11	$-V_S$
12	$+V_{IN}$ D
13	$-V_{IN}$ D
14	Output D

Mask Pattern



Die Size: 80 x 84 mils
Min. Pad Dimension: 4 x 4 mils

Absolute Maximum Ratings

Supply Voltage ..... ±20V
Differential Input Voltage 30V
Input Voltage[1] ..... ±15V
Output Short Circuit
Duration[2] ..... Indefinite
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
HA-4741-2 or -8 ..... -55°C to +125°C
HA-4741-5 ..... 0°C to +70°C
Lead Soldering Temperature
(60 Sec) ..... +300°C

Notes: 1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Short circuit to ground on one amplifier only.

Thermal Characteristics

	14-Lead Plastic DIP	14-Lead Ceramic DIP
Max. Junction Temp.	125°C	175°C
Max. P_D $T_A < 50°C$	468mW	1042mW
Therm. Res. θ_{JC}	—	60°C/W
Therm. Res. θ_{JA}	160°C/W	120°C/W
For $T_A > 50°C$ Derate at	6.25mW per °C	8.33mW per °C

Ordering Information

Part Number	Package	Operating Temperature Range
HA1-4741-5	Plastic	0°C to +70°C
HA3-4741-5	Ceramic	0°C to +70°C
HA1-4741-2	Ceramic	-55°C to +125°C
HA1-4741-8*	Ceramic	-55°C to +125°C

*MIL-STD-883, Level B Processing

Electrical Characteristics ($V_S = \pm 15V$ and $T_A = +25°C$ unless otherwise specified)

Parameters	Test Conditions	HA-4741-2			HA-4741-5			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 10k\Omega$		0.5	3.0		1.0	5.0	mV
Input Offset Current			15	30		30	50	nA
Input Bias Current			60	200		60	300	nA
Input Resistance			0.5			0.5		MΩ
Large Signal Voltage Gain	$R_L \geq 2k\Omega$ $V_{OUT} \pm 10V$	50	100		25	50		V/mV
Input Voltage Range		±12			±12			V
Output Resistance			300			300		Ω
Output Current	$V_{OUT} \pm 10V$	±5	±15		±5	±15		mA
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$ $\Delta V = \pm 5V$	80			80			dB
Supply Current (All Amplifiers)			4.5	5.0		5.0	7.0	mA
Transient Response Rise Time			75			75		nS
Overshoot			25			25		%
Slew Rate			1.6			1.6		V/μS
Unity Gain Bandwidth			3.5			3.5		MHz
Power Bandwidth	$V_O = 20Vp\text{-}p$ $R_L = 2k$		25			25		kHz
Input Noise Voltage Density	f = 1kHz		9.0			9.0		$nV/\sqrt{Hz}$
Channel Separation			108			108		dB

Electrical Characteristics (Continued)

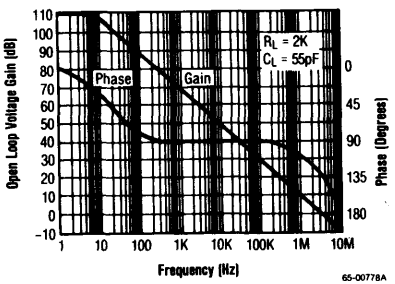
(V_S = ±15V and -55°C ≤ T_A ≤ +125°C for HA-4741-2, 0°C ≤ T_A ≤ +70°C for HA-4741-5)

Parameters	Test Conditions	HA-4741-2			HA-4741-5			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 10k\Omega$		4.0	5.0		5.0	6.5	mV
Input Offset Current				75			100	nA
Input Bias Current				325			400	nA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$ V_{OUT} ±10V	25			15			V/mV
Output Voltage Swing	$R_L \geq 10k\Omega$	±12	±13.7		±12	±13.7		V
	$R_L \geq 2k\Omega$	±10	±12.5		±10	±12.5		V
Supply Current (All Amplifiers)			10			10		mA
Average Input Offset Voltage Drift			5.0			5.0		µV/°C
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$ ΔV ±5.0V	74			74			dB
Power Supply Rejection Ratio	$R_S \leq 10k\Omega$ ΔV ±5.0V	80			80			dB

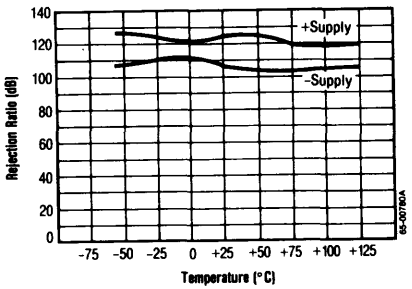
Typical Performance Characteristics

($+V_S$ = +15V, $-V_S$ = -15V, T_A = +25°C unless otherwise noted)

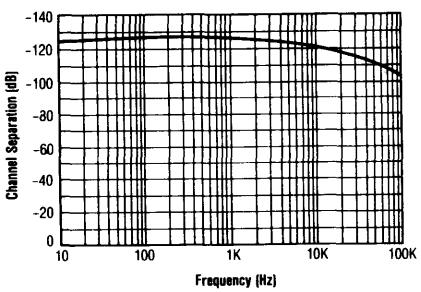
Open Loop Frequency Response

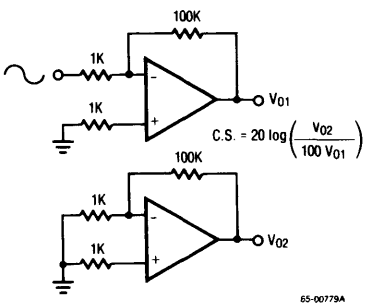


Power Supply Rejection Ratio vs. Temperature

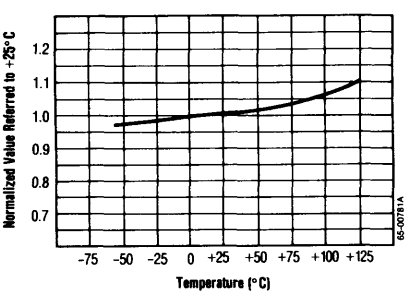


Channel Separation vs. Frequency

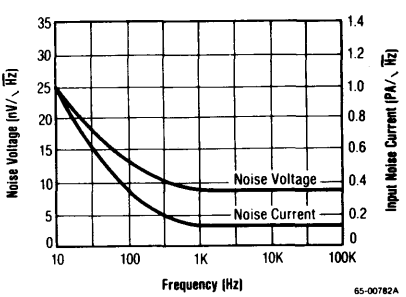




Transient Response vs. Temperature

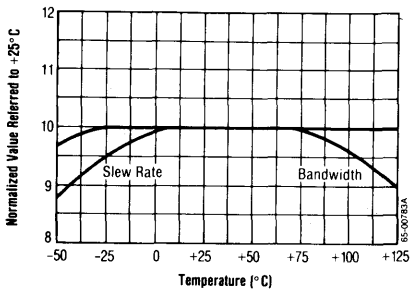


Input Noise vs. Frequency

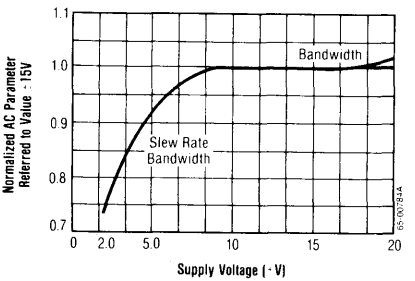


Typical Performance Characteristics (Continued)

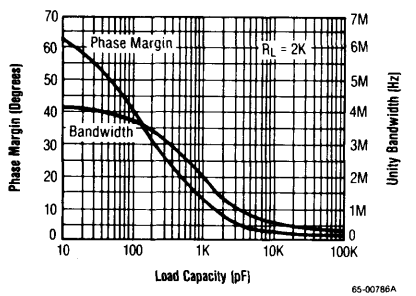
Normalized AC Parameters vs. Temperature



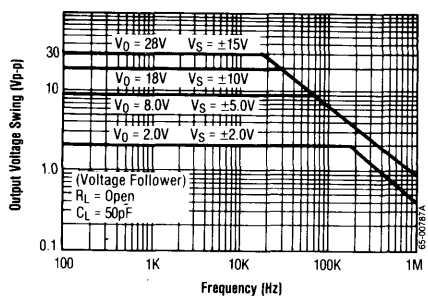
Slew Rate vs. Supply Voltage



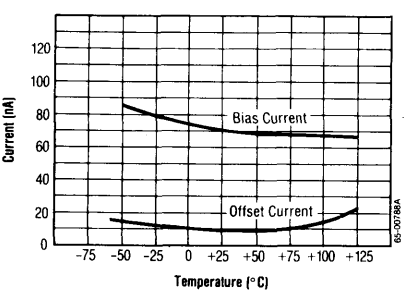
Small Signal Bandwidth and Phase Margin vs. Load Capacitance



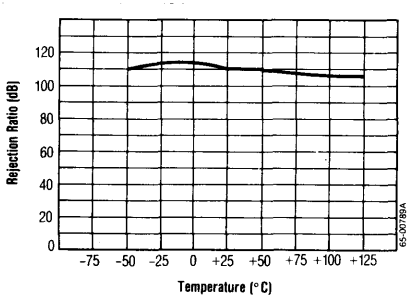
Output Voltage Swing vs. Frequency



Input Currents vs. Temperature

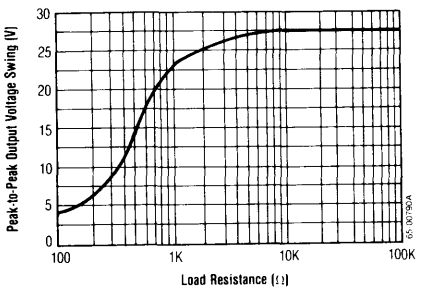


Common Mode Rejection Ratio vs. Temperature



Typical Performance Characteristics (Continued)

Maximum Output Voltage Swing vs. Load Resistance



Raytheon

General Purpose Operational Amplifier

LM101A/ 201A/301A

Features

- Offset voltage 3.0mV maximum over temperature
- Input current 100nA maximum over temperature
- Offset current 20nA maximum over temperature
- Offsets guaranteed over entire common-mode range and supply voltage range
- Frequency compensated 30pF
- Supply voltage ±5.0V to ±20V

Description

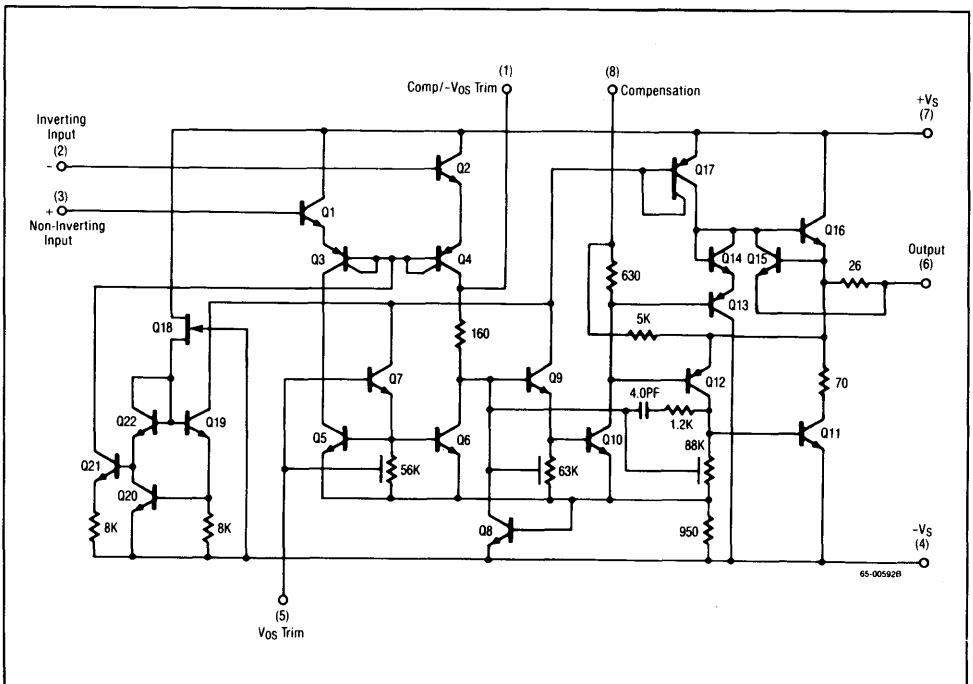
The LM101A, 201A, and 301A are general purpose high performance operational amplifiers fabricated monolithically on a silicon chip by an advanced epitaxial process. The units may be fully compensated with the addition of a 30pF capacitor stabilizing the circuit for all feedback configurations including capacitive loads.

The device may be operated as a comparator with a differential input as high as ±30V. Used as a comparator the output can be clamped at any desired level to make it compatible with logic circuits.

The LM101A operates over the full military temperature range from -55°C to +125°C. The commercial version, LM301A operates over a temperature range from 0°C to +70°C.

The LM201A is the same as the LM101A except its performance is guaranteed from -25°C to +85°C.

Schematic Diagram

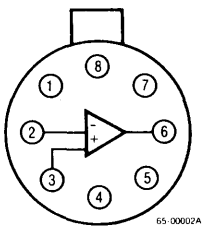


LM101A/201A/301A

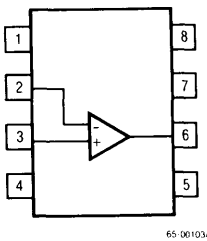
General Purpose Operational Amplifier

Connection Information

8-Lead Metal Can TO-99
(Top View)



8-Lead Dual In-Line Package
(Top View)



Pin	Function
1	Comp/V_{OS} Trim
2	-Input
3	+Input
4	$-V_S$
5	V_{OS} Trim
6	Output
7	$+V_S$
8	Comp

Absolute Maximum Ratings

Supply Voltage
- LM101A/LM201A ..... ±22V
- LM301A ..... ±18V

Differential Input Voltage 30V

Input Voltage[1] ..... ±15V

Output Short-Circuit Duration[2] ..... Indefinite

Storage Temperature Range ..... -65°C to +150°C

Operating Temperature Range
- LM101A ..... -55°C to +125°C
- LM201A ..... -25°C to +85°C
- LM301A ..... 0°C to +70°C

Lead Soldering Temperature (60 Sec) ..... +300°C

Notes:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Continuous short-circuit is allowed for case temperatures to +125°C and ambient temperatures to +75°C for LM107; case temperatures to +70°C and ambient temperatures to +55°C for LM307.

Thermal Characteristics

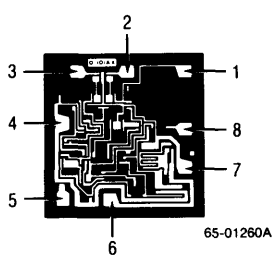
	8-Lead Plastic DIP	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can
Max. Junc. Temp.	125°C	175°C	175°C
Max. P_D T_A < 50°C	468mW	833mW	658mW
Therm. Res. θ_{JC}	—	45°C/W	50°C/W
Therm. Res. θ_{JA}	160°C/W	150°C/W	190°C/W
For T_A > 50°C Derate at	6.25mW per °C	8.33mW per °C	5.26mW per °C

Ordering Information

Part Number	Package	Operating Temperature Range
LM101ADE	Ceramic	-55°C to +125°C
LM101ADE/883B*	Ceramic	-55°C to +125°C
LM101AH	TO-99	-55°C to +125°C
LM101AH/883B*	TO-99	-55°C to +125°C
LM201ADE	Ceramic	-25°C to +85°C
LM201AH	TO-99	-25°C to +85°C
LM301ADE	Ceramic	0°C to +70°C
LM301AH	TO-99	0°C to +70°C
LM301AN	Plastic	0°C to +70°C

*MIL-STD-883, Level B Processing

Mask Pattern



Die Size: 55 x 55 mils
Min. Pad Dimension: 4 x 4 mils

Electrical Characteristics

(C = 30pF; LM101A, LM201A: $\pm 5.0V \leq V_S \leq \pm 20V$; LM301A: $\pm 5.0V \leq V_S \leq \pm 15V$; see Note 1)

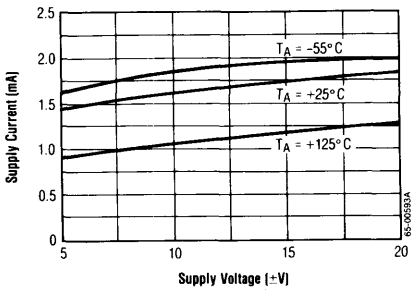
Parameters	Test Conditions	LM101A/LM201A			LM301A			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = +25°C$, $R_S \leq 50k\Omega$		0.7	2.0		2.0	7.5	mV
Input Offset Current	$T_A = +25°C$		1.5	10		3.0	50	nA
Input Bias Current	$T_A = +25°C$		30	75		70	250	nA
Input Resistance	$T_A = +25°C$	1.5	4.0		0.5	2.0		MΩ
Supply Current	$T_A = +25°C$ (Note 2)		1.8	3.0		1.8	3.0	mA
Large Signal Voltage Gain	$T_A = +25°C$, $V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	50	160		25	160		V/mV
Input Offset Voltage	$R_S \leq 50k\Omega$			3.0			10	mV
Average Input Offset Voltage Drift			3.0	15		6.0	30	μV/°C
Input Offset Current				20			70	nA
Average Input Offset Current Drift	$+25°C \leq T_A \leq +125°C$		0.01	0.1				nA/°C
	$+25°C \leq T_A \leq +70°C$					0.01	0.3	
	$-55°C \leq T_A \leq +25°C$		0.02	0.2				
	$0°C \leq T_A \leq +25°C$					0.02	0.6	
Input Bias Current				100			300	nA
Supply Current	$T_A = +125°C$, $V_S = \pm 20V$		1.2	2.5				mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	25			15			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k\Omega$	±12	±14		±12	±14		V
	$R_L \geq 2k\Omega$	±10	±13		±10	±13		
Input Voltage Range	(Note 2)	±15			±12			V
Common Mode Rejection Ratio	$R_S \leq 50k\Omega$	80	96		70	90		dB
Power Supply Rejection Ratio	$R_S \leq 50k\Omega$	80	96		70	96		dB

Notes: 1. These specifications apply for $-55°C < T_A < +125°C$ LM101A, $-25°C$ to $+85°C$ LM201A, and $0°C < T_A < +70°C$ LM301A, unless otherwise specified.

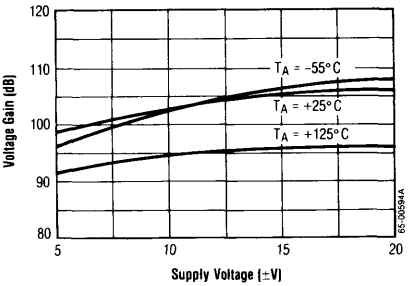
2. $V_S = \pm 20V$ for LM101A and LM201A, $V_S = \pm 15V$ for LM301A.

Typical Performance Characteristics

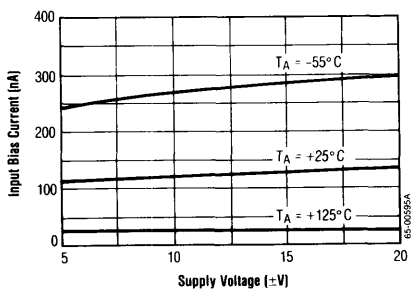
Supply Current



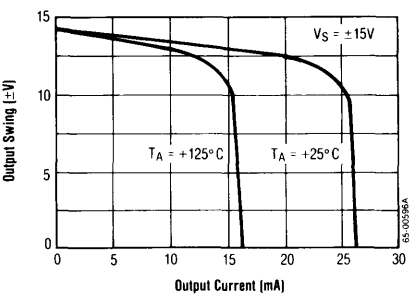
Voltage Gain



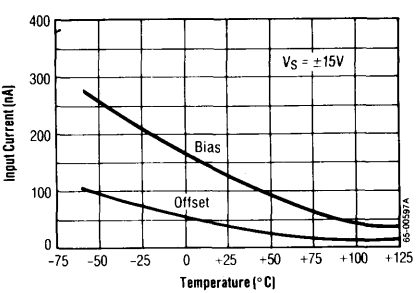
Input Bias Current



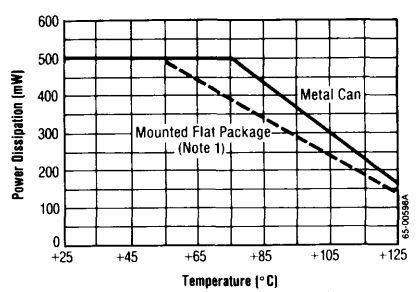
Current Limiting



Input Current

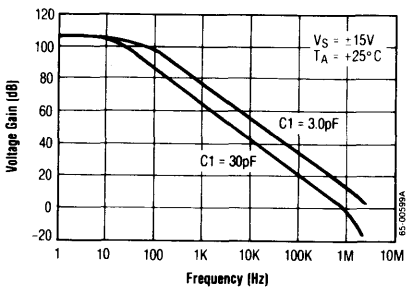


Maximum Power Dissipation

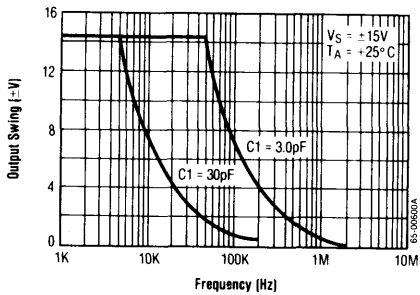


Typical Performance Characteristics (Continued)

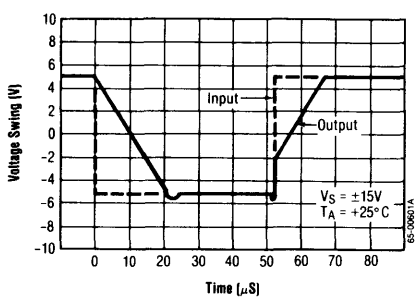
Open Loop Frequency Response



Large Signal Frequency Response

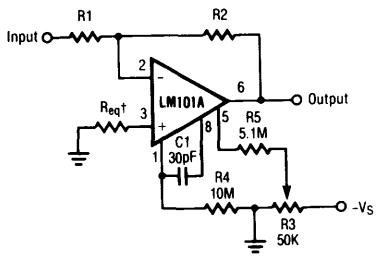


Voltage Follower Pulse Response



Typical Applications

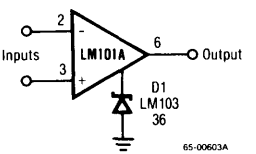
Inverting Amplifier With Balancing Circuit



†May be zero or equal to parallel combination of R1 and R2 for minimum offset.

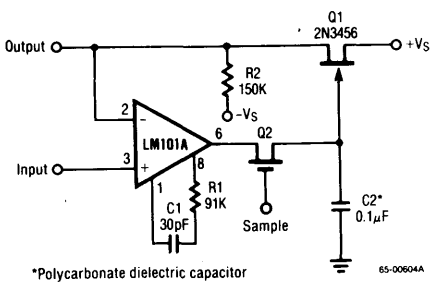
65-00602A

Voltage Comparator for Driving DTL or TTL Integrated Circuits



65-00603A

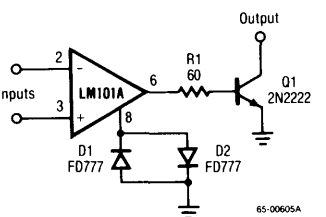
Low Drift Sample and Hold



*Polycarbonate dielectric capacitor

65-00604A

Voltage Comparator for Driving RTL Logic or High Current Driver



65-00605A

Raytheon

Single-Supply Quad Operational Amplifiers

LM124/224/324
2902

Features

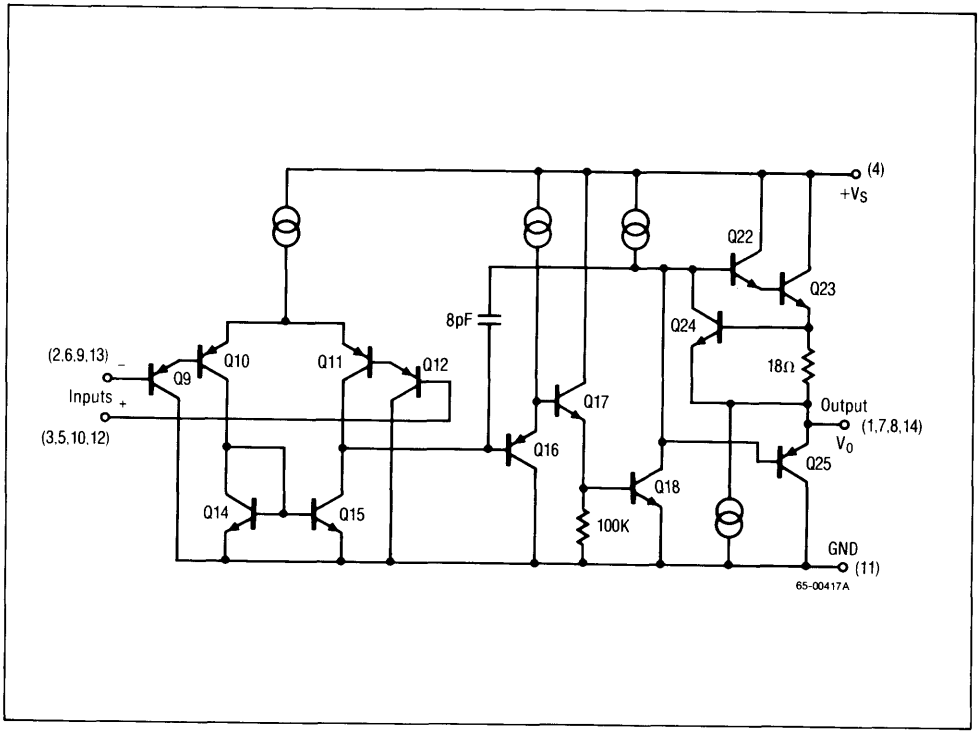
- Large DC voltage gain — 100dB
- Compatible with all forms of logic
- Temperature compensated
- Wide bandwidth at unity gain frequency — 1MHz
- Large output voltage swing — 0V to $+V_S$ -1.5V
- Input common mode voltage range includes ground

Description

Each of the devices in this series consists of four independent high-gain operational amplifiers that are designed for single-supply operation. Operation from split power supplies is also possible and the low power supply drain is independent of the magnitude of the power supply voltage.

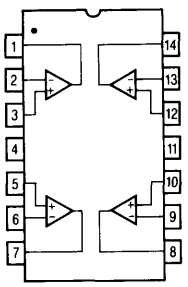
Used with a dual supply, the circuit will operate over a wide range of supply voltages. However, a large amount of crossover distortion may occur with loads to ground. An external current-sinking resistor to $-V_S$ will reduce crossover distortion. There is no crossover distortion problem in single-supply operation if the load is direct-coupled to ground.

Schematic Diagram (¼ Shown)



Connection Information

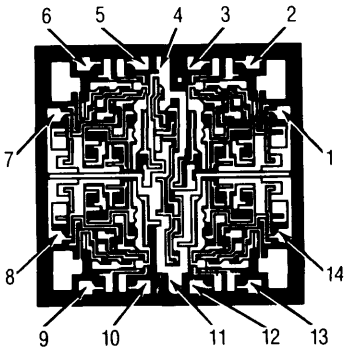
14-Lead
Dual In-Line Package
(Top View)



65-00418A

Pin	Function
1	Output 1
2	-Input 1
3	+Input 1
4	$+V_S$
5	+Input 2
6	-Input 2
7	Output 2
8	Output 3
9	-Input 3
10	+Input 3
11	Ground
12	+Input 4
13	-Input 4
14	Output 4

Mask Pattern



Die Size: 74 x 75 mils
Min. Pad Dimensions: 4 x 4 mils

Absolute Maximum Ratings

Supply Voltage, $+V_S$
- LM124/224/324 ..... +32V or ±16V
- LM2902 ..... +26V or ±13V

Differential Input Voltage
- LM124/224/324 ..... 32V
- LM2902 ..... 26V

Input Voltage ..... -0.3V to +32V

Output Short Circuit to GND
(One Amplifier) $+V_S \leq 15V$ and
$T_A = +25°C$[1] ..... Continuous

Input Current ($V_{IN} < -0.3V$)[2] 50mA

Operating Temperature Range
- LM124 ..... -55°C to +125°C
- LM224 ..... -25°C to +85°C
- LM324 ..... 0°C to +70°C
- LM2902 ..... -40°C to +85°C

Thermal Characteristics

	14-Lead Micro-pak Plastic DIP	14-Lead Plastic DIP	14-Lead Ceramic DIP
Max. Junction Temp.	125°C	125°C	175°C
Max. P_D $T_A < 50°C$	300mW	468mW	1042mW
Therm. Res. θ_{JC}	—	—	60°C/W
Therm. Res. θ_{JA}	200°C/W	160°C/W	120°C/W
For $T_A > 50°C$ Derate at	5.0mW per °C	6.25mW per °C	8.38mW per °C

Ordering Information

Part Number	Package	Operating Temperature Range
LM324J	Ceramic	0°C to +70°C
LM324M	Micro Plastic	0°C to +70°C
LM324N	Plastic	0°C to +70°C
LM224J	Ceramic	-25°C to +85°C
LM224N	Plastic	-25°C to +85°C
LM2902N	Plastic	-40°C to +85°C
LM124J	Ceramic	-55°C to +125°C
LM124J/883B*	Ceramic	-55°C to +125°C

*MIL-STD-883, Level B Processing

Electrical Characteristics ($+V_S$ = +5.0V[3])

Parameters	Test Conditions	LM124/224			LM324			LM2902			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[4]	T_A = +25°C		±2.0	±5.0		±2.0	±7.0		±2.0	±7.0	mV
Input Bias Current[5]	T_A = +25°C		45	150		45	250		45	250	nA
Input Offset Current	T_A = +25°C		±3.0	±30		±5.0	±50		±5.0	±50	nA
Input Voltage Range[6]	$+V_S$ = +30V, T_A = +25°C	0		$+V_S$ -1.5	0		$+V_S$ -1.5	0		$+V_S$ -1.5	V
Supply Current	R_L = ∞, $+V_S$ = 30V, (LM2902 $+V_S$ = 26V)		1.5	3.0		1.5	3.0		1.5	3.0	mA
	R_L = ∞ On All Op Amps		0.7	1.2		0.7	1.2		0.7	1.2	mA
Large Signal Voltage Gain	$+V_S$ = 15V (For Large V_O Swing) $R_L \geq 2.0k\Omega$, T_A = +25°C	50	100		25	100			100		V/mV
Output Voltage Swing	R_L = 2.0kΩ, T_A = +25°C (LM2902 $R_L \geq 10k\Omega$)	0		$+V_S$ -1.5	0		$+V_S$ -1.5	0		$+V_S$ -1.5	V
Common Mode Rejection Ratio	T_A = +25°C	70	85		65	70		50	70		dB
Power Supply Rejection Ratio	T_A = +25°C	65	100		65	100		50	100		dB
Channel Separation[7]	f = 1.0kHz to 20kHz T_A = +25°C (Input Referred)		-120			-120			-120		dB
Output Current Source	V_{IN+} = 1.0V, V_{IN-} = 0V, $+V_S$ = 15V, T_A = +25°C	20	40		20	40		20	40		mA
Sink	V_{IN-} = 1.0V, V_{IN+} = 0V $+V_S$ = 15V, T_A = +25°C	10	20		10	20		10	20		mA
	V_{IN-} = 1.0V, V_{IN+} = 0V T_A = +25°C, V_O = 200mV	12	50		12	50					μA

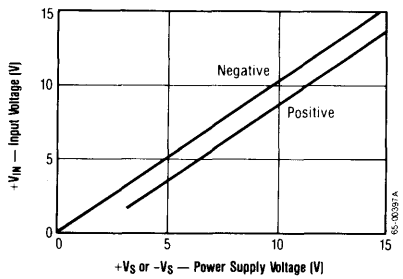
Notes:
1. Short circuits from the output to $+V_S$ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of $+V_S$. At values of supply voltage in excess of $+V_S$, continuous short circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
2. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the $+V_S$ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage again returns to a value greater than -0.3V.
3. These specifications apply for $+V_S$ = +5.0V and -55°C ≤ T_A ≤ +125°C, unless otherwise stated. With the LM224, all temperature specifications are limited to -25°C ≤ T_A ≤ +85°C; the LM324 temperature specifications are limited to 0°C ≤ T_A ≤ +70°C; and the LM2902 specifications are limited to -40°C ≤ T_A ≤ +85°C.
4. $V_O \cong$ 1.4V, R_S = 0Ω with $+V_S$ from 5.0V to 30V; and over the full common mode range (0V to $+V_S$ -1.5V).
5. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
6. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common mode voltage range is $+V_S$ -1.5V, but either or both inputs can go to +32V without damage (+26V for LM2902).
7. Due to proximity of external components, ensure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive increases at higher frequencies.

Electrical Characteristics ($+V_S = +5.0V$[3])

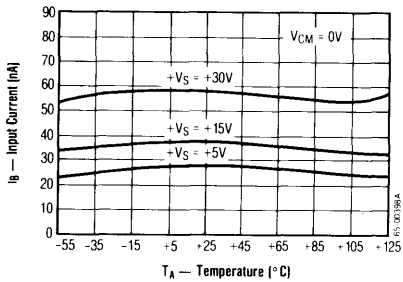
Parameters	Test Conditions	LM124/224			LM324			LM2902			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Short Circuit Current[1]	$T_A = +25°C$		40	60		40	60		40	60	mA
Input Offset Voltage[4]				±7.0			±9.0			±10	mV
Input Offset Voltage Drift	$R_S = 0\Omega$		7.0			7.0			7.0		μV/°C
Input Offset Current				±100			±150		45	±200	nA
Input Offset Current Drift			10			10			10		pA/°C
Input Bias Current			40	300		40	500		40	500	nA
Input Voltage Range[6]	$+V_S = +30V$	0		$+V_S$ -2.0	0		$+V_S$ -2.0	0		$+V_S$ -2.0	V
Large Signal Voltage Gain	$+V_S = +15V$ (For Large V_O Swing) $R_L \geq 2.0k\Omega$	25			15			15			V/mV
Output Voltage Swing V_{OH}	$+V_S = +30V$, $R_L = 2.0k\Omega$	26			26			22			V
V_{OH}	$R_L \geq 10k\Omega$	27	28		27	28		23	24		V
V_{OL}	$+V_S = +5.0V$, $R_L = 10k\Omega$		5.0	20		5.0	20		5.0	100	mV
Output Current Source	$V_{IN+} = +1.0V$, $V_{IN-} = 0V$, $+V_S = +15V$	10	20		10	20		10	20		mA
Sink	$V_{IN-} = +1.0V$, $V_{IN+} = 0V$, $+V_S = +15V$	5.0	8.0		5.0	8.0		5.0	8.0		mA
Differential Input[6] Voltage				$+V_S$			$+V_S$			$+V_S$	V

Typical Performance Characteristics (Continued)

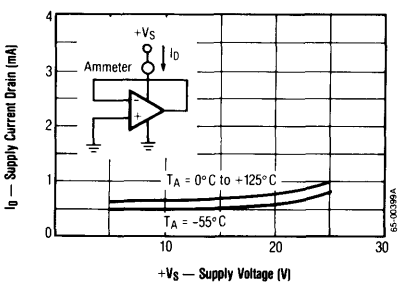
Input Voltage Range



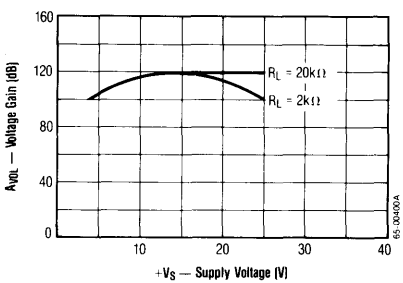
Input Current



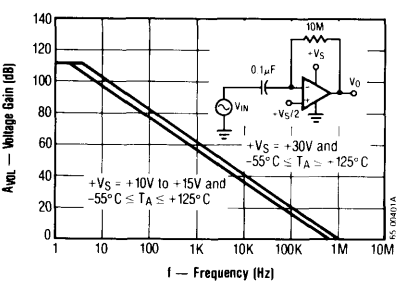
Supply Current



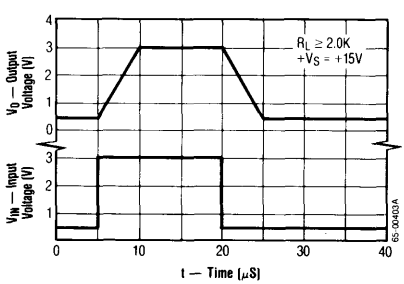
Voltage Gain



Open Loop Frequency Response

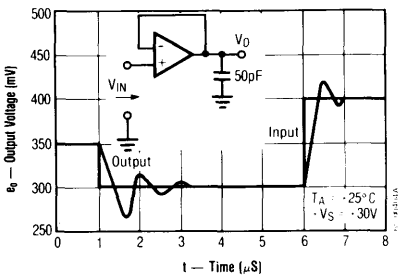


Voltage Follower Pulse Response

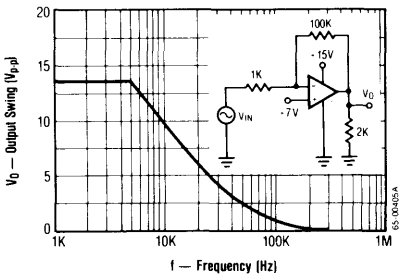


Typical Performance Characteristics

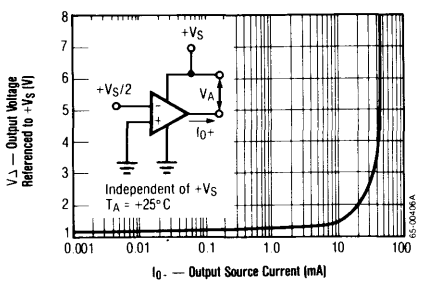
Voltage Follower Pulse Response (Small Signal)



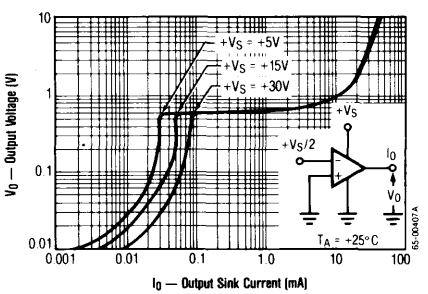
Large Signal Frequency Response



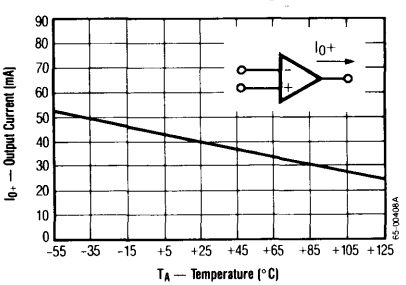
Output Characteristics Current Sourcing



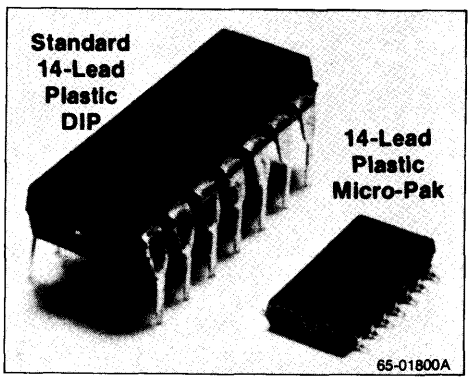
Output Characteristics Current Sinking



Current Limiting



Comparison of Standard
vs Micro-Package



Raytheon

Low Power Quad 741 Operational Amplifier

LM148/248/348

Features

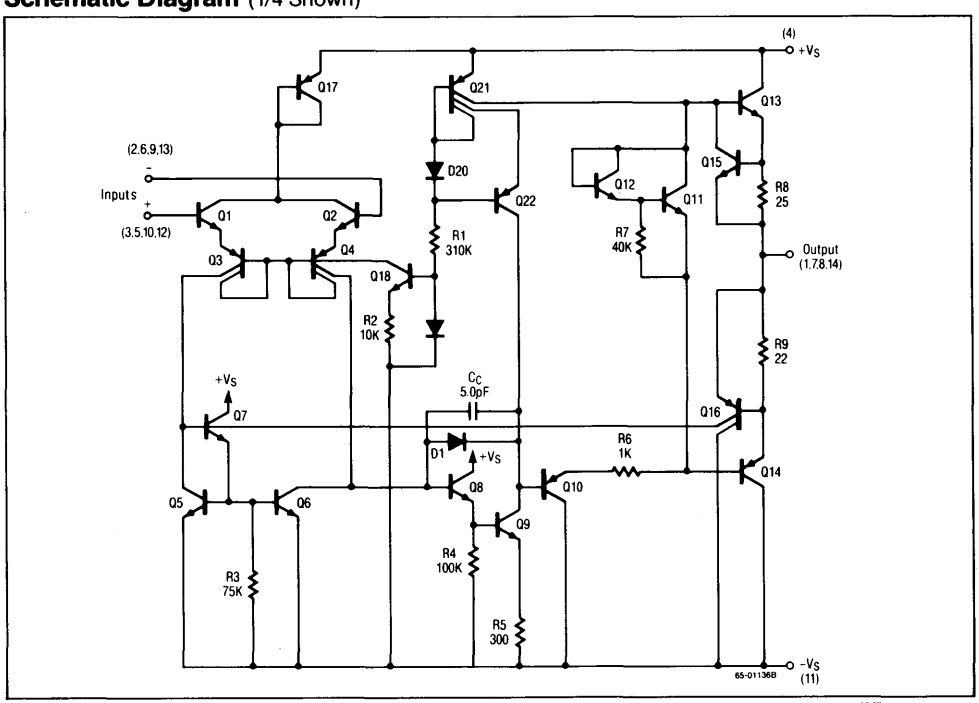
- 741 op amp operating characteristics
- Low supply current drain — 0.6mA/amplifier
- Class AB output stage — no crossover distortion
- Pin compatible with the LM124
- Low input offset voltage — 1.0mV
- Low input offset current — 4.0nA
- Low input bias current — 30nA
- Gain bandwidth product — LM148 (unity gain) 1.0MHz
- High degree of isolation between amplifiers — 120dB
- Overload protection for inputs and outputs

Description

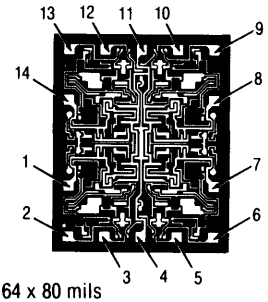
The LM148 series is a true quad 741. It consists of four independent high-gain, internally compensated, low-power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar 741 operational amplifier. In addition, the total supply current for all four amplifiers is comparable to the supply current of a single 741 type op amp. Other features include input offset currents and input bias currents which are much less than those of a standard 741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling.

The LM148 can be used anywhere multiple 741 or 1558 type amplifiers are being used and in applications where amplifier matching or high packing density is required.

Schematic Diagram (1/4 Shown)



Mask Pattern



Die Size: 64 x 80 mils
Min. Pad Dimension: 4 x 4 mils

Absolute Maximum Ratings

Supply Voltage
- LM148 ..... ±22V
- LM248/348 ..... ±18V

Differential Input Voltage
- LM148 ..... 44V
- LM248/348 ..... 36V

Input Voltage
- LM148 ..... ±22V
- LM248/348 ..... ±18V

Output Short Circuit Duration[1] ..... Indefinite

Storage Temperature Range ..... -65°C to +150°C

Operating Temperature Range
- LM148 ..... $-55°C \leq T_A \leq +125°C$
- LM248 ..... $-25°C \leq T_A \leq +85°C$
- LM348 ..... $0°C \leq T_A \leq +70°C$

Lead Soldering Temperature (60 Sec) ..... +300°C

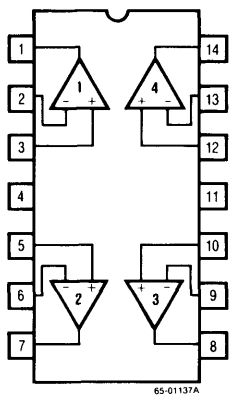
Notes: 1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Short circuit to ground on one amplifier only.

Thermal Characteristics

	14-Lead Plastic DIP	14-Lead Ceramic DIP
Max. Junction Temp.	125°C	175°C
Max. P_D $T_A < 50°C$	468mW	1042mW
Therm. Res. θ_{JC}	—	60°C/W
Therm. Res. θ_{JA}	160°C/W	120°C/W
For $T_A > 50°C$ Derate at	6.25mW per °C	8.33mW per °C

Connection Information

14-Lead
Dual In-Line Package
(Top View)



Pin	Function
1	Output A
2	$-V_{IN}$ A
3	$+V_{IN}$ A
4	$+V_S$
5	$+V_{IN}$ B
6	$-V_{IN}$ B
7	Output B
8	Output C
9	$-V_{IN}$ C
10	$+V_{IN}$ C
11	$-V_S$
12	$+V_{IN}$ D
13	$-V_{IN}$ D
14	Output D

Ordering Information

Part Number	Package	Operating Temperature Range
LM348J	Ceramic	0°C to +70°C
LM348N	Plastic	0°C to +70°C
LM248J	Ceramic	-25°C to +85°C
LM248N	Plastic	-25°C to +85°C
LM148J	Ceramic	-55°C to +125°C
LM148J/883B*	Ceramic	-55°C to +125°C

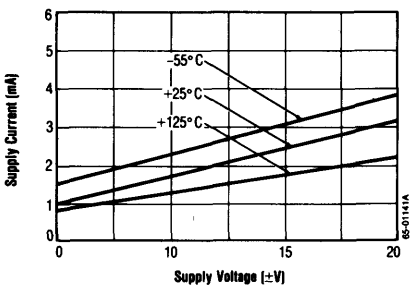
*MIL-STD-883, Level B Processing

Electrical Characteristics ($V_S = \pm 15V$ and over the absolute maximum operating temperature range ($T_L \leq T_A \leq T_H$) unless otherwise specified)

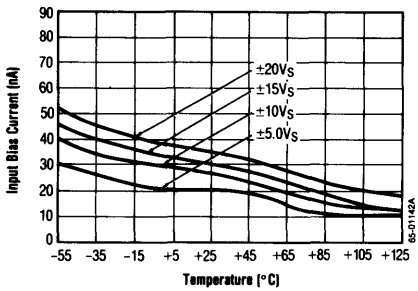
Parameters	Test Conditions	LM148			LM248			LM348			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = +25°C$, $R_S \leq 10k\Omega$		1.0	5.0		1.0	6.0		1.0	6.0	mV
Input Offset Current	$T_A = +25°C$		4.0	25		4.0	50		4.0	50	nA
Input Bias Current	$T_A = +25°C$		30	100		30	200		30	200	nA
Input Resistance (Differential Mode)	$T_A = +25°C$	0.8	2.5		0.8	2.5		0.8	2.5		MΩ
Supply Current All Amplifiers	$T_A = +25°C$, $V_S = \pm 15V$		2.4	3.6		2.4	4.5		2.4	4.5	mA
Large Signal Voltage Gain	$T_A = +25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$ $R_L \geq 2k\Omega$	50	160		25	160		25	160		V/mV
Channel Separation	$T_A = +25°C$, f = 1Hz to 20kHz		120			120			120		dB
Unity Gain Bandwidth	$T_A = +25°C$		1.0			1.0			1.0		MHz
Phase Margin	$T_A = +25°C$		60			60			60		Degrees
Slew Rate	$T_A = +25°C$		0.5			0.5			0.5		V/μS
Short Circuit Current	$T_A = +25°C$		25			25			25		mA
Input Offset Voltage	$R_S \leq 10k\Omega$			6.0			7.5			7.5	mV
Input Offset Current				75			125			100	nA
Input Bias Current				325			500			400	nA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L > 2k\Omega$	25			15			15			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k\Omega$	±12	±13		±12	±13		±12	±13		V
	$R_L = 2k\Omega$	±10	±12		±10	±12		±10	±12		V
Input Voltage Range	$V_S = \pm 15V$	±12			±12			±12			V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	90		70	90		70	90		dB
Power Supply Rejection Ratio	$R_S \leq 10k\Omega$	77	96		77	96		77	96		dB

Typical Performance Characteristics

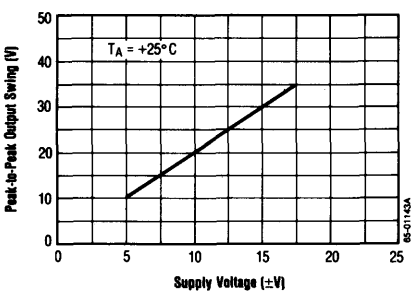
Supply Current vs. Supply Voltage



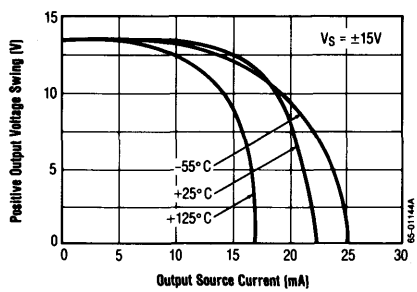
Input Bias Current vs. Temperature



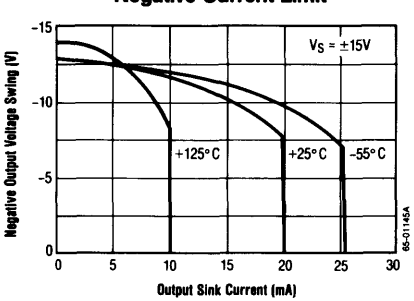
Voltage Swing vs. Supply Voltage



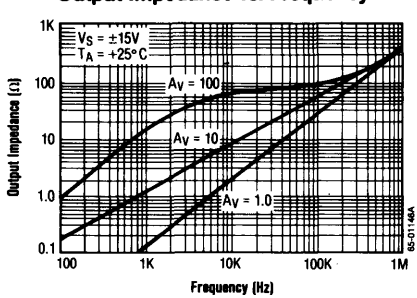
Positive Current Limit



Negative Current Limit

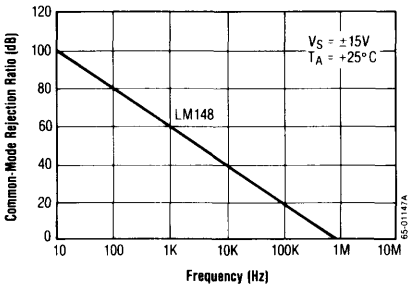


Output Impedance vs. Frequency

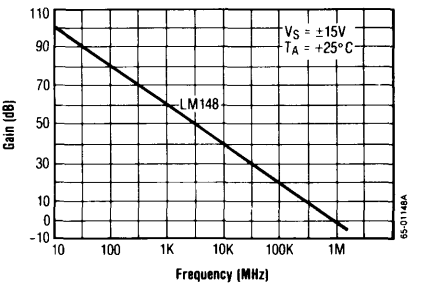


Typical Performance Characteristics (Continued)

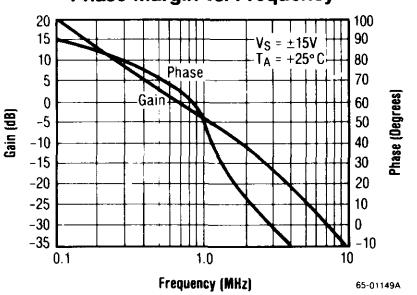
Common Mode Rejection Ratio vs. Frequency



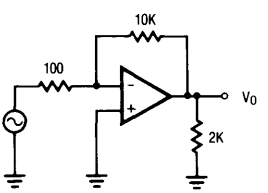
Open Loop Frequency Response



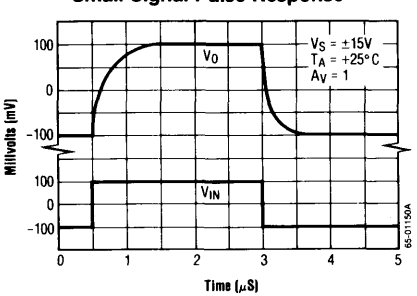
Phase Margin vs. Frequency



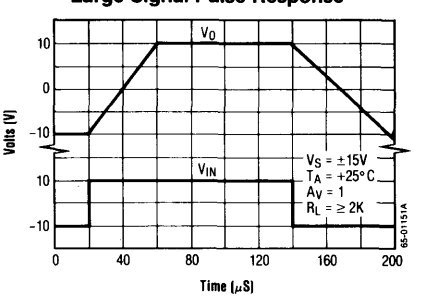
Test Circuit



Small Signal Pulse Response

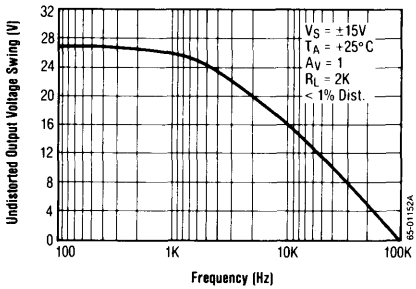


Large Signal Pulse Response

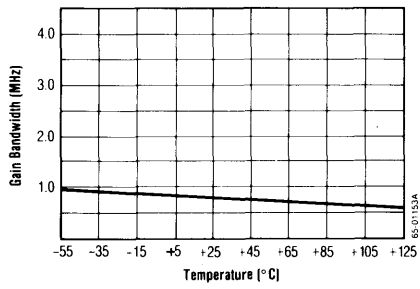


Typical Performance Characteristics (Continued)

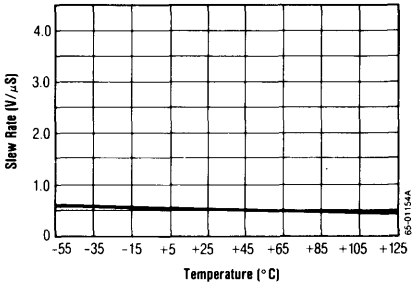
Undistorted Output Voltage Swing vs. Frequency



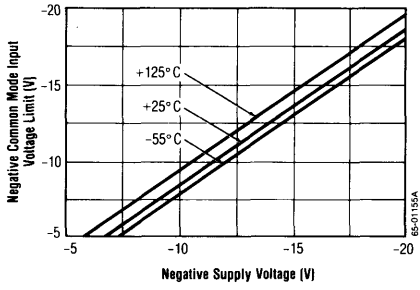
Gain Bandwidth vs. Temperature



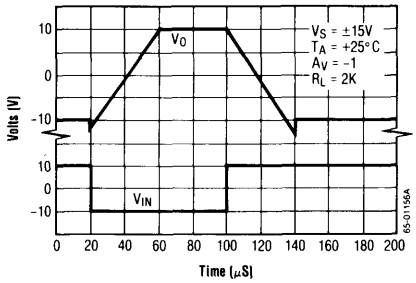
Slew Rate vs. Temperature



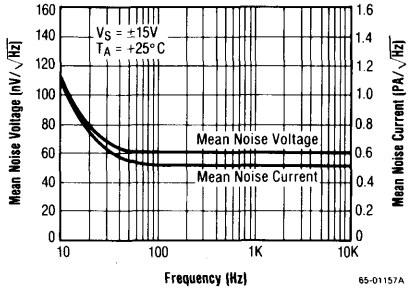
Negative Common Mode Input Voltage Limit



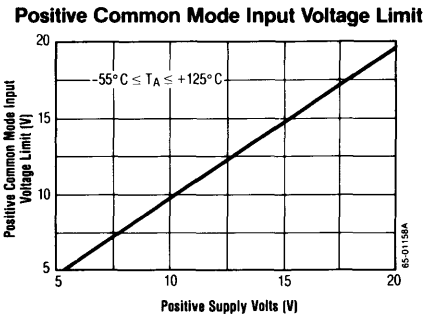
Inverting Large Signal Pulse Response



Input Noise Voltage and Noise Current



Typical Performance Characteristics (Continued)



Typical Simulation

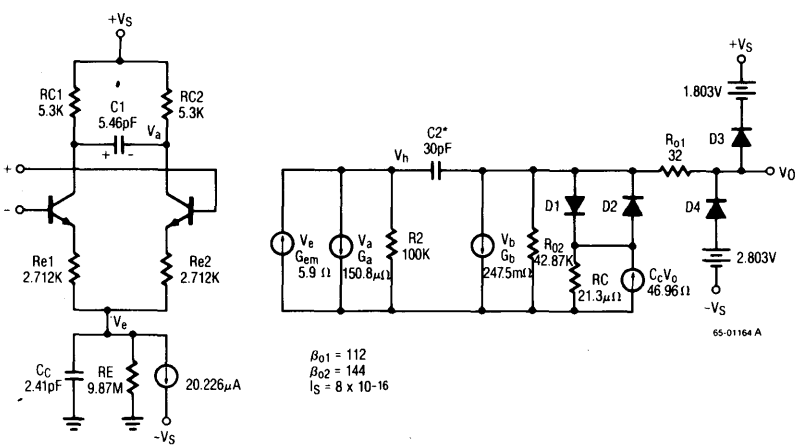


Figure 1. LM148 Macromodel for Computer Simulation

Typical Applications

The 148 series are low power quad operational amplifiers that exhibit performance comparable to the popular 741. Substitution can therefore be made with no change in circuit behavior.

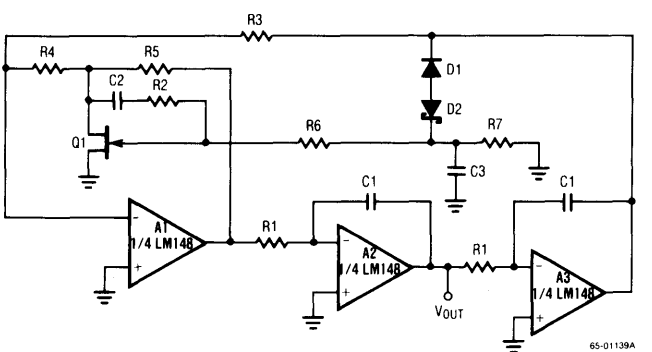
The input characteristics of these devices allow differential voltages which exceed the supplies. Output phase will be correct as long as one of the inputs are within the operating common mode range. If both exceed the negative limit, the output will latch positive. Current limiting resistors should be used on the inputs in case voltages become excessive.

When capacitive loading becomes much greater than 100pF, a resistor should be placed between the output and feedback connection in order to reduce phase shift.

The 148 series is short circuit protected to either ground or the supplies continuously when only one of the four amplifiers are shorted. If multiple shorts occur simultaneously, the unit can be destroyed due to excessive power dissipation.

To assure stability and to minimize pickup, feedback resistors should be placed close to the input to maximize the feedback pole frequency (a function of input to ground capacitance). A good rule of thumb is that the feedback pole frequency should be 6 times the operating -3.0dB frequency. If less, a lead capacitor should be placed between the output and input.

Typical Applications

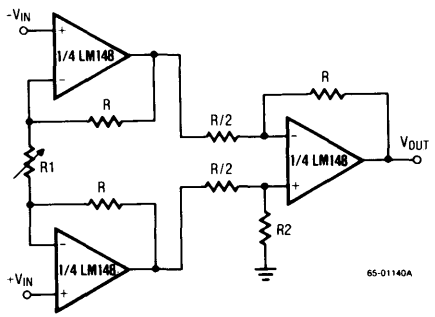


$$f = \frac{1}{2\pi R1C1} \times \sqrt{K},\ K = \frac{R4R5}{R3}\left(\frac{1}{r_{DS}} + \frac{1}{R4} + \frac{1}{R5}\right),\ r_{DS} \cong \frac{R_{ON}}{\left(1 - \frac{V_{GS}}{V_P}\right)}\ 1/2$$

f_{MAX} = 5.0kHz, THD ≤ 0.03%
R1 = 100K pot., C1 = 0.0047μF, C2 = 0.01μF, C3 = 0.1μF, R2 = R6 = R7 = 1M, R3 = 5.1K, R4 = 12Ω, R5 = 240Ω, Q1 = NS5102, D1 = 1N914, D2 = 3.6V avalanche diode (ex. LM103), V_S = ±15V
A simpler version with some distortion degradation at high frequencies can be made by using A1 as a simple inverting amplifier, and by putting back to back zeners in the feedback loop of A3.

Figure 2. One Decade Low Distortion Sinewave Generator

Typical Applications (Continued)

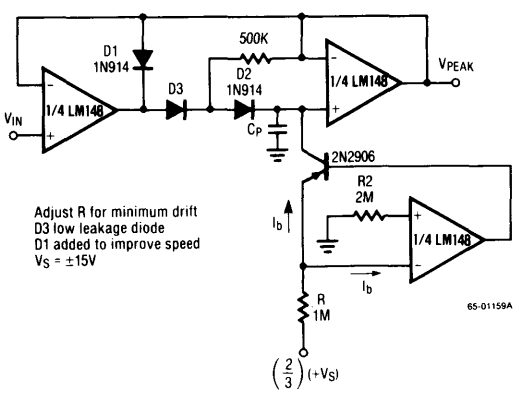


$V_{OUT} = 2\left(\frac{2R}{R1} + 1\right)$, $-V_S - 3V \leq V_{IN\,CM} \leq +V_S - 3V$.

$V_S = \pm 15V$

R = R2, trim R2 to boost CMRR

Figure 3. Low Cost Instrumentation Amplifier



Adjust R for minimum drift
D3 low leakage diode
D1 added to improve speed
$V_S = \pm 15V$

Figure 4. Low Voltage Peak Detector With Bias Current Compensation

Typical Applications (Continued)

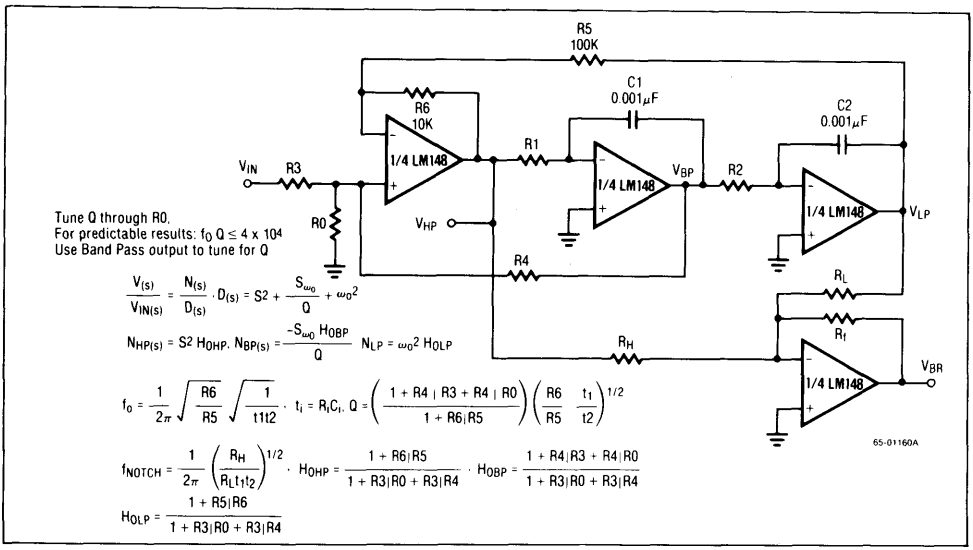


Figure 5. Universal State-Space Filter

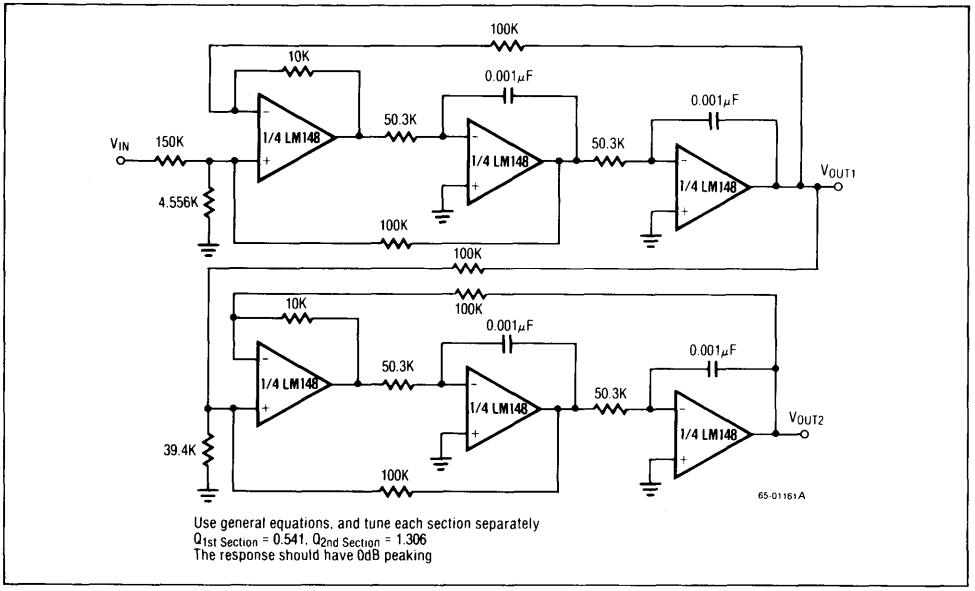
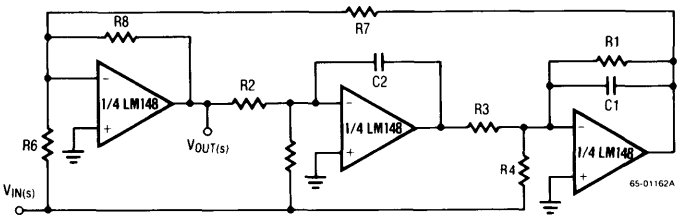


Figure 6. 1kHz 4 Pole Butterworth Filter

Typical Applications (Continued)



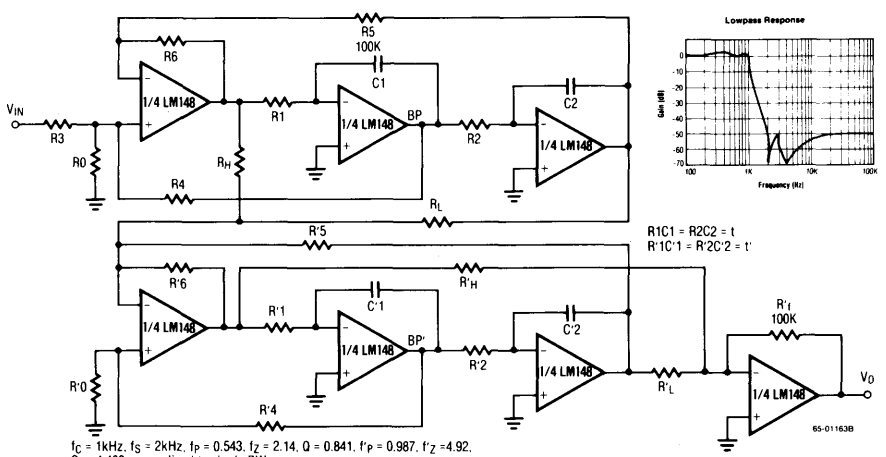
$$Q = \sqrt{\frac{R8}{R7}} \times \frac{R1C1}{\sqrt{R3C2R2C1}}, \quad f_o = \frac{1}{2\pi}\sqrt{\frac{R8}{R7}} \times \frac{1}{\sqrt{R2R3C1C2}}, \quad f_{NOTCH} = \frac{1}{2\pi}\sqrt{\frac{R6}{R3R5R7C1C2}}$$

Necessary condition for notch: $\frac{1}{R6} = \frac{R1}{R4R7}$

Ex: f_{NOTCH} = 3kHz, Q = 5, R1 = 270K, R2 = R3 =20K, R4 = 27K, R5 = 20K, R6 = R8 = 10K, R7 = 100K.
C1 = C2 = 0.001μF

Better noise performance than the state-space approach

Figure 7. 3 Amplifier Bi-Quad Notch Filter



f_C = 1kHz, f_S = 2kHz, f_P = 0.543, f_Z = 2.14, Q = 0.841, f'_P = 0.987, f'_Z =4.92,
Q' = 4.403, normalized to ripple BW

$$f_P = \frac{1}{2\pi}\sqrt{\frac{R6}{R5}} \times \frac{1}{t}, \quad f_Z = \frac{1}{2\pi}\sqrt{\frac{R_H}{R_L}} \times \frac{1}{t}, \quad Q = \frac{1 + R4|R3 + R4|R0}{1 + R6|R5} \times \sqrt{\frac{R6}{R5}}, \quad Q' = \sqrt{\frac{R'6}{R'5}} \cdot \frac{1 + R'4|R'0}{1 + R'6|R'5 + R'6|R_P}$$

$$R_P = \frac{R_H R_L}{R_H + R_L}$$

Use the BP outputs to tune Q, Q', tune the 2 sections separately

R1 = R2 = 92.6K, R3 = R4 = R5 = 100K, R6 = 10K, R0 = 107.8K, R_L = 100K, R_H =155.1K,
R'1 = R'2 = 50.9K, R'4 = R'5 = 100K, R'6 = 10K, R'0 = 5.78K, R'_L = 100K, R'_H = 248.12K, R'_f = 100K.

All capacitors are 0.001μF

Figure 8. 4th Order 1 kHz Elliptic Filter (4 Poles, 4 Zeros)

Raytheon

Low Power Dual Operational Amplifier

LM358

Features

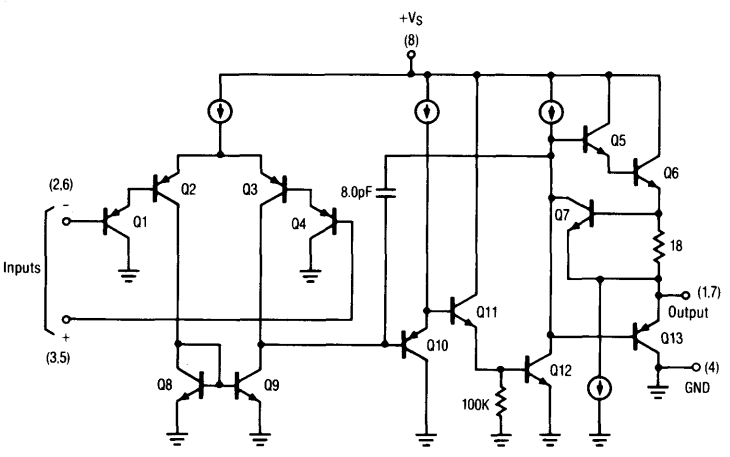
- Internally frequency compensated for unity gain
- Large DC voltage gain — 100dB
- Wide bandwidth (unity gain, temperature compensated) — 1MHz
- Wide power supply range
  Single supply — +3V to +30V
  or dual supplies — ±1.5V to ±15V
- Very low supply current drain — 500μA
  Essentially independent of supply voltage — 1mW/Op Amp at +5V
- Low input biasing current (temperature compensated) — 45nA
- Low input offset voltage — 2mV
- Low offset current — 5nA
- Input common mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing — 0V to $+V_S$ -1.5V

Description

The LM358 consists of two independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks, and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM358 can be directly operated off of the standard +5V power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15V power supplies.

Schematic Diagram (1/2 Shown)



Absolute Maximum Ratings

Supply Voltage ..... +32V or ±16V
Differential Input Voltage 32V
Input Voltage ..... -0.3V to +32V
Output Short Circuit to Ground
(One Amplifier)[1]
$V_S \leq +15V$ and $T_A = +25°C$ ..... Continuous
Input Current ($V_{IN} < -0.3V_{OL}$)[2] 50mA
Operating Temperature
Range ..... -20°C to +75°C
Lead Soldering Temperature (10 Sec)
LM358NB ..... +300°C
LM358M ..... +260°C

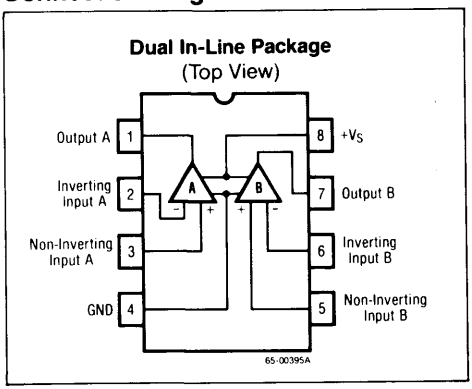
Thermal Characteristics

	8-Lead Micro-Pak Plastic DIP	8-Lead Plastic DIP
Max. Junction Temp	125°C	125°C
Max. P_D $T_A < 50°C$	300mW	468mW
Therm. Res. θ_{JC}	—	—
Therm. Res. θ_{JA}	240°C/W	160°C/W
For $T_A > 50°C$ Derate at	4.17mW per °C	6.25mW per °C

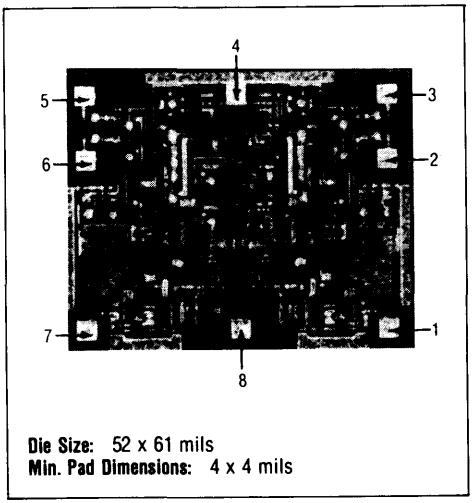
Ordering Information

Part Number	Package	Operating Temperature Range
LM358M	Micro-Plastic	-20°C to +75°C
LM358NB	Plastic	-20°C to +75°C

Connection Diagram



Mask Pattern



Die Size: 52 x 61 mils
Min. Pad Dimensions: 4 x 4 mils

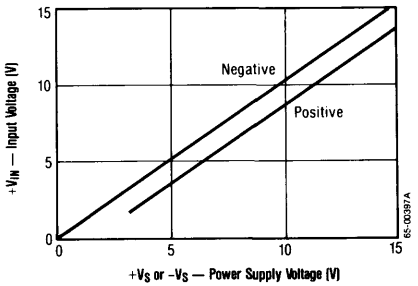
Electrical Characteristics ($+V_S$ = +5.0V, T_A = +25°C)

Parameters	Test Conditions	Min	Typ	Max	Units
Input Offset Voltage	(Note 3)		±2.0	±7.0	mV
Input Bias Current	(Note 4)		45	250	nA
Input Offset Current			±5.0	±50	nA
Input Voltage Range	$+V_S$ = +30V (Note 5)	0		V_S -1.5	V
Supply Current	$R_L = \infty$, $+V_S$ = +30V		1.0	2.0	mA
	$R_L = \infty$ On All Op Amps		0.7	1.2	
Large Signal Voltage Gain	$+V_S$ = +15V (For Large V_O Swing) $R_L \geq 2k\Omega$	25	100		V/mV
Output Voltage Swing	$R_L = 2k\Omega$	0		V_S -1.5	V
Common Mode Rejection Ratio		65	70		dB
Power Supply Rejection Ratio		65	100		dB
Channel Separation	f = 1kHz to 20kHz (Input Referred) (Note 6)		-120		dB
Output Source Current	V_{IN+} = 1V, V_{IN-} = 0V, $+V_S$ = +15V	20	40		mA
Output Sink Current	V_{IN-} = 1V, V_{IN+} = 0V, $+V_S$ = +15V	10	20		mA
Output Sink Current	V_{IN-} = 1V, V_{IN+} = 0V, V_O = 200mW	12	50		μA
Short Circuit Current	(Note 1)		40	60	mA
The following specifications apply for $+V_S$ = +5.0V, 0°C to +70°C					
Input Offset Voltage	(Note 3)			±9.0	mV
Average Input Offset Voltage Drift	$R_S = 0\Omega$		7.0		μV/°C
Input Offset Current				±150	nA
Average Input Offset Current Drift			10		pA/°C
Input Bias Current			40	500	nA
Input Voltage Range	$+V_S$ = +30V (Note 5)	0		$+V_S$ -2.0	V

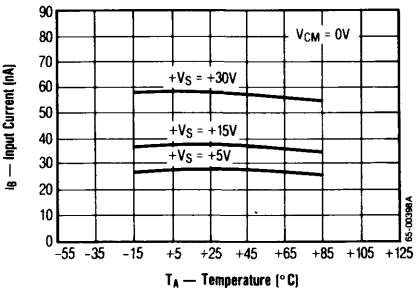
Notes:
1. Short circuits from the output to $+V_S$ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of $+V_S$. At values of supply voltage in excess of +15V, continuous short circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
2. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the $+V_S$ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3V
3. $V_O \cong 1.4V$, $R_S = 0\Omega$ with $+V_S$ from +5V to +30V; and over the full input common mode range (0V to $+V_S$ -1.5V).
4. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
5. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than +0.3V. The upper end of the common mode voltage range is $+V_S$ -1.5V, but either or both inputs can go to +32V without damage.
6. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive coupling increases at higher frequencies.

Typical Performance Characteristics

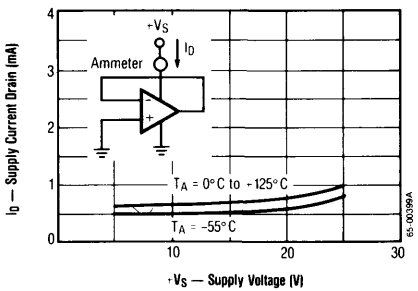
Input Voltage Range vs. Supply Voltage



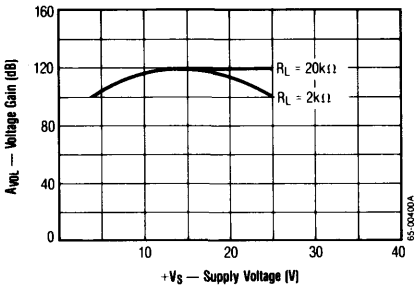
Input Current vs. Temperature



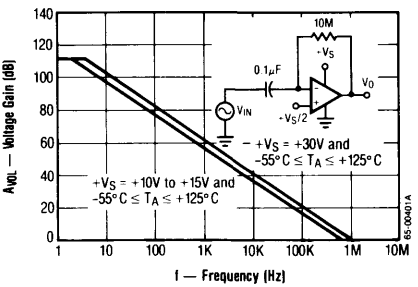
Supply Current vs. Supply Voltage



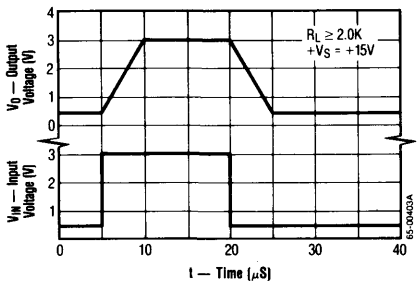
Voltage Gain vs. Supply Voltage



Open Loop Frequency Response

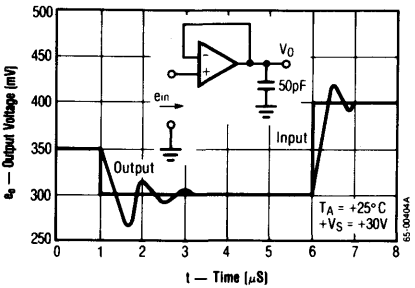


Voltage Follower Pulse Response

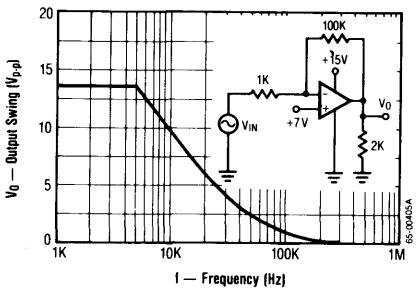


Typical Performance Characteristics (Continued)

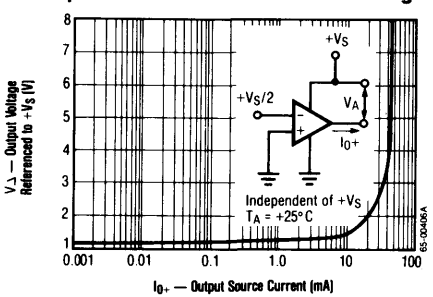
Voltage Follower Pulse Response (Small Signal)



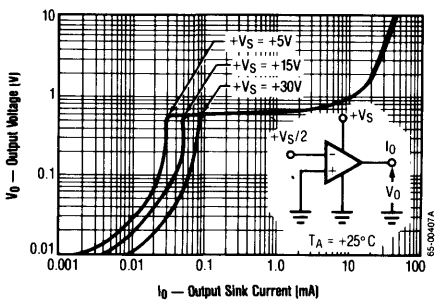
Large Signal Frequency Response



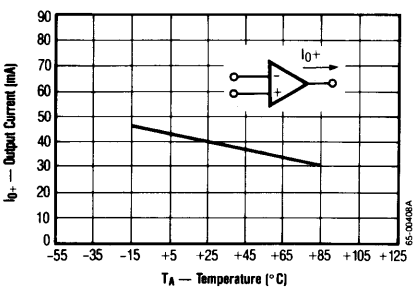
Output Characteristics Current Sourcing



Output Characteristics Current Sinking



Current Limiting vs. Temperature



Raytheon

Current Mode Single-Supply Quad Operational Amplifier

LM2900/3900

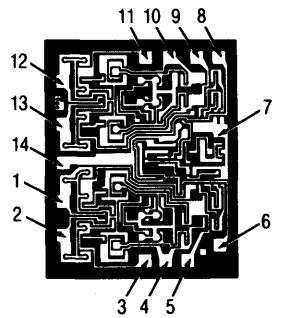
Features

- Wide single supply voltage range — 4.0V to 36V
- Supply current drain independent of supply voltage
- Low input biasing current — 30nA
- High open-loop gain — 70dB
- Wide bandwidth — 2.5MHz (unity gain)
- Larger gain-bandwidth product in non-inverting mode (A_V = 100 at f = 1.0MHz)
- Large output voltage swing (V_S -1.0)V_{p-p}
- Internally frequency compensated for unity gain
- Output short-circuit protection

Description

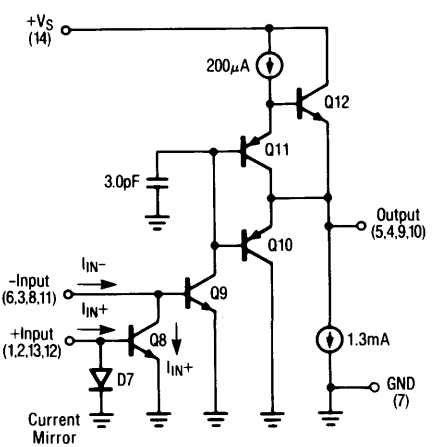
The LM2900 and LM3900 consist of four independent, dual input, internally compensated amplifiers which were designed specifically to operate off a single power supply voltage and to provide a large output voltage swing. These amplifiers make use of a current mirror to achieve the non-inverting input function. Application areas include: AC amplifiers, RC active filters, low frequency triangle, squarewave and pulse waveform generation circuits, tachometers and low speed, high voltage digital logic gates.

Mask Pattern



Die Size: 56 x 70 mils
Min. Pad Dimension: 4 x 4 mils

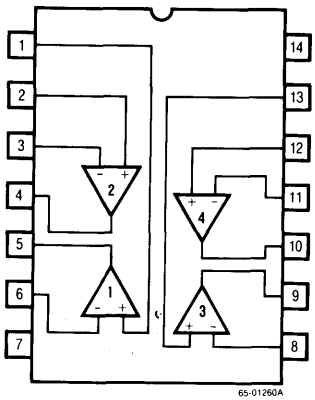
Schematic Diagram (1/4 Shown)



Current Mode Single-Supply Quad Operational Amplifier

Connection Information

14-Lead
Dual In-Line Package
(Top View)



65-01260A

Pin	Function
1	+Input 1
2	+Input 2
3	-Input 2
4	Output 2
5	Output 1
6	-Input 1
7	Ground
8	-Input 3
9	Output 3
10	Output 4
11	-Input 4
12	+Input 4
13	+Input 3
14	$+V_S$

Absolute Maximum Ratings

Supply Voltage
LM2900 ..... ±36V
LM3900 ..... ±32V
Supply Voltage ..... ±18V
Input Currents, $I_{IN\pm}$ or I_{IN-} 20mA
Output Short Circuit Duration .... Continuous
One Amplifier, T_A = +25°C
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
LM2900 ..... -40°C to +85°C
LM3900 ..... 0°C to +70°C
Lead Soldering Temperature
(10 Sec) ..... +300°C

Thermal Characteristics

	14-Lead Plastic DIP
Max. Junc. Temp.	125°C
Max. P_D T_A < 50°C	468mW
Therm. Res. θ_{JC}	—
Therm. Res. θ_{JA}	160°C/W
For T_A > 50°C Derate at	6.25mW per °C

Ordering Information

Part Number	Package	Operating Temperature Range
LM3900N	Plastic	0°C to +70°C
LM2900N	Plastic	-40°C to +85°C

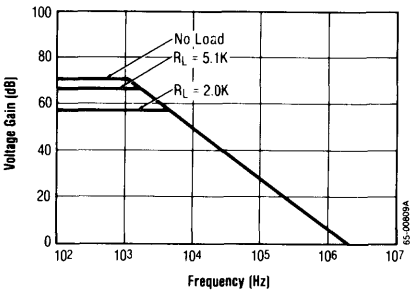
Electrical Characteristics (V_S = +15V and T_A = +25°C unless otherwise noted)

Parameter	Test Conditions	LM2900/3900 Min	LM2900/3900 Typ	LM2900/3900 Max	Units
Large Signal Voltage Gain	f = 100Hz	1200	2800		V/V
Input Resistance (Differential Mode)	Inverting Input		1.0		MΩ
Output Resistance			8.0		kΩ
Unity Gain Bandwidth[1]	Inverting Input		2.5		MHz
Input Bias Current	Inverting Input		30	200	nA
Slew Rate	Positive Output Swing		0.5		V/μS
	Negative Output Swing		20		
Supply Current	R_L = ∞ On All Amplifiers		6.2	10	mA
Output Voltage Swing V_{OUT} High	R_L = 2k, I_{IN-} = 0, I_{IN+} = 0	13.5	14.2		V
V_{OUT} Low	I_{IN-} = 10μA, I_{IN+} = 0		0.09	0.2	V
Output Current	Source	6.0	18		mA
	Sink[2]	0.5	1.3		
Power Supply Rejection Ratio	f = 100Hz		70		dB
Mirror Gain[3]	I_{IN+} = 200μA	0.90	1.0	1.1	μA/μA
Mirror Current[4]			10	500	μA
Negative Input Current[5]			1.0		mA

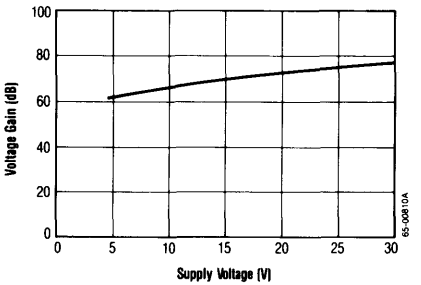
Notes:
1. When used as a "non-inverting amplifier", the gain-bandwidth product is not limited to 2.5MHz. The isolation provided by the "current mirror" allows a constant unity voltage gain feedback for the main inverting amplifier. This means that large values of gain can be achieved at high frequencies and the dominant limit is due to the slew rate of the amplifier. For example: a voltage gain of 100 is easily obtained at 1MHz and an output voltage swing of 160mV_{p-p} can be achieved prior to slew rate limiting. This operational mode is useful for signal frequencies in the 50kHz to 1MHz range as would be encountered in IF or carrier frequency applications.
2. The output current sink capability can be increased for large signal conditions by overdriving the inverting input.
3. This spec indicates the current gain of the current mirror which is used as the non-inverting input.
4. Input V_{BE} match between the non-inverting and the inverting inputs occurs for a mirror-current (non-inverting input current) of approximately 10μA. This is therefore a typical design center for many of the application circuits.
5. Clamp transistors are included on the IC to prevent the input voltages from swinging below ground more than approximately -0.3V. The negative input currents which may result from large signal overdrive with capacitance input coupling need to be externally limited to values of approximately 1.0mA. Negative input currents in excess of 4.0mA will cause the output voltage to drop to a low voltage. This maximum current applies to any one of the input terminals. If more than one of the input terminals are simultaneously driven, negative smaller maximum currents are allowed. Common mode current biasing can be used to prevent negative input voltages; for example, see the "Differentiator Circuit" in the applications section.

Typical Performance Characteristics

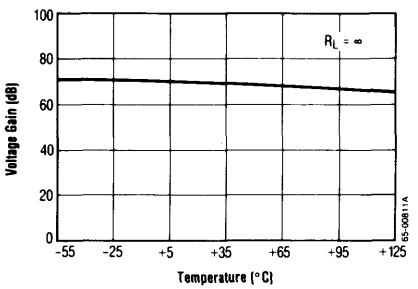
Open Loop Gain



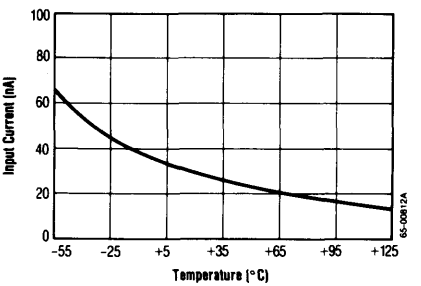
Voltage Gain vs. Supply Voltage



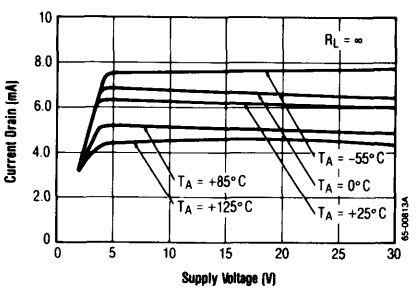
Voltage Gain vs. Temperature



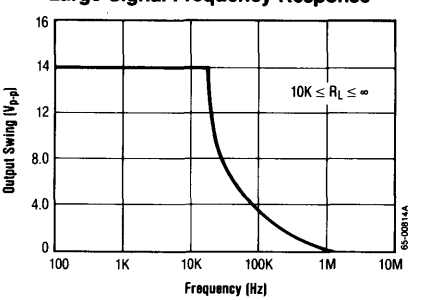
Input Current vs. Temperature



Supply Current

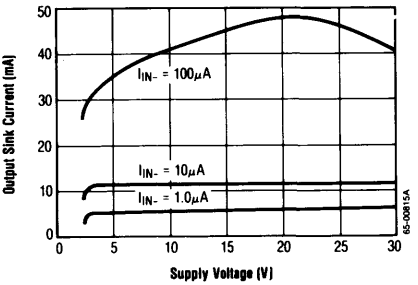


Large Signal Frequency Response

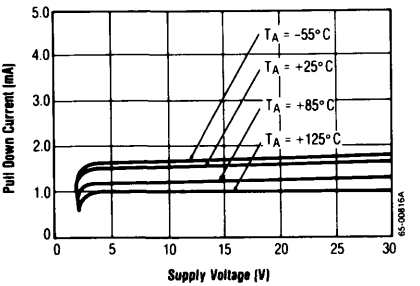


Typical Performance Characteristics (Continued)

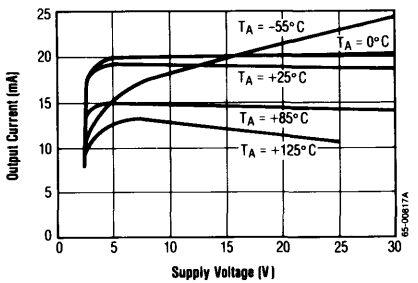
Output Sink Current vs. Supply Voltage



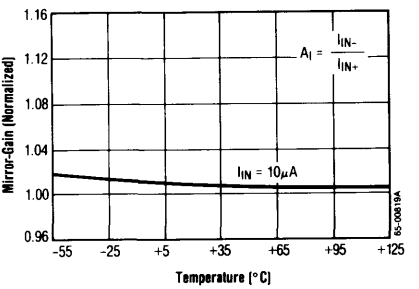
Output Class A Bias Current



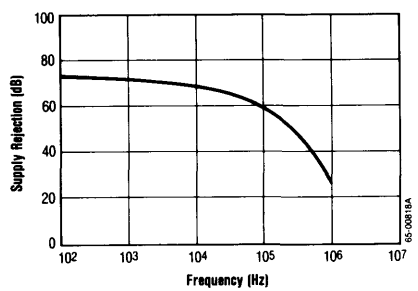
Output Source Current



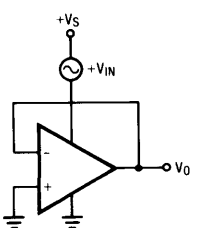
Mirror Gain vs. Temperature



Supply Rejection vs. Frequency

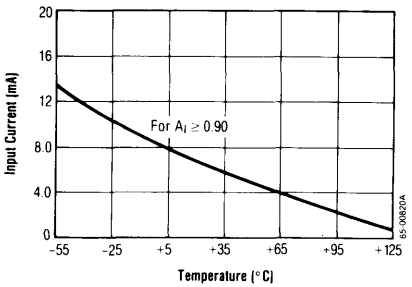


Test Circuit for Supply Rejection



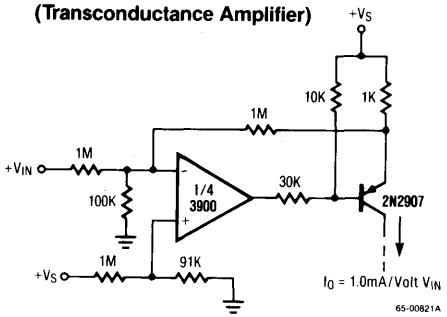
Typical Performance Characteristics (Continued)

Maximum Mirror Current

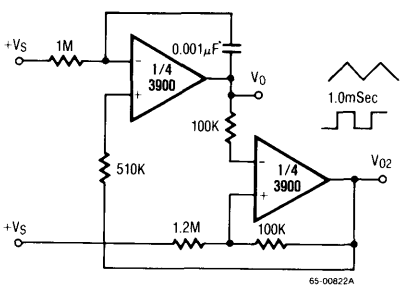


3900 Typical Applications (V_S = +15V)

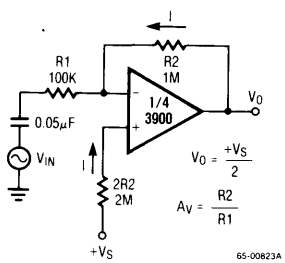
Voltage-Controlled Current Source (Transconductance Amplifier)



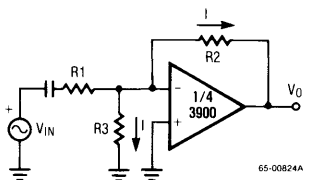
Triangle/Square Generator



Inverting Amplifier



V_{BE} Biasing



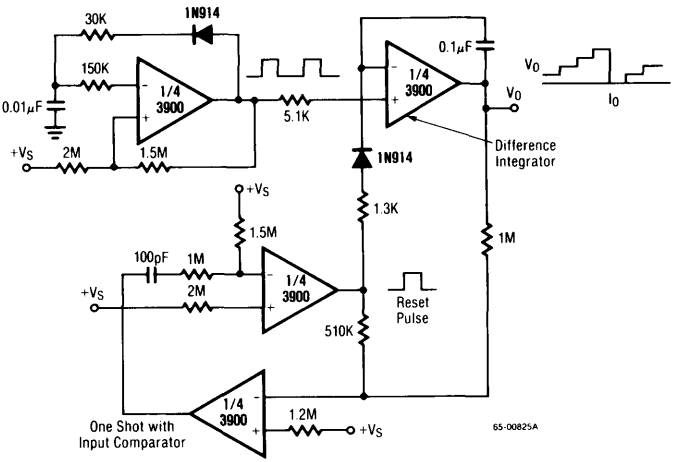
V_{BE} = 0.5V

$$V_O = V_{BE}\left(1 + \frac{R2}{R3}\right)$$

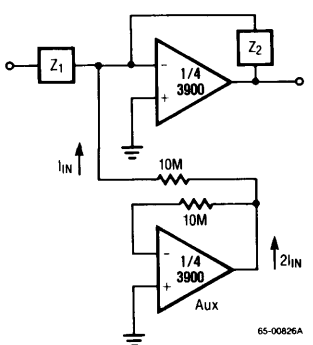
$$A_V = \frac{-R2}{R1}$$

3900 Typical Applications (Continued)

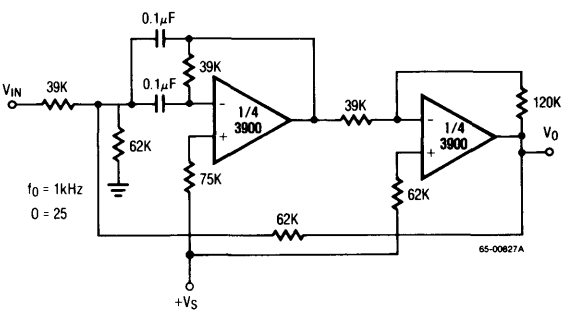
Free-Running Staircase Generator/Pulse Counter



Supplying I_{IN} With Auxiliary Amplifier (to Allow High Z Feedback Networks)

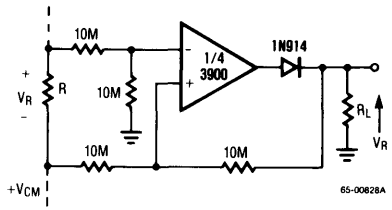


Bandpass Active Filter

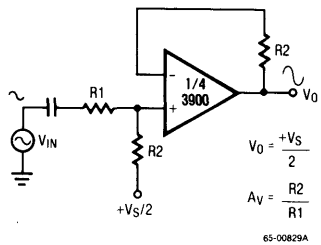


3900 Typical Applications (Continued)

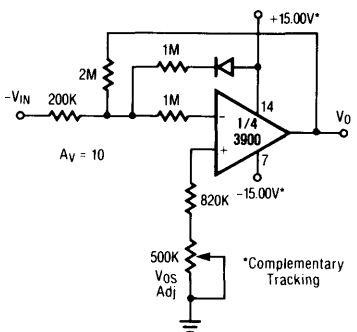
Ground Referencing a Differential Input Signal



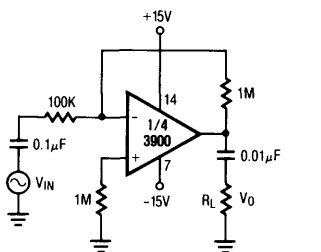
Non-Inverting Amplifier



Split Supply ($+V_S$ = +15V and $-V_S$ = -15V)



Non-Inverting DC Gain



AC Amplifier

65-00830A

Raytheon

Instrumentation Grade Operational Amplifier

OP-05 Series

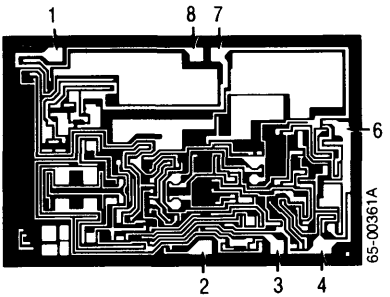
Features

- Low noise 0.1Hz to 10Hz — 0.35μV_{p-p}
- Low V_{OS} — 0.15mV
- Ultra-low V_{OS} drift — 0.2μV/°C
- Fits 725, 108A, 741, and AD510 sockets
- Long term stability — 0.2μV/Month
- Low input bias current — ±1nA
- High CMRR — 126dB
- Wide input voltage range — ±14V

Description

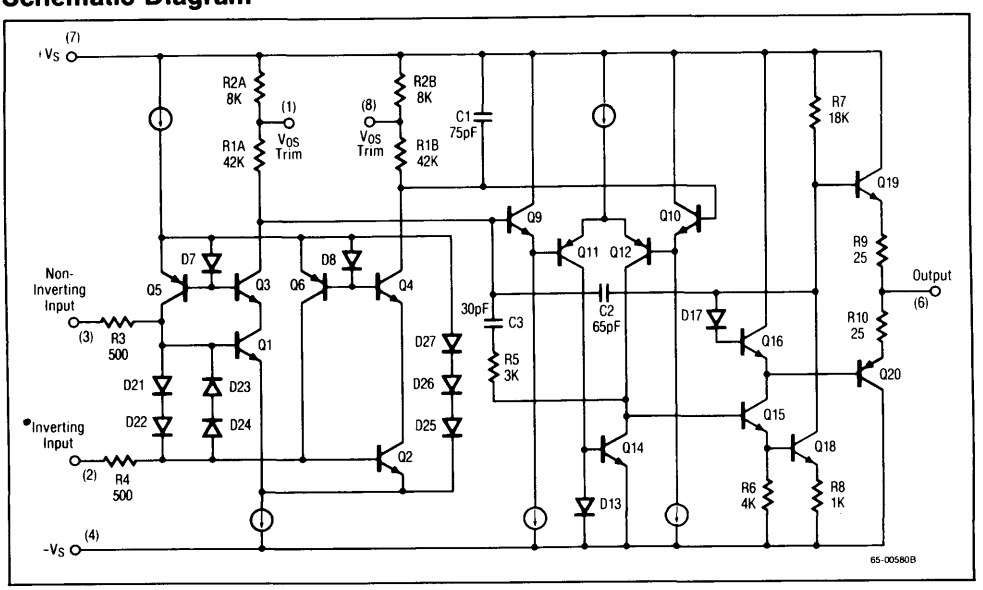
The OP-05 series of instrumentation grade operational amplifiers is designed for low level signal conditioning where ultra low V_{OS} and TCV_{OS} are required along with very low bias currents. Internal compensation eliminates the need for external components. Novel circuit design and tight process controls are used to obtain very low values of V_{OS}. Low frequency noise is minimized. Internal biasing techniques reduce external bias and offset currents to values in the order of ±1nA over the military temperature range. Raytheon's OP-05s are direct replacements for the 108A, 714, 725 and 5507. They can replace chopper stabilized amplifiers in many applications.

Mask Pattern



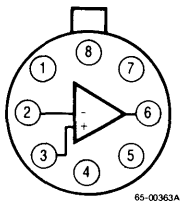
Die Size: 65 x 101 mils
Min. Pad Dimensions: 4 x 4 mils

Schematic Diagram

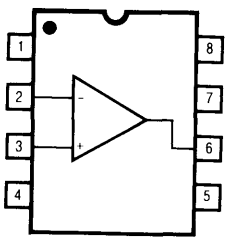


Connection Information

TO-99
Metal Can
(Top View)



8-Lead
Dual In-Line Package
(Top View)



Pin	Function
1	V_{OS} Trim
2	-Input
3	+Input
4	$-V_S$ (Case)
6	Output
7	$+V_S$
8	V_{OS} Trim

Absolute Maximum Ratings

Supply Voltage ..... ±22V
Input Voltage[1] ..... ±22V
Differential Input Voltage 30V
Internal Power Dissipation[2] 500mW
Output Short Circuit Duration ..... Indefinite
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
OP-05A ..... -55°C to +125°C
OP-05E/C/D ..... 0°C to +70°C
Lead Soldering Temperature
(60 Sec) ..... +300°C

Notes:
1. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
2. Maximum power dissipation vs. ambient temperature.

Thermal Characteristics

	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can
Max. Junction Temp.	175°C	175°C
Max. P_D $T_A < 50°C$	833mW	658mW
Therm. Res. θ_{JC}	45°C/W	50°C/W
Therm. Res. θ_{JA}	150°C/W	190°C/W
For $T_A > 50°C$ Derate at	8.33mW per °C	5.26mW per °C

Ordering Information

Part Number	Package	Operating Temperature Range
OP-05CT	TO-99	0°C to +70°C
OP-05ET	TO-99	0°C to +70°C
OP-05CDE	Ceramic	0°C to +70°C
OP-05EDE	Ceramic	0°C to +70°C
OP-05CNB	Plastic	0°C to +70°C
OP-05ENB	Plastic	0°C to +70°C
OP-05T	TO-99	-55°C to +125°C
OP-05T/883B*	TO-99	-55°C to +125°C
OP-05AT	TO-99	-55°C to +125°C
OP-05AT/883B*	TO-99	-55°C to +125°C
OP-05DE	Ceramic	-55°C to +125°C
OP-05DE/883B*	Ceramic	-55°C to +125°C
OP-05ADE	Ceramic	-55°C to +125°C
OP-05ADE/883B*	Ceramic	-55°C to +125°C

*MIL-STD-883, Level B Processing

Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	OP-05A			OP-05			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[4]			70	150		200	500	μV
Long Term Input Offset Voltage Stability[1,2]			0.2	1.0		0.2	1.0	μV/Mo
Input Offset Current			0.3	2.0		0.4	2.8	nA
Input Bias Current			±0.7	±2		±1	±3	nA
Input Noise Voltage[2]	0.1Hz to 10Hz		0.35	0.6		0.35	0.6	μV_{p-p}
Input Noise Voltage Density[2]	f_0 = 10Hz		10.3	18		10.3	18	$\frac{nV}{\sqrt{Hz}}$
	f_0 = 100Hz		10	13		10	13	
	f_0 = 1000Hz		9.6	11		9.6	11	
Input Noise Current[2]	0.1Hz to 10Hz		14	30		14	30	pA_{p-p}
Input Noise Current Density[2]	f_0 = 10Hz		0.32	0.80		0.32	0.80	$\frac{pA}{\sqrt{Hz}}$
	f_0 = 100Hz		0.14	0.23		0.14	0.23	
	f_0 = 1000Hz		1.12	0.17		0.12	0.17	
Input Resistance (Diff. Mode)[3]		30	80		20	60		MΩ
Input Resistance (Com. Mode)			200			200		GΩ
Input Voltage Range		±13.5	±14		±13.5	±14		V
Common Mode Rejection Ratio	V_{CM} = ±13.5V	114	126		114	126		dB
Power Supply Rejection Ratio	V_S = ±3V to ±18V	100	110		100	110		dB
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_O = ±10V	300	500		200	500		V/mV
Large Signal Voltage Gain[3]	$R_L \geq 500k\Omega$, V_O = ±0.5V, V_S = ±3V	150	500		150	500		
Output Voltage Swing	$R_L \geq 10k\Omega$	±12.5	±13		±12.5	±13		V
	$R_L \geq 2k\Omega$	±12	±12.8		±12	±12.8		
	$R_L \geq 1k\Omega$	±10.5	±12		±10.5	±12		
Slew Rate[2]	$R_L \geq 2k\Omega$	0.1	0.17		0.1	0.17		V/μS
Unity Gain Bandwidth[2]			0.5			0.5		MHz
Open Loop Output Resistance	V_O = 0, I_O = 0		60			60		Ω
Power Consumption	V_S = ±15V		75	120		75	120	mW
	V_S = ±3V		4	6		4	6	
Offset Adjustment Range	R_p = 20kΩ		±4			±4		mV

Notes:
1. Long Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV.
2. This parameter is tested on a sample basis only, and guaranteed to an LTPD of 10.
3. Guaranteed by design.
4. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	OP-05E			OP-05C			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[4]			200	500		300	1300	μV
Long Term Input Offset Voltage Stability[1,2]			0.3	1.5		0.4	2.0	μV/Mo
Input Offset Current			0.5	3.8		0.8	6.0	nA
Input Bias Current			±1.2	±4.0		±1.8	±7.0	nA
Input Noise Voltage[2]	0.1Hz to 10Hz		0.35	0.6		0.38	0.65	μV_{p-p}
Input Noise Voltage Density[2]	f_O = 10Hz		10.3	18		10.5	20	$\frac{nV}{\sqrt{Hz}}$
	f_O = 100Hz		10	13		10.2	13.5	
	f_O = 1000Hz		9.6	11		9.8	11.5	
Input Noise Current[2]	0.1Hz to 10Hz		14	30		15	35	pA_{p-p}
Input Noise Current Density[2]	f_O = 10Hz		0.32	0.8		0.35	0.9	$\frac{pA}{\sqrt{Hz}}$
	f_O = 100Hz		0.14	0.23		0.15	0.27	
	f_O = 1000Hz		1.12	0.17		0.13	0.18	
Input Resistance (Diff. Mode)[3]		15	50		8.0	33		MΩ
Input Resistance (Com. Mode)			160			120		GΩ
Input Voltage Range		±13.5	±14		±13	±14		V
Common Mode Rejection Ratio	V_{CM} = ±13.5V	110	123		100	120		dB
Power Supply Rejection Ratio	V_S = ±3V to ±18V	94	105		90	104		dB
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_O = ±10V	200	500		120	400		V/mV
Large Signal Voltage Gain[3]	$R_L \geq 500k\Omega$, V_O = ±0.5V, V_S = ±3V	150	500		100	400		
Output Voltage Swing	$R_L \geq 10k\Omega$	±12.5	±13		±12	±13		V
	$R_L \geq 2k\Omega$	±12	±12.8		±11.5	±12.8		
	$R_L \geq 1k\Omega$	±10.5	±12		±10.5	±12		
Slew Rate[2]	$R_L \geq 2k\Omega$	0.1	0.17		0.1	0.17		V/μS
Unity Gain Bandwidth[2]			0.5			0.5		MHz
Open Loop Output Resistance	V_O = 0, I_O = 0		60			60		Ω
Power Consumption	V_S = ±15V		75	120		80	150	mW
	V_S = ±3V		4.0	6.0		4.0	8.0	
Offset Adjustment Range	R_p = 20kΩ		±4.0			±4.0		mV

Notes:
1. Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV.
2. This parameter is tested on a sample basis only, and guaranteed to an LTPD of 10.
3. Guaranteed by design.
4. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

Electrical Characteristics (V_S = ±15V and -55°C ≤ T_A ≤ +125°C unless otherwise noted)

Parameters	Test Conditions	OP-05A			OP-05			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[3]			100	240		300	700	μV
Average Input Offset Voltage Drift Without External Trim[2]			0.3	0.9		0.7	2.0	μV/°C
With External Trim[2]	R_P = 20kΩ		0.2	0.5		0.3	1.0	
Input Offset Current			0.8	4		1.2	5.6	nA
Average Input Offset Current Drift[1]			5	25		8	50	pA/°C
Input Bias Current			±1	±4		±2	±6	nA
Average Input Bias Current Drift[1]			8	25		13	50	pA/°C
Input Voltage Range		±13	±13.5		±13	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ±13V	110	123		110	123		dB
Power Supply Rejection Ratio	V_S = ±3V to ±18V	94	106		94	106		dB
Large Signal Voltage Gain	R_L ≥ 2kΩ, V_O = ±10V	200	400		150	400		V/mV
Output Voltage Swing	R_L ≥ 2kΩ	±12	±12.6		±12	±12.6		V

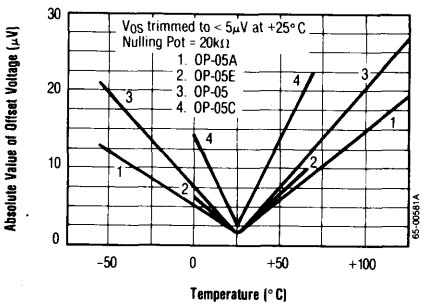
Electrical Characterisstics (V_S = ±15V and 0°C ≤ T_A ≤ +70°C unless otherwise noted)

Parameters	Test Conditions	OP-05E			OP-05C			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[3]			250	600		350	1600	μV
Average Input Offset Voltage Drift Without External Trim[2]			0.7	2.0		1.3	4.5	μV/°C
With External Trim[2]	R_P = 20kΩ		0.2	0.6		0.4	1.5	
Input Offset Current			0.9	5.3		1.6	8.0	nA
Average Input Offset Current Drift[1]			8.0	35		12	50	pA/°C
Input Bias Current			±1.5	±5.5		±2.2	±9.0	nA
Average Input Bias Current Drift[1]			13	35		18	50	pA/°C
Input Voltage Range		±13	±13.5		±13	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ±13V	107	123		97	120		dB
Power Supply Rejection Ratio	V_S = ±3V to ±18V	90	104		86	100		dB
Large Signal Voltage Gain	R_L ≥ 2kΩ, V_O = ±10V	180	450		100	400		V/mV
Output Voltage Swing	R_L ≥ 2kΩ	±12	±12.6		±11	±12.6		V

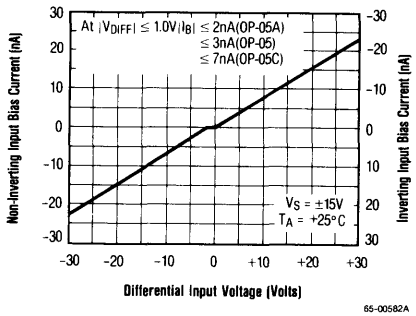
Notes:
1. This parameter is tested on a sample basis only, and guaranteed to an LTPD of 10.
2. Guaranteed by design.
3. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

Typical Performance Characteristics

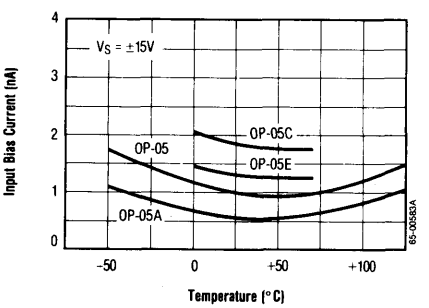
Trimmed Offset Voltage vs. Temperature



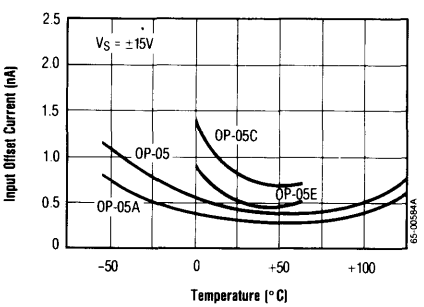
Input Bias Current vs. Differential Input Voltage



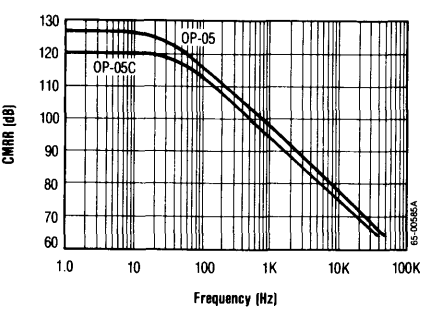
Input Bias Current vs. Temperature



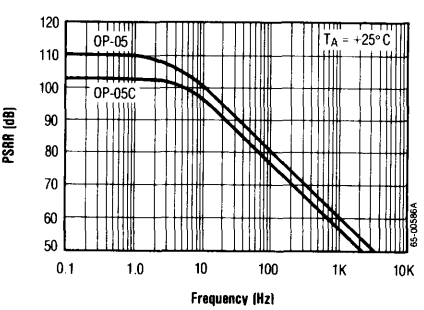
Input Offset Current vs. Temperature



CMRR vs. Frequency

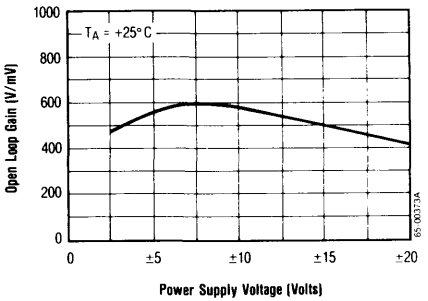


PSRR vs. Frequency

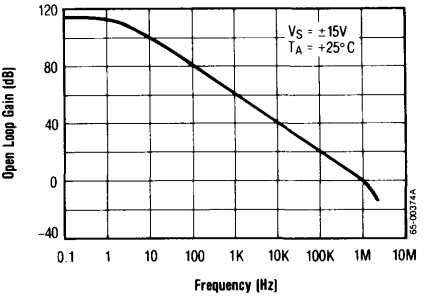


Typical Performance Characteristics (Continued)

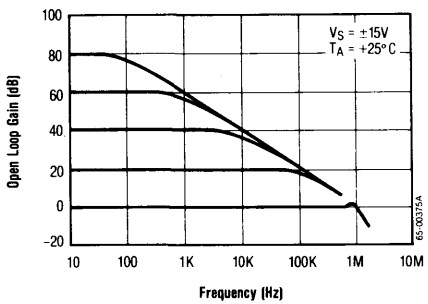
Open Loop Gain vs. Supply Voltage



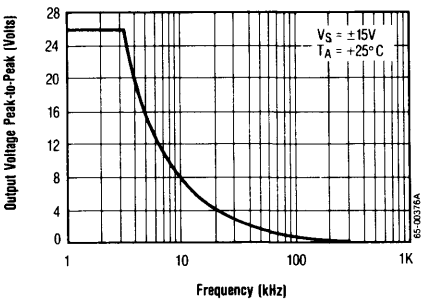
Open Loop Frequency Response



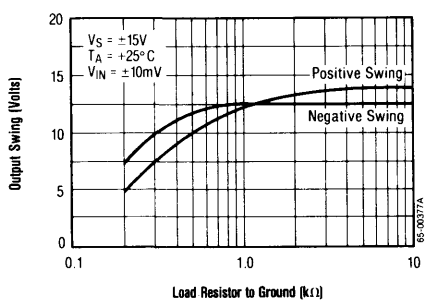
Closed Loop Response for Various Gain Configurations



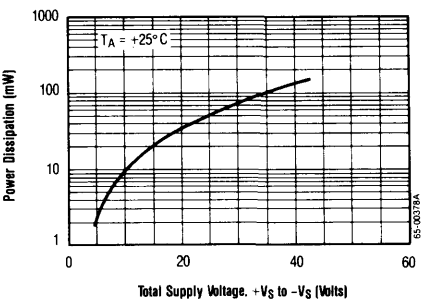
Maximum Undistorted Output vs. Frequency



Output Voltage vs. Load Resistance

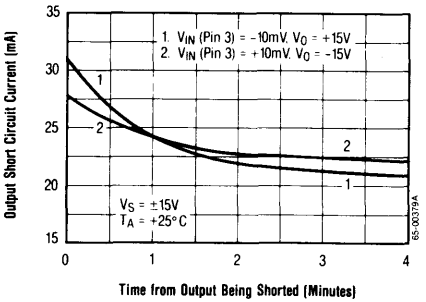


Power Consumption vs. Supply Voltage



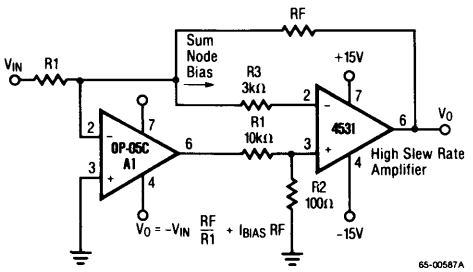
Typical Performance Characteristics (Continued)

Output Short Circuit Current vs. Time

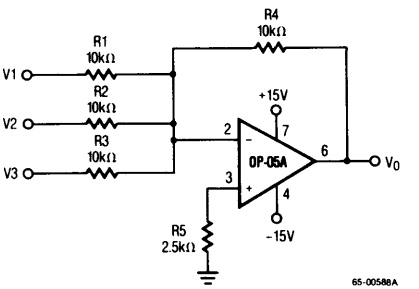


Typical Applications

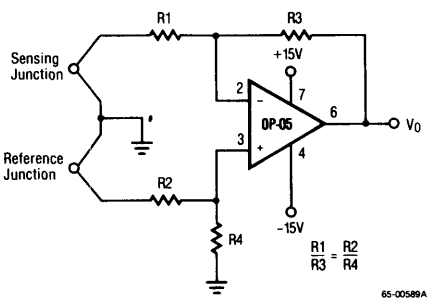
High Speed, Low V_{OS} Composite Amplifier*



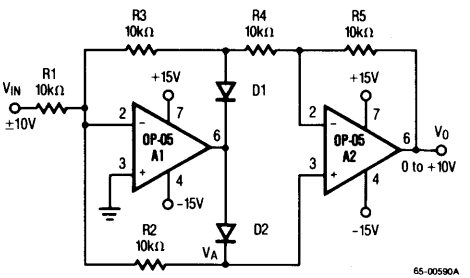
Adjustment-Free Precision Summing Amplifier*



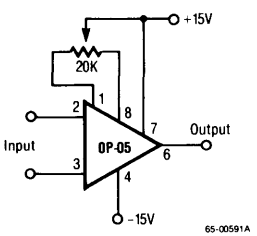
High Stability Thermocouple Amplifier*



Precision Absolute Value Circuit*



Offset Nulling Circuit



*Pin Outs Shown for Metal Can Packages

Raytheon

Instrumentation Grade Operational Amplifier

OP-07 Series

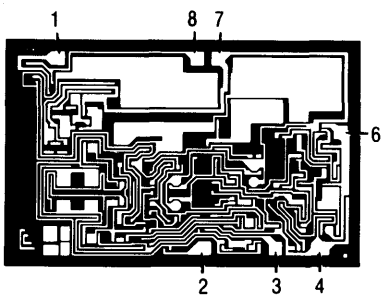
Features

- Low noise 0.1Hz to 10Hz — 0.35μV_{p-p}
- Ultra-low V_{OS} — 10μV
- Ultra-low V_{OS} Drift — 0.2$\mu V/°C$
- Fits 725, 108A, 741, and AD510 sockets
- Long term stability — 0.2μV/Month
- Low input bias current — ±1nA
- High CMRR — 126dB
- Wide input voltage range — ±14V

Description

The OP-07 amplifier series is designed for precision low level signal conditioning where ultra low V_{OS} and T_CV_{OS} are required along with very low bias currents. Internal compensation eliminates the need for external components. Novel circuit design and tight process controls are used to obtain very low values of V_{OS}. V_{OS} is further reduced by a computer controlled digital nulling technique at test. Low frequency noise is minimized. Internal biasing techniques reduce external bias and offset currents to values in the order of ±1nA over the military temperature range. OP-07s are direct replacements for the 108A, 714, 725 and 5507. They can replace chopper stabilized amplifiers in many applications.

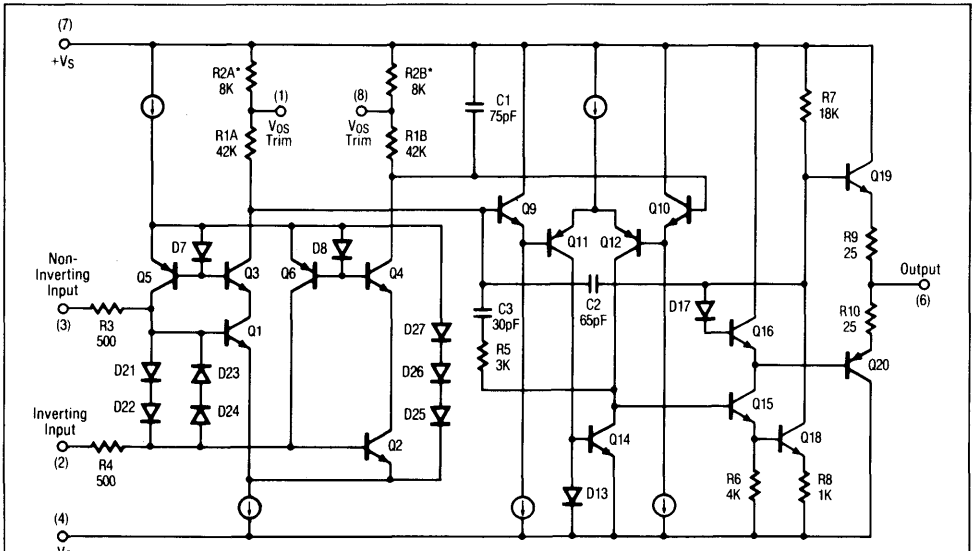
Mask Pattern



Die Size: 65 x 101 mils
Min. Pad Dimensions: 4 x 4 mils

65-00361A

Schematic Diagram

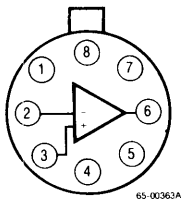


*R2A and R2B are electronically adjusted during factory test for minimum V_{OS}.

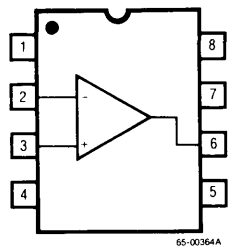
65-00362B

Connection Information

TO-99
Metal Can
(Top View)



8-Lead
Dual In-Line Package
(Top View)



Pin	Function
1	V_{OS} Trim
2	-Input
3	+Input
4	$-V_S$ (Case)
6	Output
7	$+V_S$
8	V_{OS} Trim

Absolute Maximum Ratings

Supply Voltage ..... ±22V
Input Voltage[1] ..... ±22V
Differential Input Voltage 30V
Internal Power Dissipation[2] 500mW
Output Short Circuit Duration ..... Indefinite
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
OP-07A ..... -55°C to +125°C
OP-07E/C/D ..... 0°C to +70°C
Lead Soldering Temperature
(60 Sec) ..... +300°C

Notes: 1. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
2. Maximum power dissipation vs. ambient temperature.

Thermal Characteristics

	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can
Max. Junction Temp.	175°C	175°C
Max. P_D T_A < 50°C	833mW	658mW
Therm. Res. θ_{JC}	45°C/W	50°C/W
Therm. Res. θ_{JA}	150°C/W	190°C/W
For T_A > 50°C Derate at	8.33mW per °C	5.26mW per °C

Ordering Information

Part Number *	Package	Operating Temperature Range
OP-07CT	TO-99	0°C to +70°C
OP-07DT	TO-99	0°C to +70°C
OP-07ET	TO-99	0°C to +70°C
OP-07CDE	Ceramic	0°C to +70°C
OP-07DDE	Ceramic	0°C to +70°C
OP-07EDE	Ceramic	0°C to +70°C
OP-07CNB	Plastic	0°C to +70°C
OP-07DNB	Plastic	0°C to +70°C
OP-07ENB	Plastic	0°C to +70°C
OP-07DE	Ceramic	-55°C to +125°C
OP-07DE/883B*	Ceramic	-55°C to +125°C
OP-07ADE	Ceramic	-55°C to +125°C
OP-07ADE/883B*	Ceramic	-55°C to +125°C
OP-07T	TO-99	-55°C to +125°C
OP-07T/883B*	TO-99	-55°C to +125°C
OP-07AT	TO-99	-55°C to +125°C
OP-07AT/883B*	TO-99	-55°C to +125°C

*MIL-STD-883, Level B Processing

Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	OP-07A			OP-07			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[4]			10	25		30	75	μV
Long Term Input Offset Voltage Stability[1,2]			0.2	1.0		0.2	1.0	μV/Mo
Input Offset Current			0.3	2.0		0.4	2.8	nA
Input Bias Current			±0.7	±2.0		±1.0	±3.0	nA
Input Noise Voltage[2]	0.1Hz to 10Hz		0.35	0.6		0.35	0.6	μV_{p-p}
Input Noise Voltage Density[2]	f_O = 10Hz		10.3	18		10.3	18	$\frac{nV}{\sqrt{Hz}}$
	f_O = 100Hz		10	13		10	13	
	f_O = 1000Hz		9.6	11		9.6	11	
Input Noise Current[2]	0.1Hz to 10Hz		14	30		14	30	pA_{p-p}
Input Noise Current Density[2]	f_O = 10Hz		0.32	0.80		0.32	0.80	$\frac{pA}{\sqrt{Hz}}$
	f_O = 100Hz		0.14	0.23		0.14	0.23	
	f_O = 1000Hz		0.12	0.17		0.12	0.17	
Input Resistance (Diff. Mode)[3]		30	80		20	60		MΩ
Input Resistance (Com. Mode)			200			200		GΩ
Input Voltage Range		±13	±14		±13	±14		V
Common Mode Rejection Ratio	V_{CM} = ±13V	110	126		110	126		dB
Power Supply Rejection Ratio	V_S = ±3V to ±18V	100	110		100	110		dB
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_O = ±10V	300	500		200	500		V/mV
Large Signal Voltage Gain[3]	$R_L \geq 500k\Omega$, V_O = ±0.5V, V_S = ±3V	150	500		150	500		
Output Voltage Swing	$R_L \geq 10k\Omega$	±12.5	±13		±12.5	±13		V
	$R_L \geq 2k\Omega$	±12	±12.8		±12	±12.8		
	$R_L \geq 1k\Omega$	±10.5	±12		±10.5	±12		
Slew Rate[2]	$R_L \geq 2k\Omega$	0.1	0.17		0.1	0.17		V/μS
Unity Gain Bandwidth[2]	A_{VCL} = +1.0		0.5			0.5		MHz
Open Loop Output Resistance	V_O = 0, I_O = 0		60			60		Ω
Power Consumption	V_S = ±15V		75	120		75	120	mW
	V_S = ±3V		4.0	6.0		4.0	6.0	
Offset Adjustment Range	R_P = 20kΩ		±4.0			±4.0		mV

Notes:
1. Long Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV.
2. This parameter is tested on a sample basis only, and guaranteed to an LTPD of 10.
3. Guaranteed by design.
4. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

Electrical Characteristics (Continued) (V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	OP-07E			OP-07C			OP-07D			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[4]			30	75		60	150		60	150	μV
Long Term Input Offset Voltage Stability[1,2]			0.3	1.5		0.4	2.0		0.5	3.0	μV/Mo
Input Offset Current			0.5	3.8		0.8	6.0		0.8	6.0	nA
Input Bias Current			±1.2	±4.0		±1.8	±7.0		±2.0	±12	nA
Input Noise Voltage[2]	0.1Hz to 10Hz		0.35	0.6		0.38	0.65		0.38	0.65	μV_{p-p}
Input Noise Voltage Density[2]	f_O = 10Hz		10.3	18		10.5	20		10.5	20	$\frac{nV}{\sqrt{Hz}}$
	f_O = 100Hz		10	13		10.2	13.5		10.2	13.5	
	f_O = 1000Hz		9.6	11		9.8	11.5		9.8	11.5	
Input Noise Current[2]	0.1Hz to 10Hz		14	30		15	35		15	35	pA_{p-p}
Input Noise Current Density[2]	f_O = 10Hz		0.32	0.8		0.35	0.9		0.35	0.9	$\frac{pA}{\sqrt{Hz}}$
	f_O = 100Hz		0.14	0.23		0.15	0.27		0.15	0.27	
	f_O = 1000Hz		0.12	0.17		0.13	0.18		0.13	0.18	
Input Resistance (Diff. Mode)[3]		15	50		8.0	33		7.0	31		MΩ
Input Resistance (Com. Mode)			160			120			120		GΩ
Input Voltage Range		±13	±14		±13	±14		±13	±14		V
Common Mode Rejection Ratio	V_{CM} = ±13V	106	123		100	120		94	110		dB
Power Supply Rejection Ratio	V_S = ±3.0V to ±18V	94	107		90	104		90	104		dB
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_O = ±10V	200	500		120	400		120	400		V/mV
Large Signal Voltage Gain[3]	$R_L \geq 500\Omega$, V_O = ±0.5V, V_S = ±3.0V	150	500		100	400					
Output Voltage Swing	$R_L \geq 10k\Omega$	±12.5	±13		±12	±13		±12	±13		V
	$R_L \geq 2k\Omega$	±12	±12.8		±11.5	±12.8		±11.5	±12.8		
	$R_L \geq 1k\Omega$	±10.5	±12			±12					
Slew Rate[2]	$R_L \geq 2k\Omega$	0.1	0.17		0.1	0.17		0.1	0.17		V/μS
Unity Gain Bandwidth[2]	A_{VCL} = +1.0		0.5			0.5			0.5		MHz
Open Loop Output Resistance	V_O = 0, I_O = 0		60			60			60		Ω
Power Consumption	V_S = ±15V		75	120		80	150		80	150	mW
	V_S = ±3.0V		4.0	6.0		4.0	8.0		4.0	8.0	
Offset Adjustment Range	R_p =20kΩ		±4.0			±4.0			±4.0		mV

(See footnotes on page 6-60)

Electrical Characteristics (Continued)

(V_S = ±15V and -55°C ≤ T_A ≤ +125°C unless otherwise noted)

Parameters	Test Conditions	OP-07A			OP-07			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[3]			25	60		60	200	μV
Average Input Offset Voltage Drift Without External Trim[2]			0.2	0.6		0.3	1.3	μV/°C
With External Trim[2]	R_p = 20kΩ		0.2	0.6		0.3	1.3	μV/°C
Input Offset Current			0.8	4.0		1.2	5.6	nA
Average Input Offset Current Drift[1]			5.0	25		8.0	50	pA/°C
Input Bias Current			±1.0	±4.0		±2.0	±6.0	nA
Average Input Bias Current Drift[1]			8.0	25		13	50	pA/°C
Input Voltage Range		±13	±13.5		±13	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ±13V	106	123		106	123		dB
Power Supply Rejection Ratio	V_S = ±3.0V to ±18V	94	106		94	106		dB
Large Signal Voltage Gain	R_L ≥ 2kΩ, V_O = ±10V	200	400		150	400		V/mV
Output Voltage Swing	R_L ≥ 2kΩ	±12	±12.6		±12	±12.6		V

Notes: 1. This parameter is tested on a sample basis only, and guaranteed to an LTPD of 10.
2. Guaranteed by design.
3. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

Electrical Characteristics (Continued)

(V_S = ±15V and 0°C ≤ T_A ≤ +70°C unless otherwise noted)

Parameters	Test Conditions	OP-07E			OP-07C			OP-07D			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[3]			45	130		85	250		85	250	μV
Average Input Offset Voltage Drift											
Without External Trim[2]			0.3	1.3		0.5	1.8		0.7	2.5	μV/°C
With External Trim[2]	R_P = 20kΩ		0.3	1.3		0.4	1.6		0.7	2.5	μV/°C
Input Offset Current			0.9	5.3		1.6	8.0		1.6	8.0	nA
Average Input Offset Current Drift[1]			8.0	35		12	50		12	50	pA/°C
Input Bias Current			±1.5	±5.5		±2.2	±9.0		±3.0	±14	nA
Average Input Bias Current Drift[1]			13	35		18	50		18	50	pA/°C
Input Voltage Range		±13	±13.5		±13	±13.5		±13	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ±13V	103	123		97	120		94	106		dB
Power Supply Rejection Ratio	V_S = ±3.0V to ±18V	90	104		86	100		86	100		dB
Large Signal Voltage Gain	R_L ≥ 2kΩ, V_O = ±10V	180	450		100	400		100	400		V/mV
Output Voltage Swing	R_L = 2kΩ	±12	±12.6		±11	±12.6		±11	±12.6		V

Notes:
1. This parameter is tested on a sample basis only, and guaranteed to an LTPD of 10.
2. Guaranteed by design.
3. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

Digital Nulling Technique

The digital nulling technique involves the zener diode nulling network of Figure 1. The zener diodes have relatively high breakdown voltages and never operate in the zener mode. The purpose of the zeners is to short out resistors R1, 2R1, 4R1, or 8R1 by forcing a high reverse current through the diode to metalize the junction. The input offset voltage can be adjusted by varying the collector resistor ratio. If the difference in the two collector resistors (R_C) is a small increment ΔR_C, V_{OS} can be written as:

$$V_{OS} = V_T \ln \frac{R_C + \Delta R_C}{R_C} = V_T \ln 1 + \frac{\Delta R_C}{R_C}$$

for $\Delta R_C/R_C \ll 1.0$ $\ln(1+\Delta R_C/R_C) \approx \Delta R_C/R_C$, thus:

$$V_{OS} \approx V_T \frac{\Delta R_C}{R_C}$$

For Figure 1 R2 + R3 $\gg$ 8R1, thus

$$V_{OS} \approx -V_T \frac{R_1}{8R1 + R2 + R3} (7 - B_3B_2B_1) \quad (B_0 = 1)$$

or:

$$V_{OS} \approx V_T \frac{R1}{R2 + R3} \quad (1 + B_3B_2B_1) \quad (B_0 = 0)$$

where $B_3B_2B_1$ is a binary number which corresponds to the state of zener diodes Z1, Z2 and Z3 as per Figure 1.

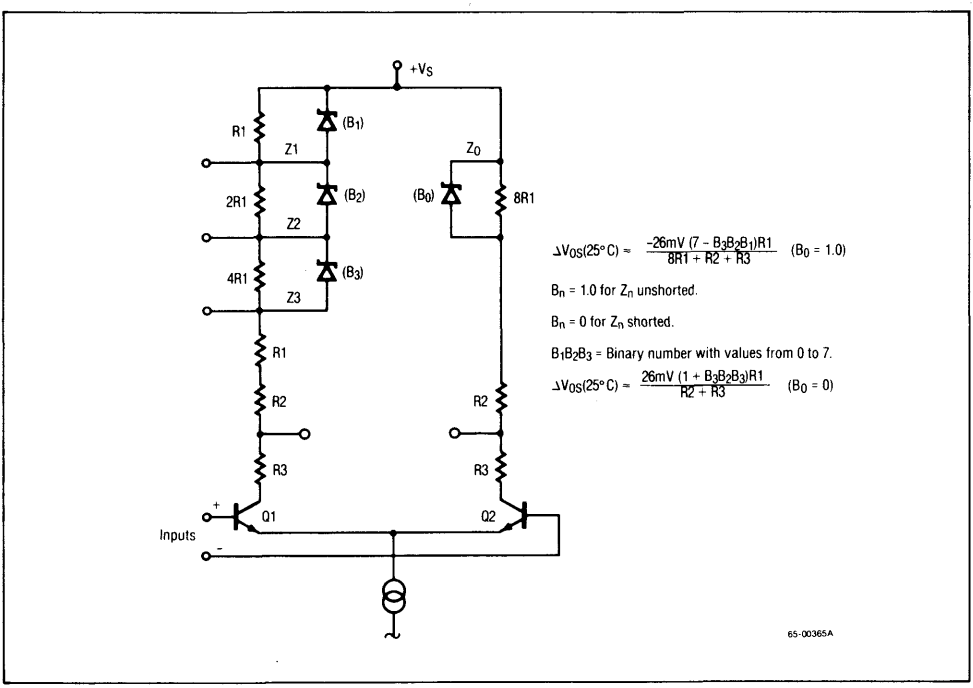
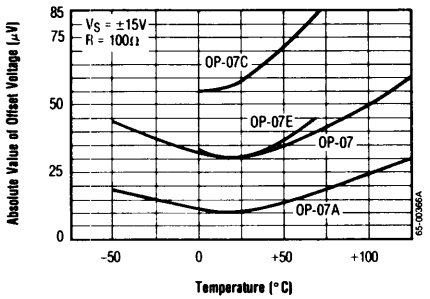


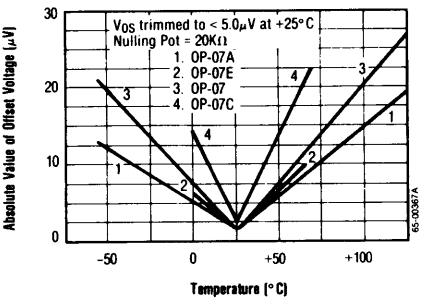
Figure 1. Digital Nulling Network

Typical Performance Characteristics

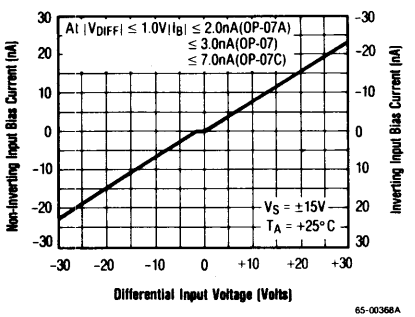
Untrimmed Offset Voltage vs. Temperature



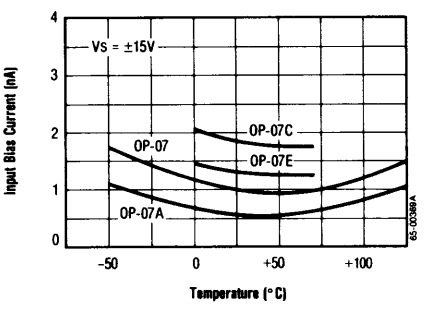
Trimmed Offset Voltage vs. Temperature



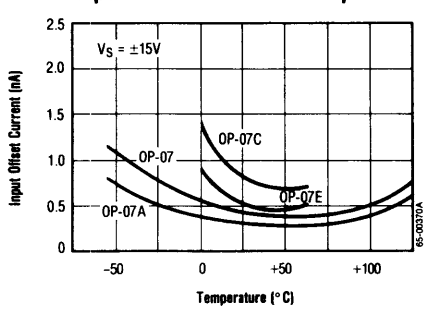
Input Bias Current vs. Differential Input Voltage



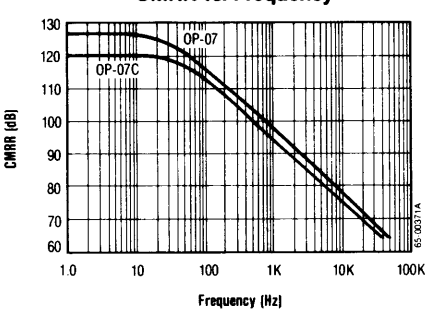
Input Bias Current vs. Temperature



Input Offset Current vs. Temperature

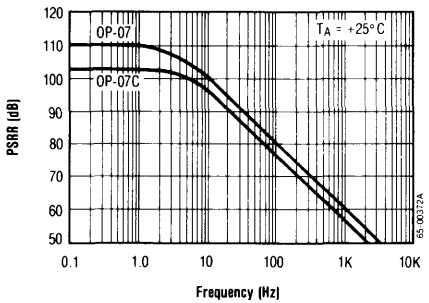


CMRR vs. Frequency

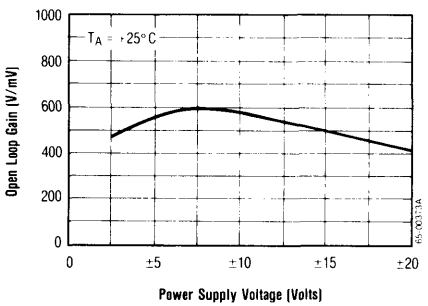


Typical Performance Characteristics (Continued)

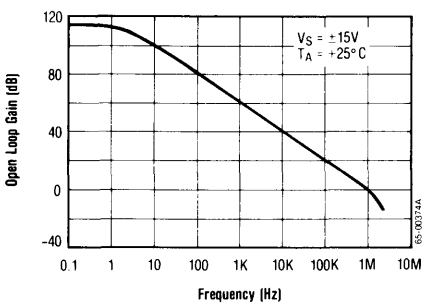
PSRR vs. Frequency



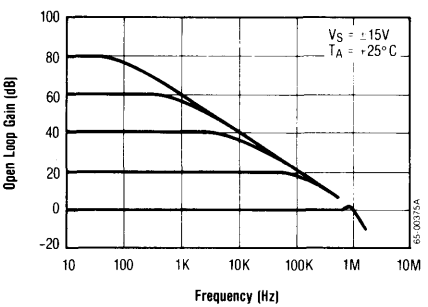
Open Loop Gain vs. Supply Voltage



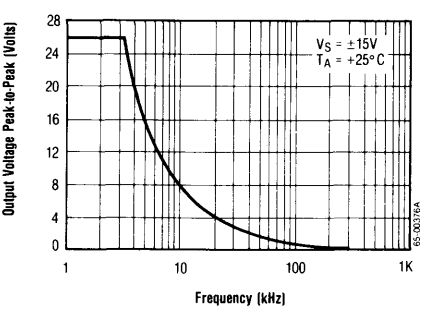
Open Loop Frequency Response



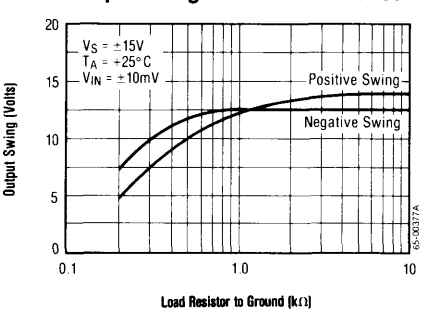
Closed Loop Response for Various Gain Configurations



Maximum Undistorted Output vs. Frequency

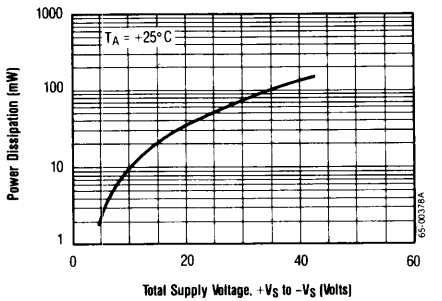


Output Voltage vs. Load Resistance

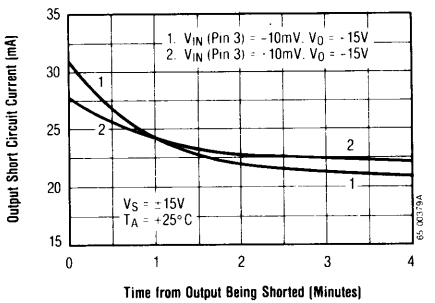


Typical Performance Characteristics (Continued)

Power Consumption vs. Supply Voltage

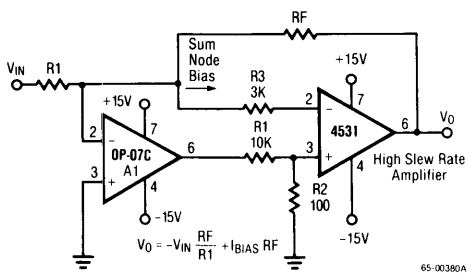


Output Short Circuit Current vs. Time

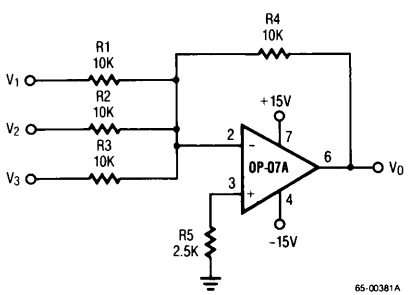


Typical Applications

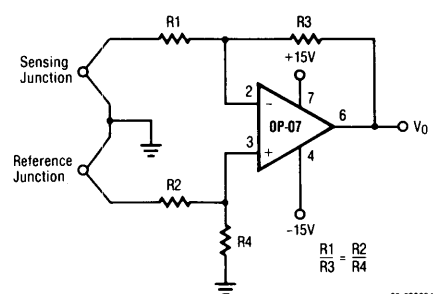
High Speed, Low V_{OS} Composite Amplifier*



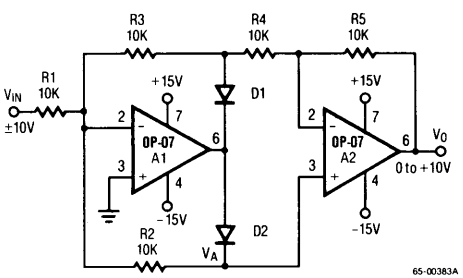
Adjustment-Free Precision Summing Amplifier*



High Stability Thermocouple Amplifier*



Precision Absolute Value Circuit*



*Pin Outs Shown for Metal Can Packages

Raytheon

Very Low Noise Operational Amplifier

OP-27

Features

- Very low noise
  Spectral noise density — 3.0nV/$\sqrt{Hz}$
  1/f Noise corner frequency — 2.7Hz
- Very low V_{OS} Drift
  0.2μV/Mo
  0.2μV/°C
- High gain — 1.8 x 10^6V/V
- High output drive capability — ±12V into 600Ω load
- High slew rate — 2.8V/μS
- Wide gain bandwidth product — 8MHz
- Good common mode rejection ratio — 126dB
- Low input offset voltage — 10μV
- Minimum low frequency noise — 0.08μV_{p-p} 0.1Hz to 10Hz
- Low input bias and offset currents — 10nA

Description

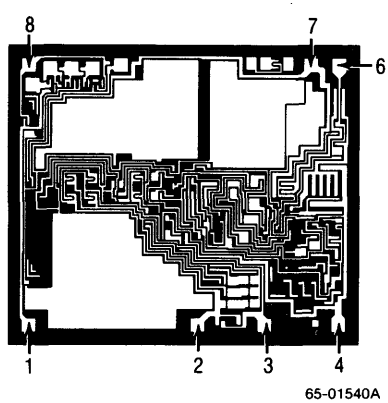
The OP-27 is designed for instrumentation grade signal conditioning where low noise (both spectral density and burst), wide bandwidth, and high slew rate are required along with low input offset voltage, low input offset temperature coefficient, and low input bias currents. These features are all available in a device which is internally compensated for excellent phase margin (70°) in a unity gain configuration. Digital nulling techniques performed at wafer sort make it feasible to guarantee temperature stable input offset voltages as low as 25μV. Input bias current cancellation techniques are used to obtain 10nA input bias currents.

The OP-27 is especially useful for instrumentation and professional quality audio systems. Applying the slew rate vs. power bandwidth equation ($fp = SR/2\pi V_p$), the OP-27 will have an undistorted output up to its power bandwidth frequency of 34kHz, and an undistorted output of $8.0V_{p-p}$ at 100kHz. This device provides performance adequate for the most demanding high fidelity applications.

In addition to providing superior performance for the professional audio market the OP-27 design uniquely addresses the needs of the instrumentation designer. Power supply rejection and common mode rejection are both in excess of 120dB. A phase margin of 70° at unity gain guards against peaking (and ringing) in low gain feedback circuits. Stable operation can be obtained with capacitive loads up to 2000pF[1]. Input offset voltage can be externally trimmed without affecting input offset voltage drift with temperature or time. The drift performance is, in fact, so good that the system designer must be cautioned that stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals are enough to degrade its performance. For this reason it is also important to keep both input terminals at the same relative temperature. The well behaved temperature performance of the OP-27 has made it unnecessary to specify a commercial grade (0°C to +70°C). All grades of the OP-27 are specified to, at least, the industrial grade (-25°C to +85°C) temperature range.

Note: 1. By decoupling the load capacitance with a series resistor of 50Ω or more load capacitances larger than 2000pF can be accommodated.

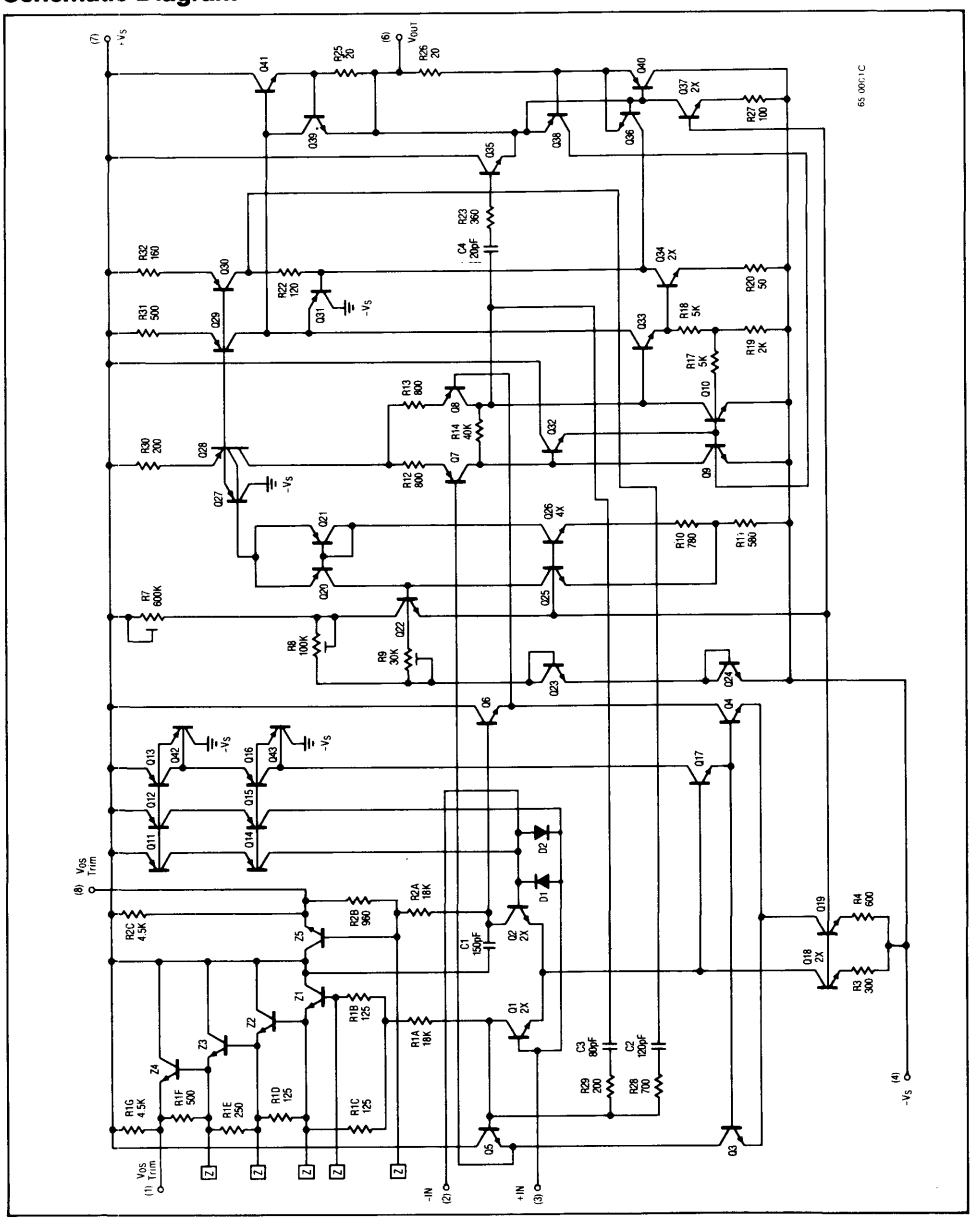
Mask Pattern



65-01540A

Die Size: 85 x 98 mils
Min. Pad Dimensions: 4 x 4 mils

Schematic Diagram

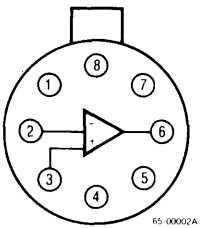


Very Low Noise Operational Amplifier

OP-27

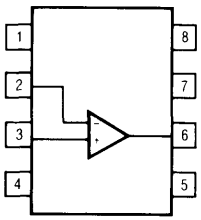
Connection Information

TO-99
Metal Can
(Top View)



65-00002A

8-Lead
Dual In-Line Package
(Top View)



65-00103A

Pin	Function
1	V_{OS} Trim
2	Inverting Input
3	Non-Inverting Input
4	$-V_S$
5	NC
6	Output
7	$+V_S$
8	V_{OS} Trim

Absolute Maximum Ratings

Supply Voltage ..... +22V
Input Voltage[1] ..... ±22V
Differential Input Voltage 0.7V
Internal Power Dissipation 658mW
Output Short Circuit Duration ..... Indefinite
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
OP-27A/B/C ..... -55°C to +125°C
OP-27E/F/G ..... -25°C to +85°C
Lead Soldering Temperature
(60 Sec) ..... +300°C

Note: 1. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

Thermal Characteristics

	8-Lead Ceramic DIP	TO-99 8-Lead Metal Can
Max. Junction Temp.	175°C	175°C
Max. P_D T_A < 50°C	833mW	658mW
Therm. Res. θ_{JC}	45°C/W	50°C/W
Therm. Res. θ_{JA}	150°C/W	190°C/W
For T_A > 50°C Derate at	8.33mW per °C	5.26mW per °C

Ordering Information

Part Number	Package	Operating Temperature Range
OP-27EDE	Ceramic	-25°C to +85°C
OP-27FDE	Ceramic	-25°C to +85°C
OP-27GDE	Ceramic	-25°C to +85°C
OP-27ET	TO-99	-25°C to +85°C
OP-27FT	TO-99	-25°C to +85°C
OP-27GT	TO-99	-25°C to +85°C
OP-27ENB	Plastic	-25°C to +85°C
OP-27FNB	Plastic	-25°C to +85°C
OP-27GNB	Plastic	-25°C to +85°C
OP-27ADE	Ceramic	-55°C to +125°C
OP-27ADE/883B*	Ceramic	-55°C to +125°C
OP-27BDE	Ceramic	-55°C to +125°C
OP-27BDE/883B*	Ceramic	-55°C to +125°C
OP-27CDE	Ceramic	-55°C to +125°C
OP-27CDE/883B*	Ceramic	-55°C to +125°C
OP-27AT	TO-99	-55°C to +125°C
OP-27AT/883B*	TO-99	-55°C to +125°C
OP-27BT	TO-99	-55°C to +125°C
OP-27BT/883B*	TO-99	-55°C to +125°C
OP-27CT	TO-99	-55°C to +125°C
OP-27CT/883B*	TO-99	-55°C to +125°C

*MIL-STD-883, Level B Processing

Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	OP-27A/E			OP-27B/F			OP-27C/G			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[5]			10	25		20	60		30	100	μV
Long Term Input Offset Voltage Stability[1,2]			0.2	1.0		0.3	1.5		0.4	2.0	μV/Mo
Input Offset Current			7.0	35		9.0	50		12	75	nA
Input Bias Current			±10	±40		±12	±55		±15	±80	nA
Input Noise Voltage[2]	0.1Hz to 10Hz		0.08	0.18		0.08	0.18		0.09	0.25	μV_{p-p}
Input Noise Voltage Density[2]	f_0 = 10Hz		3.5	5.5		3.5	5.5		3.8	8.0	$\frac{nV}{\sqrt{Hz}}$
	f_0 = 30Hz		3.1	4.5		3.1	4.5		3.3	5.6	
	f_0 = 1000Hz		3.0	3.8		3.0	3.8		3.2	4.5	
Input Noise Current Density[2]	f_0 = 10Hz		1.7	4.0		1.7	4.0		1.7		$\frac{pA}{\sqrt{Hz}}$
	f_0 = 30Hz		1.0	2.3		1.0	2.3		1.0		
	f_0 = 1000Hz		0.4	0.6		0.4	0.6		0.4	0.6	
Input Resistance (Diff. Mode)[4]		1.5	6.0		1.2	5.0		0.8	4.0		MΩ
Input Resistance (Com. Mode)			3.0			2.5			2.0		GΩ
Input Voltage Range[3]		±11	±12.3		±11	±12.3		±11	±12.3		V
Common Mode Rejection Ratio	V_{CM} = ±11V	114	126		106	123		100	120		dB
Power Supply Rejection Ratio	V_S = ±4.0V to ±18V	100	120		100	120		94	118		dB
Large Signal Voltage Gain	$R_L \geq 2.0k\Omega$, V_O = ±10V	1000	1800		1000	1800		700	1500		V/mV
	$R_L \geq 1.0k\Omega$, V_O = ±10V	800	1500		800	1500			1500		
	V_O = ±1.0V, V_S = ±4.0V[4]	250	700		250	700		200	500		
Output Voltage Swing	$R_L \geq 2.0k\Omega$	±12	±13.8		±12	±13.8		±11.5	±13.5		V
	$R_L \geq 600\Omega$	±11	±12		±11	±12		±11	±12		
Slew Rate[4]	$R_L \geq 2.0k\Omega$	1.7	2.8		1.7	2.8		1.7	2.8		V/μS
Gain Bandwidth Product[4]		5.0	8.0		5.0	8.0		5.0	8.0		MHz
Open Loop Output Resistance	V_O = 0, I_O = 0		70			70			70		Ω
Power Consumption			90	140		90	140		100	170	mW
Offset Adjustment Range	R_P = 10kΩ		±4.0			±4.0			±4.0		mV

Notes:
1. Long Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV.
2. This parameter is tested on a sample basis only, and guaranteed to an LTPD of 10.
3. Caution: The Common Mode Input Range is a function of supply voltage. See Typical Performance Curves. Also, the input protection diodes do not allow the device to be removed or inserted into the circuit without first removing power.
4. Parameter is guaranteed by design.
5. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

Electrical Characteristics (V_S = ±15V, -55°C ≤ T_A ≤ +125°C unless otherwise noted)

Parameters	Test Conditions	OP-27A			OP-27B			OP-27C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[1]			30	60		50	200		70	300	μV
Average Input Offset Voltage Drift[2]			0.2	0.6		0.3	1.3		0.4	1.8	μV/°C
Input Offset Current			15	50		22	85		30	135	nA
Input Bias Current			±20	±60		±28	±95		±35	±150	nA
Input Voltage Range		±10.3	±11.5		±10.3	±11.5		±10.2	±11.5		V
Common Mode Rejection Ratio	V_{CM} = ±10V	108	122		100	119		94	116		dB
Power Supply Rejection Ratio	V_S = ±4.5V to ±18V	96	116		94	114		86	110		dB
Large Signal Voltage Gain	$R_L \geq 2.0k\Omega$, V_O = ±10V	600	1200		500	1000		300	800		V/mV
Output.Voltage Swing	$R_L \geq 2.0k\Omega$	±11.5	±13.5		±11	±13.2		±10.5	±13		V

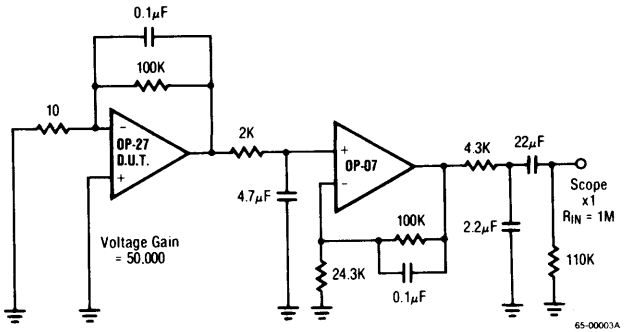
Electrical Characteristics (V_S = ±15V, -25°C ≤ T_A ≤ +85°C unless otherwise noted)

Parameters	Test Conditions	OP-27E			OP-27F			OP-27G			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[1]			20	50		40	140		55	220	μV
Average Input Offset Voltage Drift			0.2	0.6		0.3	1.3		0.4	1.8	μV/°C
Input Offset Current			10	50		14	85		20	135	nA
Input Bias Current			±14	±60		±18	±95		±25	±150	nA
Input Voltage Range		±10.5	±11.8		±10.5	±11.8		±10.5	±11.8		V
Common Mode Rejection Ratio	V_{CM} = ±10V	110	124		102	121		96	118		dB
Power Supply Rejection Ratio	V_S = ±4.5V to ±18	97	118		96	116		90	114		dB
Large Signal Voltage Gain	$R_L \geq 2.0k\Omega$, V_O = ±10V	750	1500		700	1300		450	1000		V/mV
Output Voltage Swing	$R_L \geq 2.0k\Omega$	±11.7	±13.6		±11.4	±13.5		±11	±13.3		V

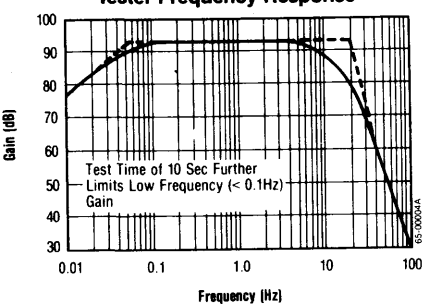
Notes: 1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. $T_C V_{OS}$ performance is guaranteed unnulled or when nulled with R_P = 8.0kΩ to 20kΩ

Typical Performance Characteristics

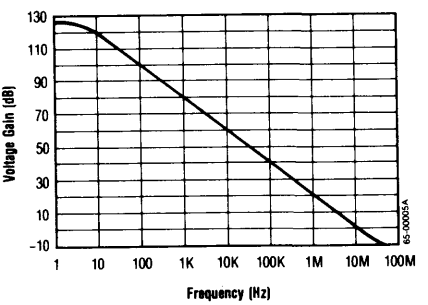
0.1Hz to 10Hz Noise Test Circuit



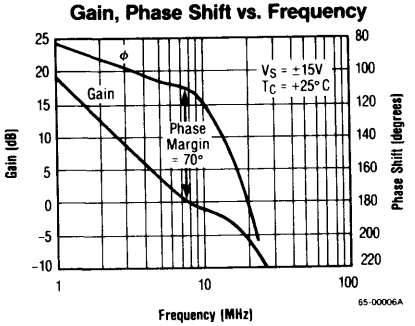
0.1Hz to 10Hz Peak-to-Peak Noise Tester Frequency Response



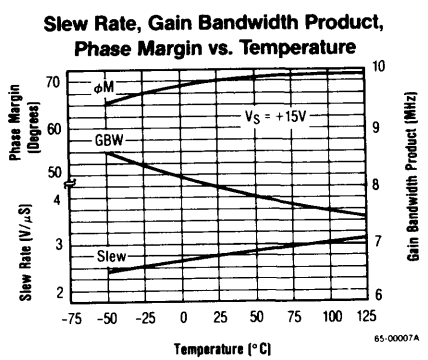
Open Loop Gain vs. Frequency



Gain, Phase Shift vs. Frequency

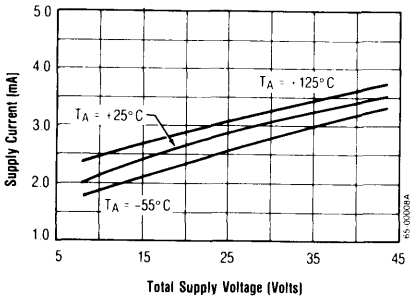


Slew Rate, Gain Bandwidth Product, Phase Margin vs. Temperature

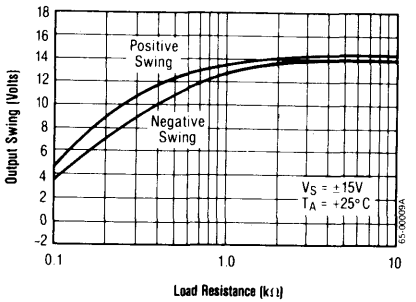


Typical Performance Characteristics (Continued)

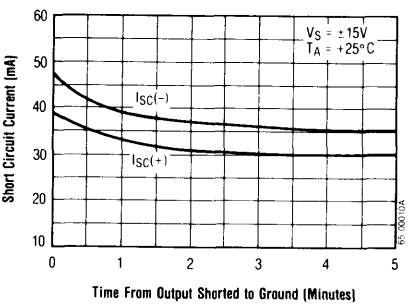
Supply Current vs. Supply Voltage



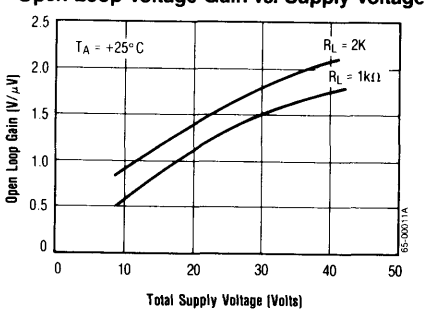
Maximum Output Swing vs. Resistive Load



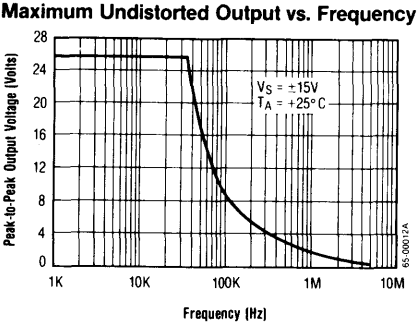
Short Circuit Current vs. Time



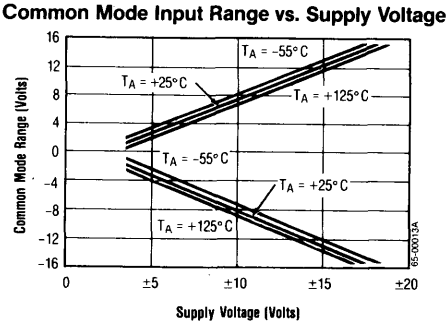
Open Loop Voltage Gain vs. Supply Voltage



Maximum Undistorted Output vs. Frequency

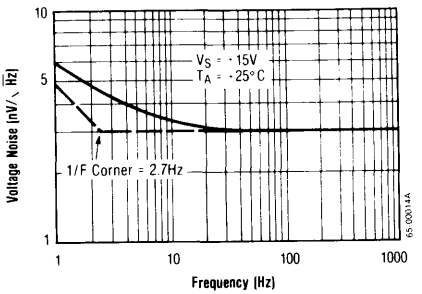


Common Mode Input Range vs. Supply Voltage

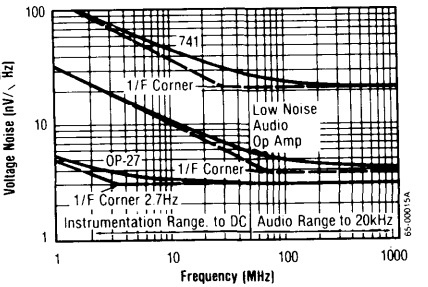


Typical Performance Characteristics (Continued)

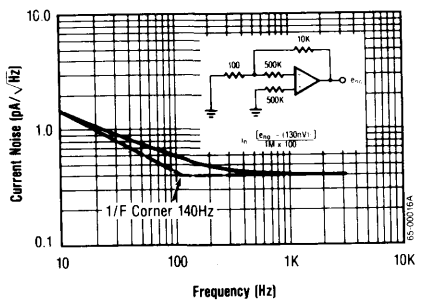
OP-27 Voltage Noise vs. Frequency



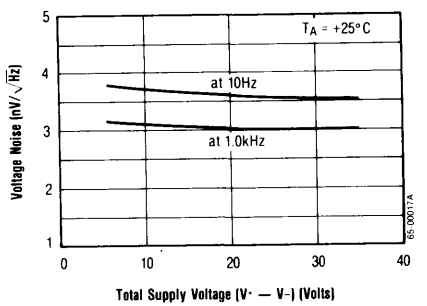
A Comparison of Op Amp Voltage Noise Spectrums



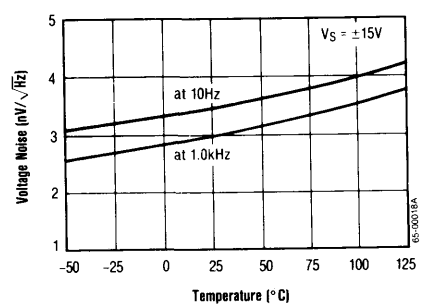
Current Noise vs. Frequency



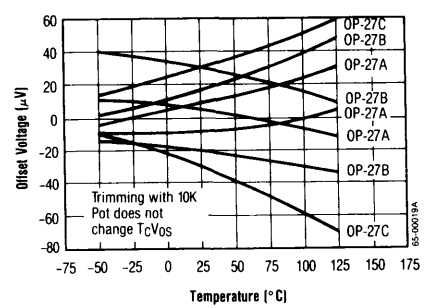
Voltage Noise vs. Supply Voltage



Voltage Noise vs. Temperature

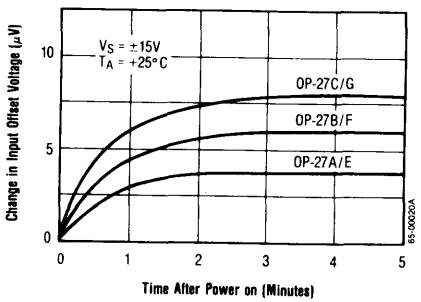


Offset Voltage Drift of Representative Units

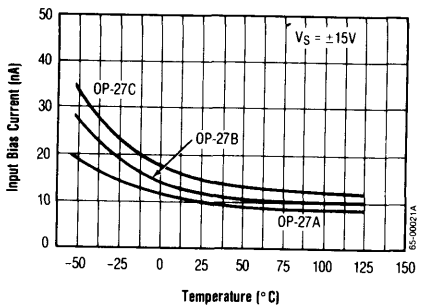


Typical Performance Characteristics (Continued)

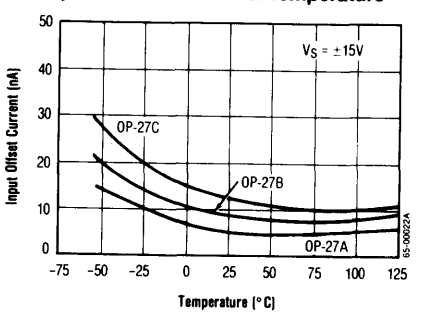
Warm-Up Drift



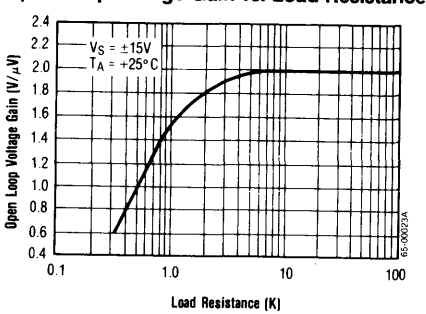
Input Bias Current vs. Temperature



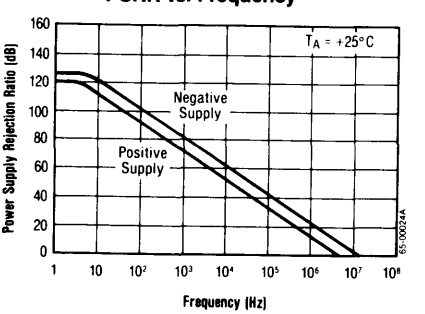
Input Offset Current vs. Temperature



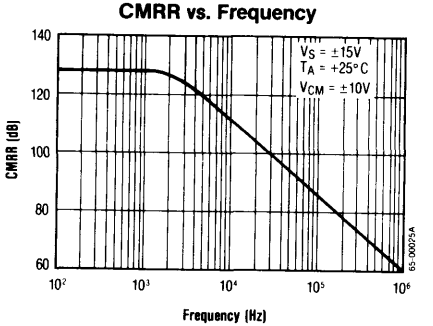
Open Loop Voltage Gain vs. Load Resistance



PSRR vs. Frequency

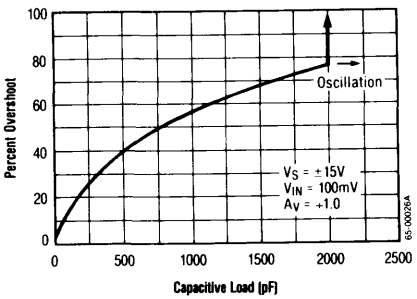


CMRR vs. Frequency

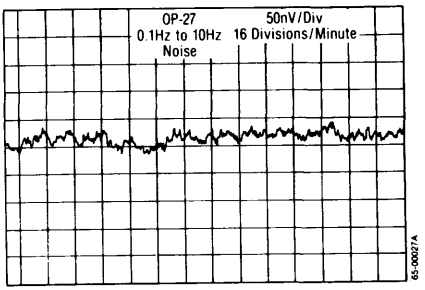


Typical Performance Characteristics (Continued)

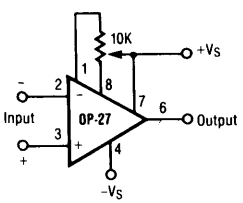
Small Signal Overshoot vs. Capacitive Load



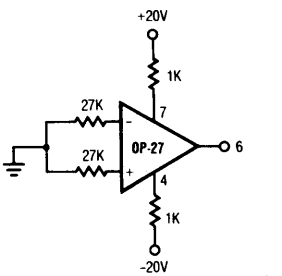
OP-27 0.1Hz to 10Hz Peak-to-Peak Noise
Vertical Scale 50nV/Division
Recorder Speed 16 Divisions/Min



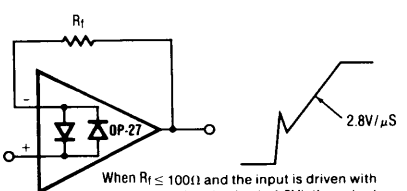
Offset Nulling Circuit



Burn-In Circuit



Large Signal Transient Response



When $R_f \leq 100\Omega$ and the input is driven with a fast, large signal pulse (≥ 1.0V), the output waveform will look as shown

65-00030A

Typical Applications

RIAA Phono Preamplifier (Figure 1)

The new moving coil magnetic phono cartridges have sensitivities that are an order of magnitude lower than the sensitivity of a typical moving magnet cartridge (0.1mV per CM/S versus 1.0mV per CM/S). This places a greater burden on the preamplifier to achieve more gain and less noise. The OP-27 is ideally suited for this task. The object in designing an RIAA phono preamp is to achieve the RIAA gain-frequency response curve while contributing as little noise as possible to avoid masking the very small signal generated by the cartridge. The circuit shown is adjusted to match a 40dB RIAA curve as shown in Figure 2. Note that by convention the RIAA gain is specified at 1kHz. With the "break points" of the curves specified at 50,500 and 2.1kHz respectively the entire curve is fixed by the specified gain at 1kHz.

The circuit is designed to operate with a 3/4000Ω step-up transformer to present the optimum source impedance to the amplifier for best noise figure. The optimum source impedance is obtained as the ratio of the spectral noise voltage e_n to the spectral noise current i_n (when e_n has dimensions of $nV/\sqrt{Hz}$ and i_n has dimensions of $pA/\sqrt{Hz}$ and the ratio has dimensions of kΩ). The circuit is designed to be tested and adjusted independent of the transformer, for this purpose introduce a very low level signal ≈ 1mV at test point TP-1. The first stage is a wideband stage which provides a small amount of gain (1 + R4/R5) approximately equal to 10dB. Low value feedback resistors must be used to prevent additional noise due to the spectral current noise or excessive Johnson noise. The gain of the first stage reduces the noise contribution of the second stage. The RIAA transfer curve poles and zeros are due entirely to the feedback network of the second stage.

The poles and zeros of the RIAA feedback network are sufficiently separated in frequency that they may be estimated with the following equations:

$$f_1(50Hz) \approx \frac{1}{2\pi R7C3}$$

$$f_2(500Hz) \approx \frac{1}{2\pi R8C3}$$

$$f_3(2100Hz) \approx \frac{1}{2\pi R8C2}$$

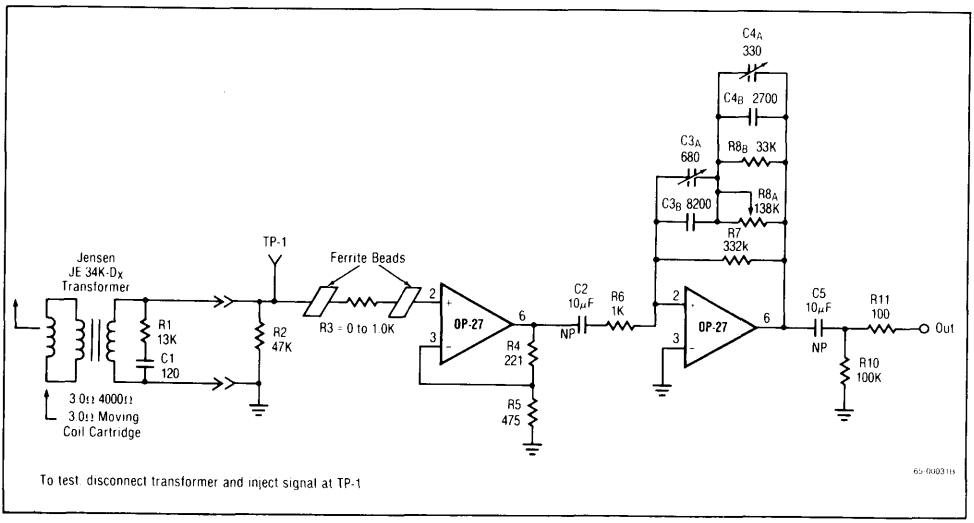


Figure 1. RIAA Phono Preamplifier

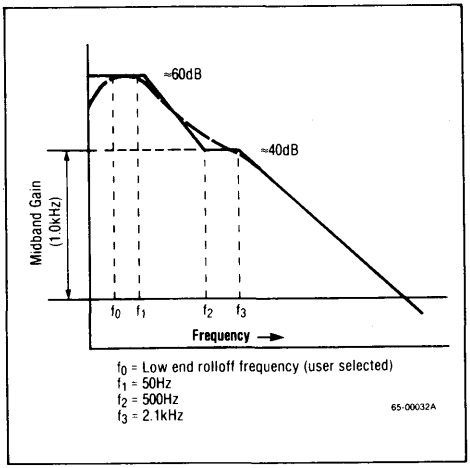


Figure 2. RIAA Phono Playback Equalization Curve

These equations are only approximations. Final tuning is performed with the adjustable capacitors and potentiometers. The following sequence can be used to adjust for the RIAA response after injecting a low level signal into TP-1 (transformer disconnected).

1. At 100Hz adjust C3A for an output level 6dB lower than the low frequency output.
2. At 1000Hz adjust R8A for an output level 20dB lower than the low frequency output.
3. At 21kHz adjust C4A for an output 40dB less than the low frequency output.

Low Impedance Microphone Preamp (Figure 3)

In this preamp the transformer converts the low microphone impedance up to a value that is close to the optimum source impedance required by the OP-27 for best noise performance. The optimum source impedance can be calculated as the ratio of e_n/i_n which for the OP-27 is approximately 7000Ω. Fortunately the noise performance does not degrade appreciably until the source impedance is four or five times this optimum value and the source impedance at the output of this transformer, approximately 15kΩ, still provides near optimum noise performance. (A high quality audio transformer with a step-up ratio of 6.7 to one is not available.) The voltage gain of the amplifier, not including the transformer step-up, is unity up to about 1.5Hz. It may be desirable to reduce the size of this capacitor to minimize burst noise even though the OP-27 has a 1/f noise corner below 3Hz. C2 rolls off the high frequency response at 90kHz giving a noise power bandwidth of 140kHz.

Instrumentation

The OP-27 is particularly adaptable to instrumentation applications. When wired into a single op amp difference amplifier configuration, the OP-27 exhibits outstanding common mode rejection ratio. The spot voltage noise is so low that it is dominated almost entirely by the resistor Johnson noise.

The three op amp instrumentation amplifier of Figure 8 avoids the low input impedance characteristics of difference amplifiers at the expense of two more operational amplifiers and a slight degradation in noise performance. The noise increases because two amplifiers are contributing to the input voltage spectral noise instead of one. Thus the noise contribution, exclusive of resistor Johnson noise, increases by slightly more than the $\sqrt{2}$. The spectral noise voltage increases from approximately $3nV/\sqrt{Hz}$ to approximately $4.9nV/\sqrt{Hz}$, with the third amplifier contributing about 10% of the noise. The gain of the input amplifier is set at 25 and the second stage at 40 for an overall gain of 1000. R7 is trimmed to optimize the common mode rejection (CMRR) with frequency. With balanced source resistors a CMRR of 100dB is achieved. With a 1kΩ source impedance imbalance CMRR is degraded to 80dB at 5kHz due to the finite (3GΩ) input impedance.

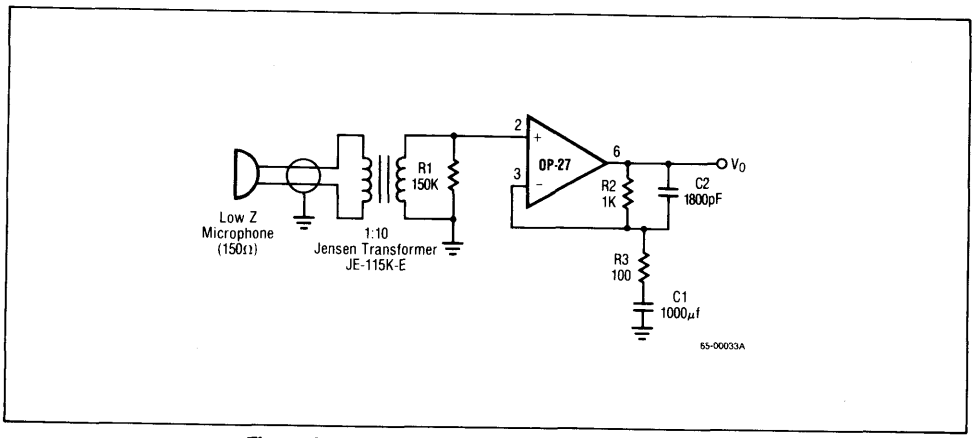


Figure 3. Low Impedance Microphone Preamplifier

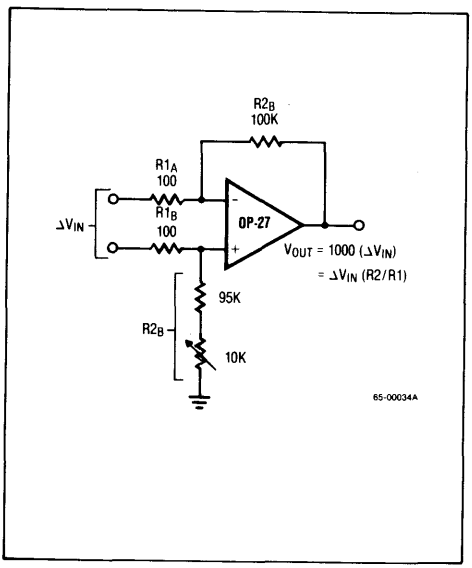
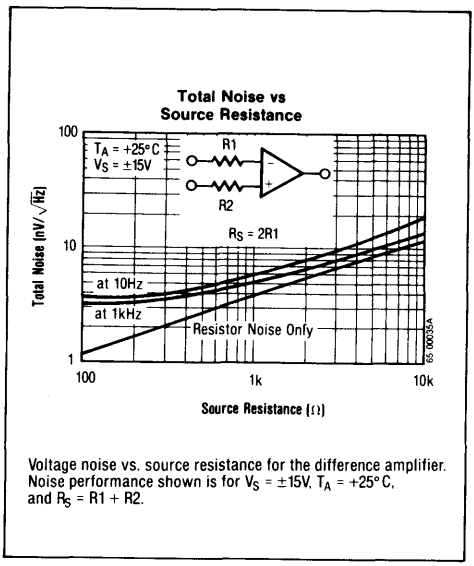


Figure 4. A Single Op Amp IC Difference Amplifier Using an OP-27. The Difference Amplifier is Connected for a Gain of 1000.



Voltage noise vs. source resistance for the difference amplifier. Noise performance shown is for V_S = ±15V, T_A = +25°C, and R_S = R1 + R2.

Figure 5. Total Noise vs. Source Resistance

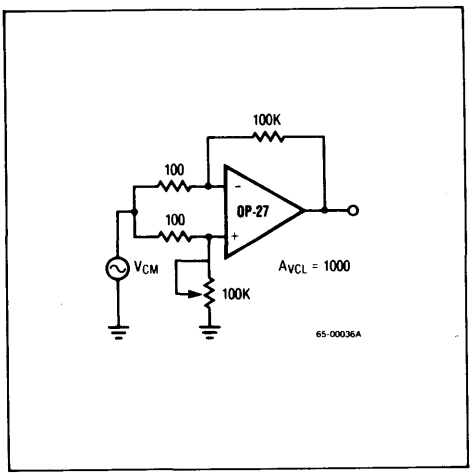


Figure 6. Common Mode Rejection Ratio Test Circuit

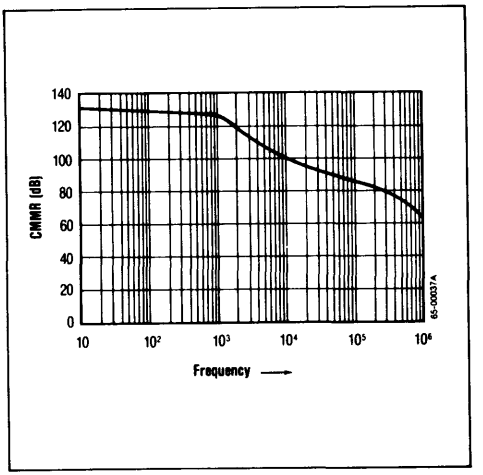


Figure 7. Common Mode Rejection Ratio vs. Frequency for the Circuit of Figure 4.

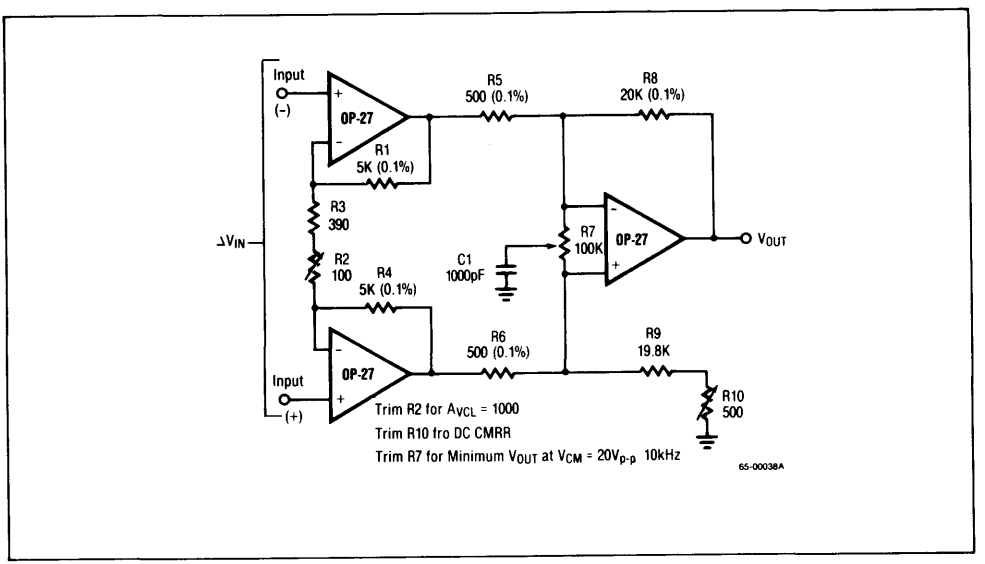


Figure 8. Three Op Amp IC Instrumentation Amplifier

Raytheon

Very Low Noise Operational Amplifier

OP-37

Features

- Very low noise
  Spectral noise density — $3nV/\sqrt{Hz}$
  1/f noise corner frequency — 2.7Hz
- Very low V_{OS} Drift
  0.2μV/Mo
  0.2μV/°C
- High gain — 1.8×10^6V/V
- High output drive capability — ±12V into 600Ω load
- High slew rate — 17V/μS
- Wide gain bandwidth product — 63MHz
- Good common mode rejectioni ratio — 126dB
- Low input offset voltage — 10μV
- Minimum low frequency noise — $0.8\mu V_{p-p}$ 0.1Hz to 10Hz
- Low input bias and offset currents — 10nA

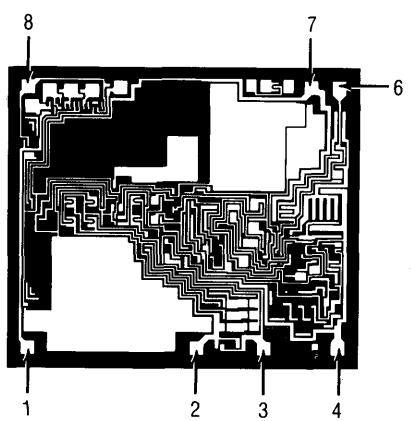
Description

The OP-37 is designed for instrumentation grade signal conditioning where low noise (both spectral density and burst), wide bandwidth, and high slew rate are required along with low input offset voltage, low input offset temperature coefficient, and low input bias currents in gains greater than or equal to ten. Digital nulling techniques performed at wafer sort make it feasible to guarantee temperature stable input offset voltages as low as 25μV. Input bias current cancellation techniques are used to obtain 10nA input bias currents.

The OP-37 is especially useful for instrumentation and professional quality audio applications in gains greater than or equal to ten. Applying the slew rate vs. power bandwidth equation ($fp = SR/2\pi V_p$), the OP-37 will have an undistorted output up to its power bandwidth frequency of 208kHz, with an undistorted output of $8V_{p-p}$ at 338kHz. This device provides performance adequate for the most demanding high fidelity applications.

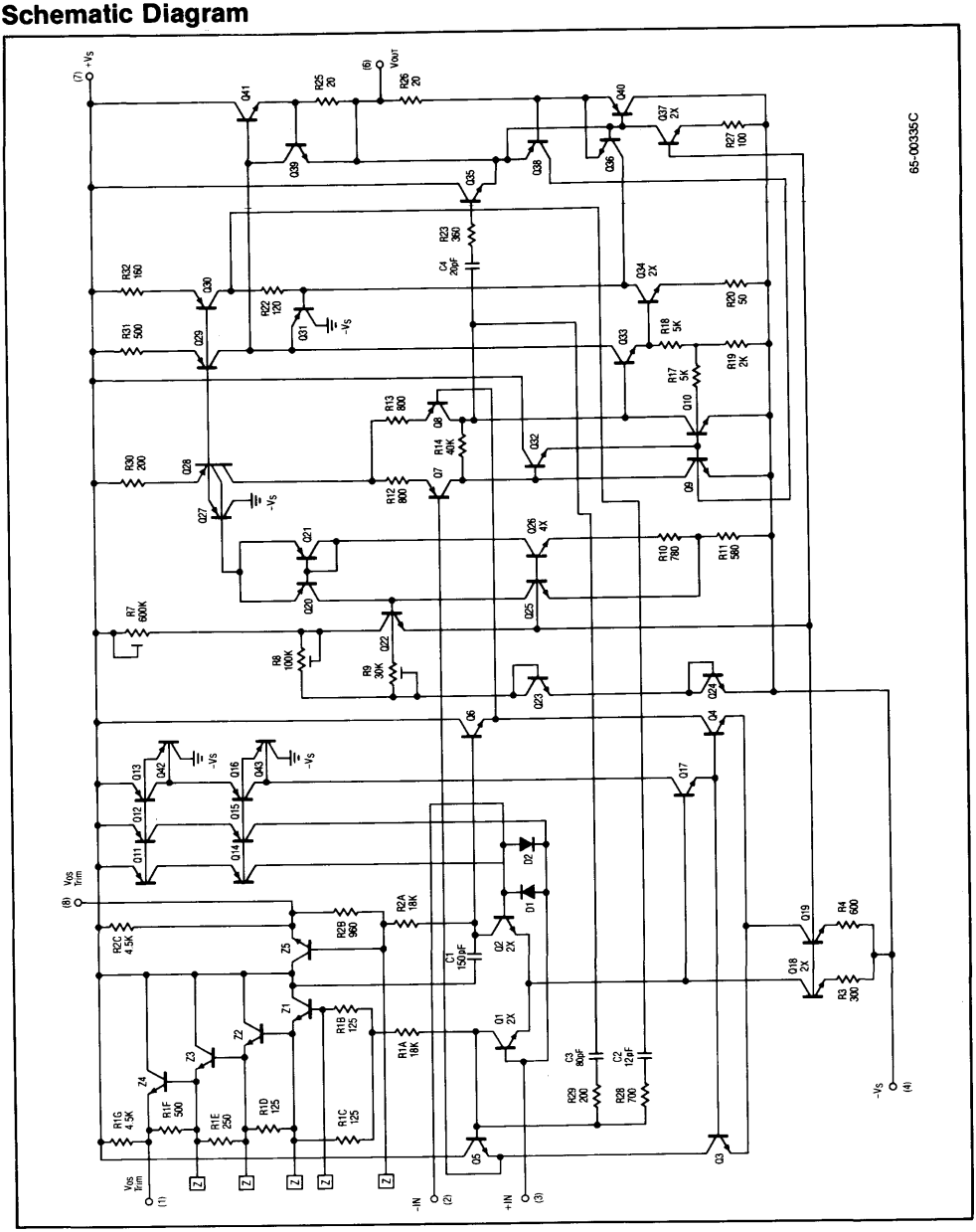
In addition to providing superior performance for the professional audio market, the OP-37 design uniquely addresses the needs of the instrumentation designer. Power supply rejection and common mode rejection are both typically 120dB. Input offset voltage can be externally trimmed without affecting input offset voltage drift with temperature or time. The drift performance is, in fact, so good that the system designer must be cautioned that stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals are enough to degrade its performance. For this reason it is also important to keep both input terminals at the same relative temperature. The well behaved temperature performance of the OP-37 has made it unnecessary to specify a commercial grade (0°C to +70°C). All grades of the OP-37 are specified to, at least, the industrial grade (-25°C to +85°C) temperature range.

Mask Pattern



Die Size: 85 x 98 mils
Min. Pad Dimensions: 4 x 4 mils

Schematic Diagram

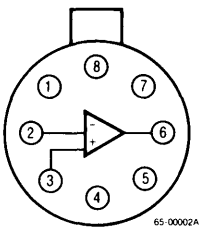


Very Low Noise Operational Amplifier

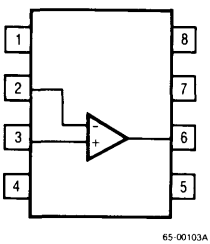
OP-37

Connection Information

TO-99
Metal Can
(Top View)



8-Lead
Ceramic Dual In-Line
(Top View)



Pin	Function
1	V_{OS} Trim
2	Inverting Input
3	Non-Inverting Input
4	$-V_S$
6	Output
7	$+V_S$
8	V_{OS} Trim

Absolute Maximum Ratings

Supply Voltage ..... +22V
Input Voltage[1] ..... ±22V
Differential Input Voltage 0.7V
Internal Power Dissipation 658mW
Output Short Circuit Duration ..... Indefinite
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
OP-27A/B/C ..... -55°C to +125°C
OP-27E/F/G ..... -25°C to +85°C
Lead Soldering Temperature
(60 Sec) ..... +300°C

Note: 1. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

Thermal Characteristics

	8-Lead Ceramic DIP	TO-99 8-Lead Metal Can
Max. Junction Temp.	175°C	175°C
Max. P_D T_A < 50°C	833mW	658mW
Therm. Res. θ_{JC}	45°C/W	50°C/W
Therm. Res. θ_{JA}	150°C/W	190°C/W
For T_A > 50°C Derate at	8.33mW per °C	5.26mW per °C

Ordering Information

Part Number	Package	Operating Temperature Range
OP-37EDE	Ceramic	-25°C to +85°C
OP-37ENB	Plastic	-25°C to +85°C
OP-37ET	TO-99	-25°C to +85°C
OP-37FDE	Ceramic	-25°C to +85°C
OP-37FNB	Plastic	-25°C to +85°C
OP-37FT	TO-99	-25°C to +85°C
OP-37GDE	Ceramic	-25°C to +85°C
OP-37GNB	Plastic	-25°C to +85°C
OP-37GT	TO-99	-25°C to +85°C
OP-37ADE	Ceramic	-55°C to +125°C
OP-37ADE/883B*	Ceramic	-55°C to +125°C
OP-37AT	TO-99	-55°C to +125°C
OP-37AT/883B*	TO-99	-55°C to +125°C
OP-37BDE	Ceramic	-55°C to +125°C
OP-37BDE/883B*	Ceramic	-55°C to +125°C
OP-37BT	TO-99	-55°C to +125°C
OP-37BT/883B*	TO-99	-55°C to +125°C
OP-37CDE	Ceramic	-55°C to +125°C
OP-37CDE/883B*	Ceramic	-55°C to +125°C
OP-37CT	TO-99	-55°C to +125°C
OP-37CT/883B*	TO-99	-55°C to +125°C

*MIL-STD-883, Level B Processing

Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	OP-37A/E			OP-37B/F			OP-37C/G			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[5]			10	25		20	60		30	100	μV
Long Term Input Offset Voltage Stability[1,2]			0.2	1.0		0.3	1.5		0.4	2.0	μV/Mo
Input Offset Current			7.0	35		9.0	50		12	75	nA
Input Bias Current			±10	±40		±12	±55		±15	±80	nA
Input Noise Voltage[2]	0.1Hz to 10Hz		0.08	0.18		0.08	0.18		0.09	0.25	μV_{p-p}
Input Noise Voltage Density[2]	f_0 = 10Hz		3.5	5.5		3.5	5.5		3.8	8.0	$\frac{nV}{\sqrt{Hz}}$
	f_0 = 30Hz		3.1	4.5		3.1	4.5		3.3	5.6	
	f_0 = 1000Hz		3.0	3.8		3.0	3.8		3.2	4.5	
Input Noise Current Density[2]	f_0 = 10Hz		1.7	4.0		1.7	4.0		1.7		$\frac{pA}{\sqrt{Hz}}$
	f_0 = 30Hz		1.0	2.3		1.0	2.3		1.0		
	f_0 = 1000Hz		0.4	0.6		0.4	0.6		0.4	0.6	
Input Resistance (Diff. Mode)[4]		1.5	6.0		1.2	5.0		0.8	4.0		MΩ
Input Resistance (Com. Mode)			3.0			2.5			2.0		GΩ
Input Voltage Range[3]		±11	±12.3		±11	±12.3		±11	±12.3		V
Common Mode Rejection Ratio	V_{CM} = ±11V	114	126		106	123		100	120		dB
Power Supply Rejection Ratio	V_S = ±4V to ±18V	100	120		100	120		94	118		dB
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_O = ±10V	1000	1800		1000	1800		700	1500		V/mV
	$R_L \geq 1k\Omega$, V_O = ±10V	800	1500		800	1500			1500		
	V_O = ±1V, V_S = ±4V[4]	250	700		250	700		200	500		
Output Voltage Swing	$R_L \geq 2k\Omega$	±12	±13.8		±12	±13.8		±11.5	±13.5		V
	$R_L \geq 600\Omega$	±11	±12		±11	±12		±11	±12		
Slew Rate[4]	$R_L \geq 2k\Omega$	11	17		11	17		11	17		V/μS
Gain Bandwidth Product[4]	f_0 = 10kHz	45	63		45	63		45	63		MHz
	f_0 = 1MHz		40			40			40		
Open Loop Output Resistance	V_O = 0, I_O = 0		70			70			70		Ω
Power Consumption			90	140		90	140		100	170	mW
Offset Adjustment Range	R_P = 10kΩ		±4.0			±4.0			±4.0		mV

Notes:
1. Long Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV.
2. This parameter is tested on a sample basis only, and guaranteed to an LTPD of 10.
3. Caution: The Common Mode Input Range is a function of supply voltage (see Typical Performance Curves). Also, the input protection diodes do not allow the device to be removed or inserted into the circuit without first removing power.
4. Parameter is guaranteed by design.
5. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

Electrical Characteristics (V_S = ±15V, -55°C ≤ T_A ≤ +125°C unless otherwise noted)

Parameters	Test Conditions	OP-37A			OP-37B			OP-37C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[1]			30	60		50	200		70	300	μV
Average Input Offset Drift[2]			0.2	0.6		0.3	1.3		0.4	1.8	μV/°C
Input Offset Current			15	50		22	85		30	135	nA
Input Bias Current			±20	±60		±28	±95		±35	±150	nA
Input Voltage Range		±10.3	±11.5		±10.3	±11.5		±10.2	±11.5		V
Common Mode Rejection Ratio	V_{CM} = ±10V	108	122		100	119		94	116		dB
Power Supply Rejection Ratio	V_S = ±4.5V to ±18V	96	116		94	114		86	110		dB
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_O = ±10V	600	1200		500	1000		300	800		V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	±11.5	±13.5		±11	±13.2		±10.5	±13		V

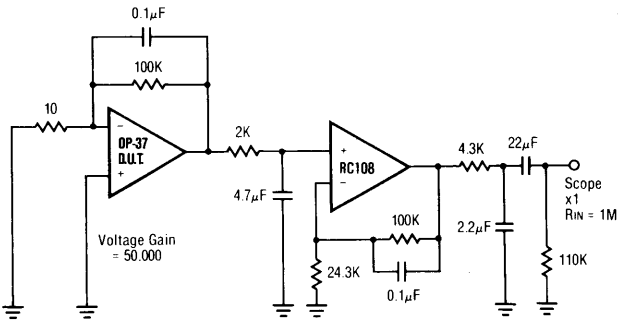
Electrical Characteristics (V_S = ±15V, -25°C ≤ T_A ≤ +85°C unless otherwise noted)

Parameters	Test Conditions	OP-37E			OP-37F			OP-37G			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[1]			20	50		40	140		55	220	μV
Average Input Offset Drift			0.2	0.6		0.3	1.3		0.4	1.8	μV/°C
Input Offset Current			10	50		14	85		20	135	nA
Input Bias Current			±14	±60		±18	±95		±25	±150	nA
Input Voltage Range		±10.5	±11.8		±10.5	±11.8		±10.5	±11.8		V
Common Mode Rejection Ratio	V_{CM} = ±10V	110	124		102	121		96	118		dB
Power Supply Rejection Ratio	V_S = ±4.5V to ±18V	97	118		96	116		90	114		dB
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_O = ±10V	750	1500		700	1300		450	1000		V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	±11.7	±13.6		±11.4	±13.5		±11	±13.3		V

Notes: 1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. $T_C V_{OS}$ performance is guaranteed unnulled or when nulled with R_P = 8.0kΩ to 20kΩ

Typical Performance Characteristics

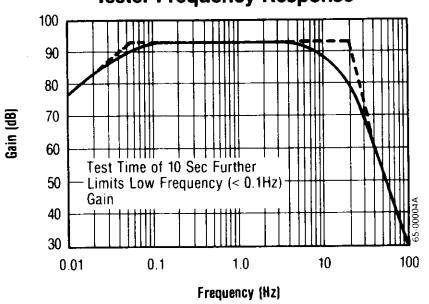
0.1Hz to 10Hz Noise Test Circuit



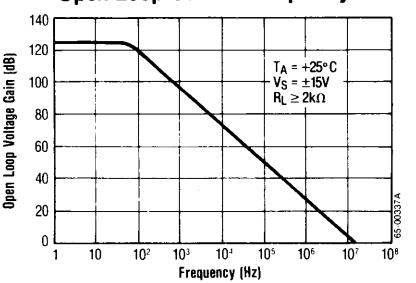
Note: All Capacitor values are for non polarized capacitors only

65-00336A

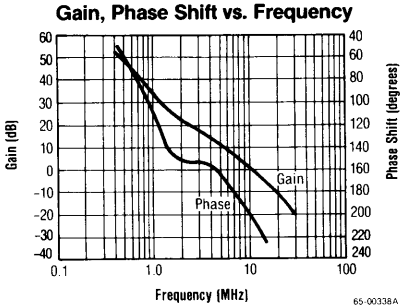
0.1Hz to 10Hz Peak-to-Peak Noise Tester Frequency Response



Open Loop Gain vs. Frequency

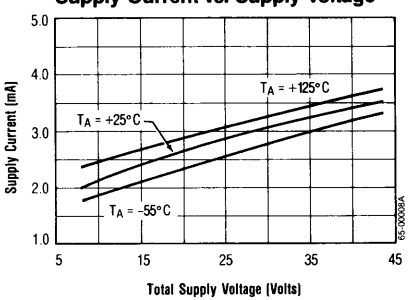


Gain, Phase Shift vs. Frequency



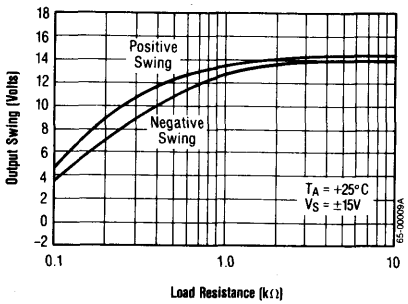
65-00338A

Supply Current vs. Supply Voltage

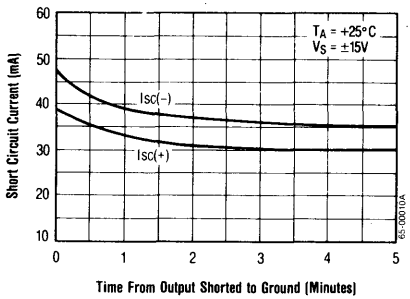


Typical Performance Characteristics (Continued)

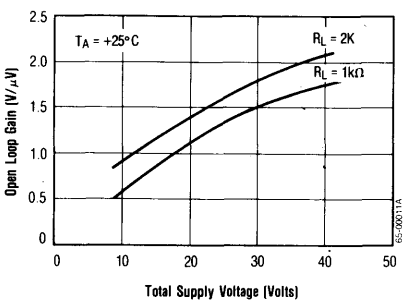
Maximum Output Swing vs. Resistive Load



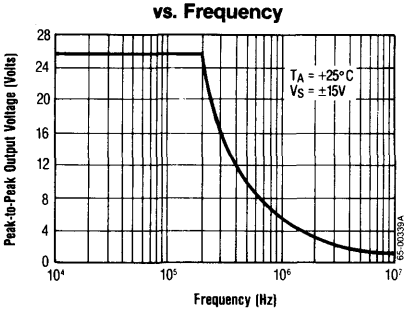
Short Circuit Current vs. Time



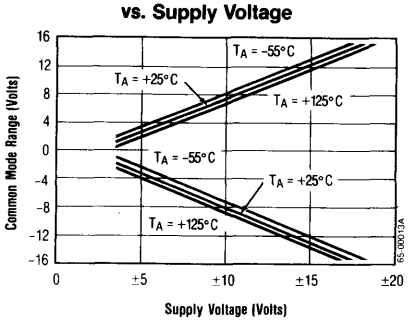
Open Loop Voltage Gain vs. Supply Voltage



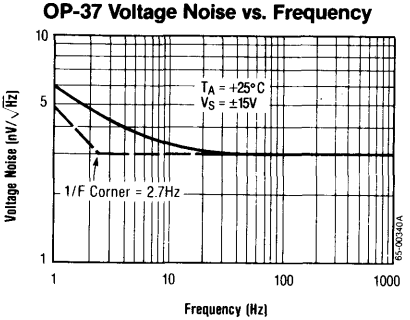
Maximum Undistorted Output vs. Frequency



Common Mode Input Range vs. Supply Voltage

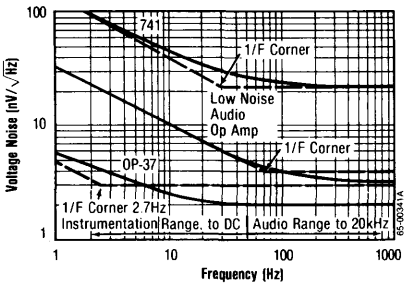


OP-37 Voltage Noise vs. Frequency

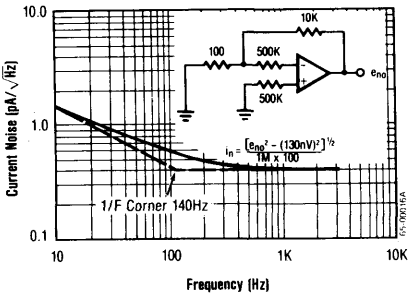


Typical Performance Characteristics (Continued)

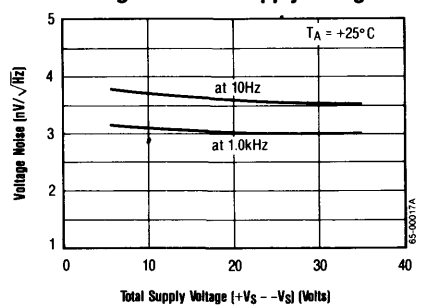
A Comparison of Op Amp Voltage Noise Spectrums



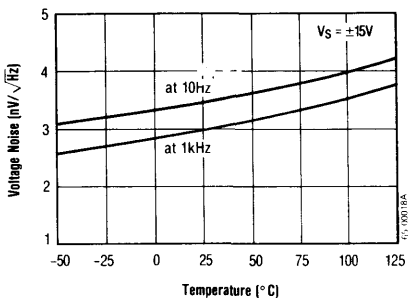
Current Noise vs. Frequency



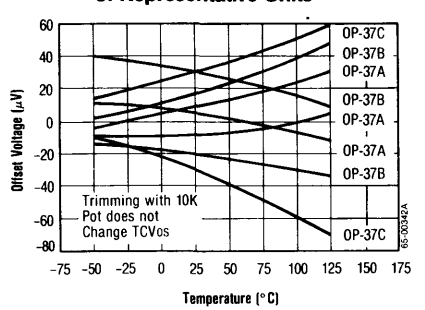
Voltage Noise vs. Supply Voltage



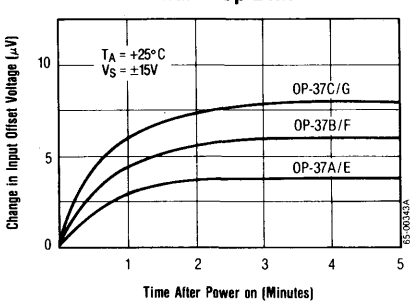
Voltage Noise vs. Temperature



Offset Voltage Drift of Representative Units

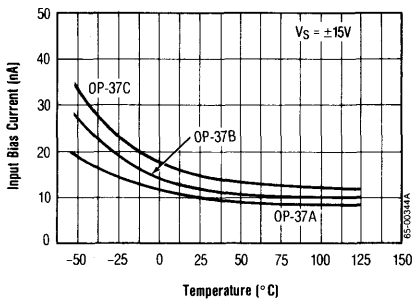


Warm-Up Drift

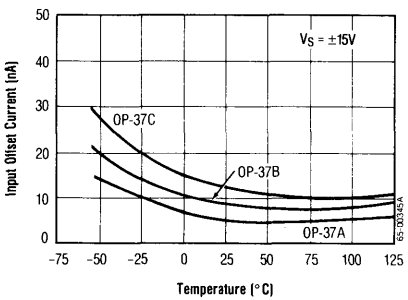


Typical Performance Characteristics (Continued)

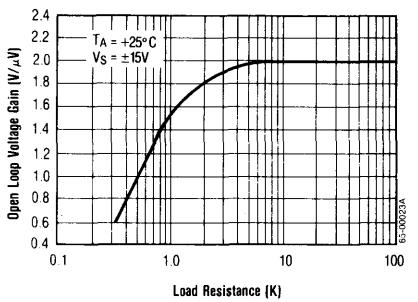
Input Bias Current vs. Temperature



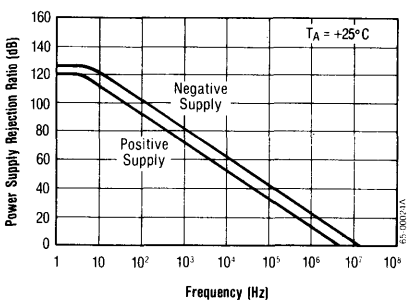
Input Offset Current vs. Temperature



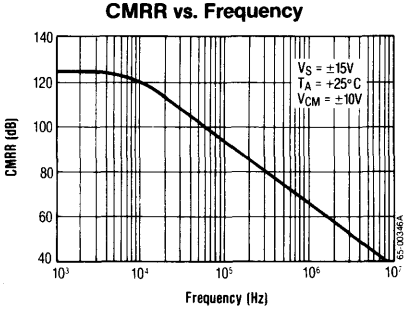
Open Loop Voltage Gain vs. Load Resistance



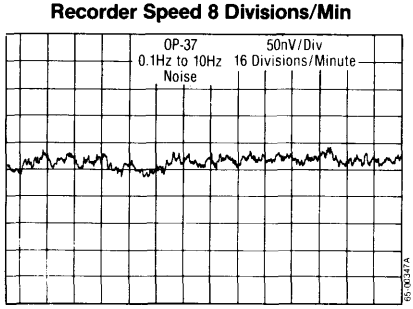
PSRR vs. Frequency



CMRR vs. Frequency

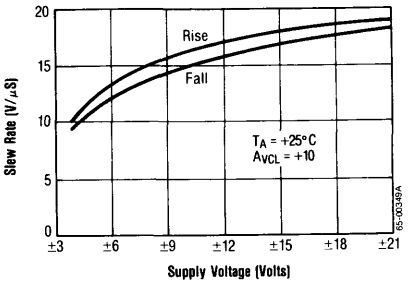


OP-37 0.1Hz to 10Hz Peak-to-Peak Noise Vertical Scale 50nV/Division Recorder Speed 8 Divisions/Min

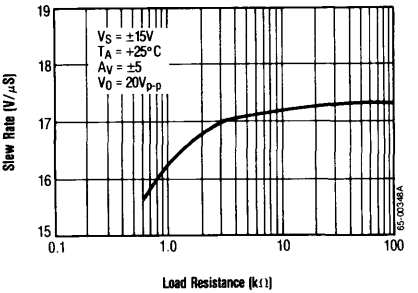


Typical Performance Characteristics (Continued)

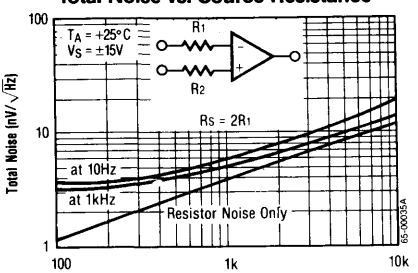
Slew Rate vs. Supply Voltage



Slew Rate vs. Load

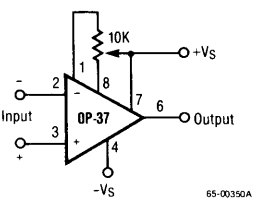


Total Noise vs. Source Resistance

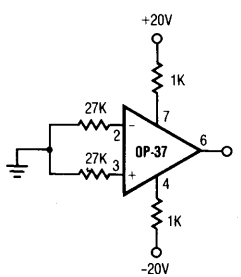


Voltage noise vs source resistance for the difference amplifier. Noise performance shown is for $V_S = \pm 15V$, $T_A = +25°C$, and $R_S = R_1 + R_2$

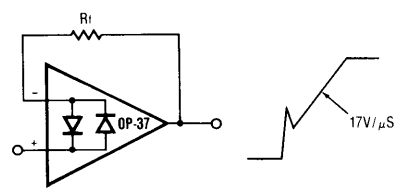
Offset Nulling Circuit



Burn-In Circuit



Large Signal Transient Response



When $R_1 \leq 100\Omega$ and the input is driven with a fast, large signal pulse ($\geq$ 1V), the output waveform will look as shown

Typical Applications

Low Impedance Microphone Preamp (Figure 1)

In this preamp the transformer converts the low microphone impedance up to a value that is close to the optimum source impedance required by the OP-37 for best noise performance. The optimum source impedance can be calculated as the ratio of e_n/i_n which for the OP-37 is approximately 7000Ω. Fortunately the noise performance does not degrade appreciably until the source impedance is four or five times this optimum value. The source impedance at the output of this transformer of 15kΩ still provides near optimum noise performance. (A high quality audio transformer with a step-up ratio of 6.7 to one is not available.) C1 rolls off the high frequency response at 90kHz giving a noise power bandwidth of 140kHz.

Instrumentation

The OP-37 is particularly adaptable to instrumentation applications. When wired into a single op amp difference amplifier configuration, the OP-37 exhibits outstanding common mode rejection ratio. The spot voltage noise is so low that it is dominated almost entirely by the resistor Johnson noise.

The three op amp instrumentation amplifier of Figure 4 avoids the low input impedance characteristics of difference amplifiers at the expense of two more operational amplifiers and a slight degradation in noise performance. The noise increases because two amplifiers are contributing to the input voltage spectral noise instead of one. Thus, the noise contribution, exclusive of resistor Johnson noise, increases by slightly more than the $\sqrt{2}$. The spectral noise voltage increases from approximately $3nV/\sqrt{Hz}$ to approximately $4.9nV/\sqrt{Hz}$, with the third amplifier contributing about 10% of the noise. The gain of the input amplifier is set at 25 and the second stage at 40 for an overall gain of 1000. R7 is trimmed to optimize the common mode rejection (CMRR) with frequency. With balanced source resistors a CMRR of 100dB is achieved. With a 1kΩ source impedance imbalance CMRR is degraded to 80dB at 5kHz due to the finite (3GΩ) input impedance.

D.A.C. Current to Voltage Converter

Many high speed voltage output D/A conversion applications require a high speed op amp to convert a standard current output DAC (such as a DAC-08 or DAC-10) to be voltage output. The OP-37 is ideal for this because it has the speed and settling time for fast data conversion, but still has excellent DC specifications to ensure high accuracy.

The current output of the DAC-10 feeds the summing junction of the OP-37. The amplifier feedback holds the summing junction at zero volts, so the current output can only flow through

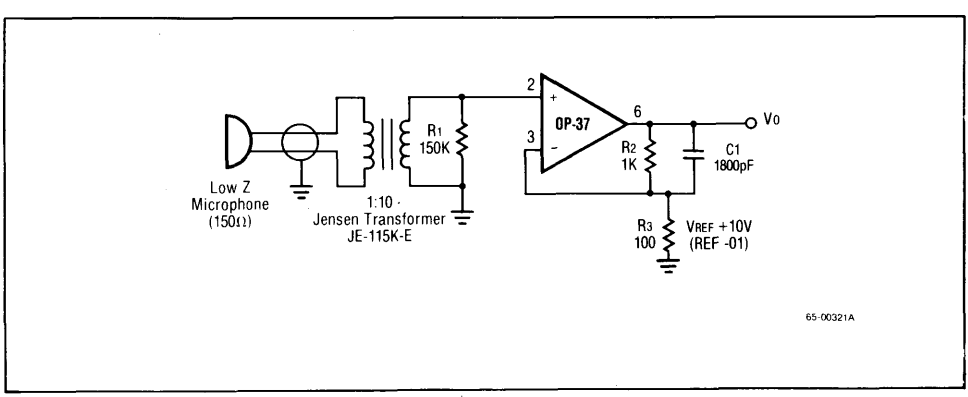


Figure 1. Low Impedance Microphone Preamplifier

the 2.5k feedback resistor. The full scale current output of 2mA times 2.5k equals a full scale output voltage of 10V. The 360Ω resistor is required to increase the effective gain of the OP-37 to meet the minimum gain requirement for stability. The high speed of the OP-37 allows a conversion time of 1μS to 1/2 LSB in this circuit. In addition, the low V_{OS} and V_{OS} drift of the OP-37 complements the high accuracy of the DAC-10, and the high output drive capability allows connection to demanding loads.

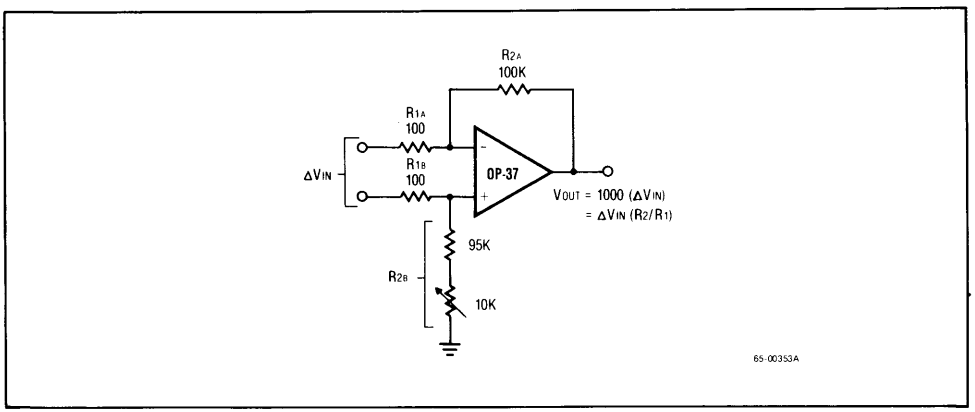


Figure 2. A Single Op Amp IC Difference Amplifier Using an OP-37. The Difference Amplifier is Connected for a Gain of 1000.

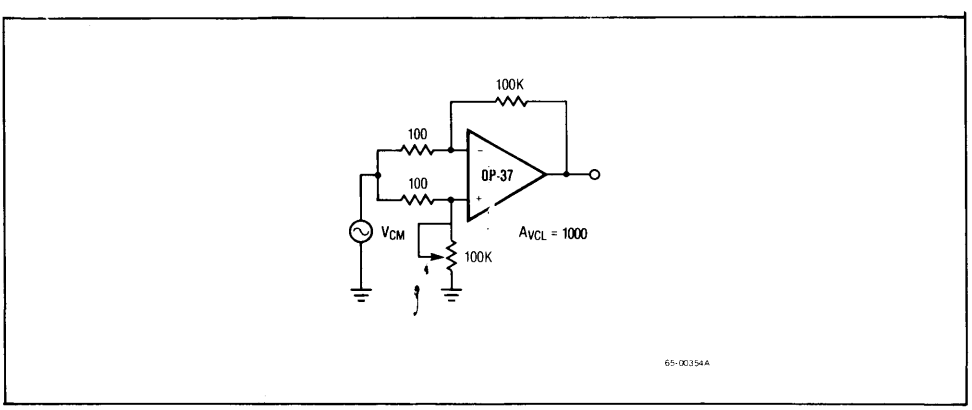


Figure 3. Common Mode Rejection Ratio Test Circuit

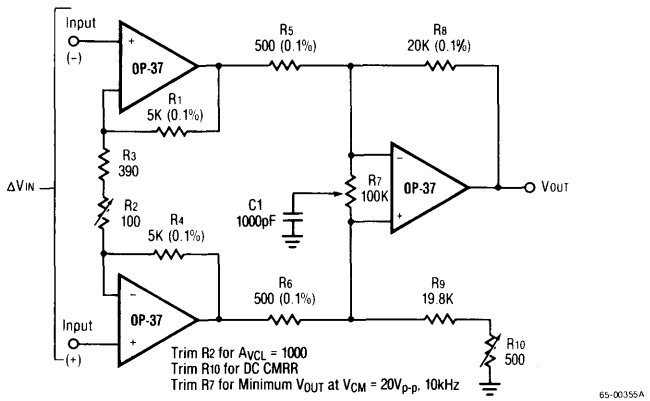


Figure 4. Three Op Amp IC Instrumentation Amplifier

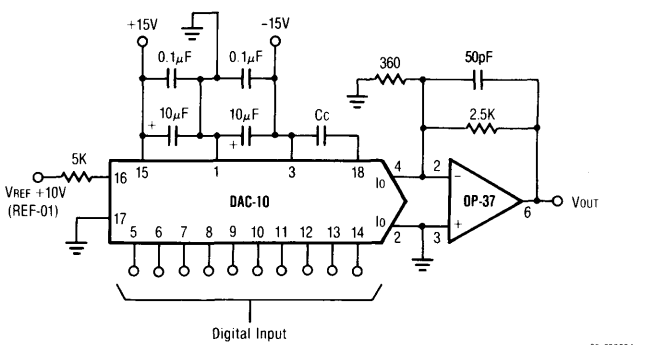


Figure 5. D/A Converter Application

Raytheon

Very Low Noise Operational Amplifier

OP-47

Features

- Very low noise
  Spectral noise density — $3nV/\sqrt{Hz}$
  1/f noise corner frequency — 2.7Hz
- Very low V_{OS} drift
  0.2μV/Mo
  0.2μV/°C
- High gain — 1.8×10^6V/V
- High output drive capability — ±12V into 600Ω load
- High slew rate — 50V/μS (A_{VCL} > 400)
- Wide gain bandwidth product — 70MHz
- Good common mode rejection ratio — 126dB
- Low input offset voltage — 20μV
- Minimum low frequency noise — $0.08\mu V_{p-p}$
  0.1Hz to 10Hz
- Low input bias and offset currents — 10nA

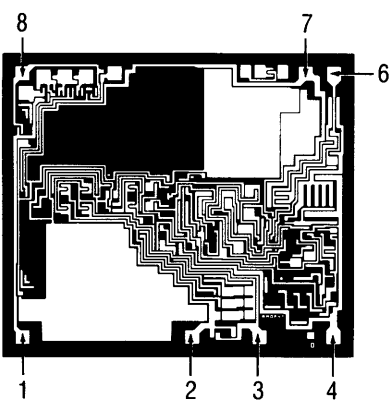
Description

The OP-47 is designed for instrumentation grade signal conditioning where low noise (both spectral density and burst), wide bandwidth, and high slew rate are required along with low input offset voltage, low input offset temperature coefficient, and low input bias currents in gains greater than or equal to 400. Digital nulling techniques performed at wafer sort make it feasible to guarantee temperature stable input offset voltages as low as 60μV. Input bias current cancellation techniques are used to obtain 10nA input bias currents.

The OP-47 is especially useful for instrumentation and professional quality audio applications in gains greater than or equal to 400. Applying the slew rate vs. power bandwidth equation ($fp = SR/2\pi V_p$) the OP-47 will have an undistorted output at $8V_{p-p}$ of 900kHz. This device provides performance adequate for the most demanding high fidelity applications.

In addition to providing superior performance for the professional audio market the OP-47 design uniquely addresses the needs of the instrumentation designer. Power supply rejection and common mode rejection are both typically 120dB. Input offset voltage can be externally trimmed without affecting input offset voltage drift with temperature or time. The drift performance is, in fact, so good that the system designer must be cautioned that stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals are enough to degrade its performance. For this reason it is also important to keep both input terminals at the same relative temperature.

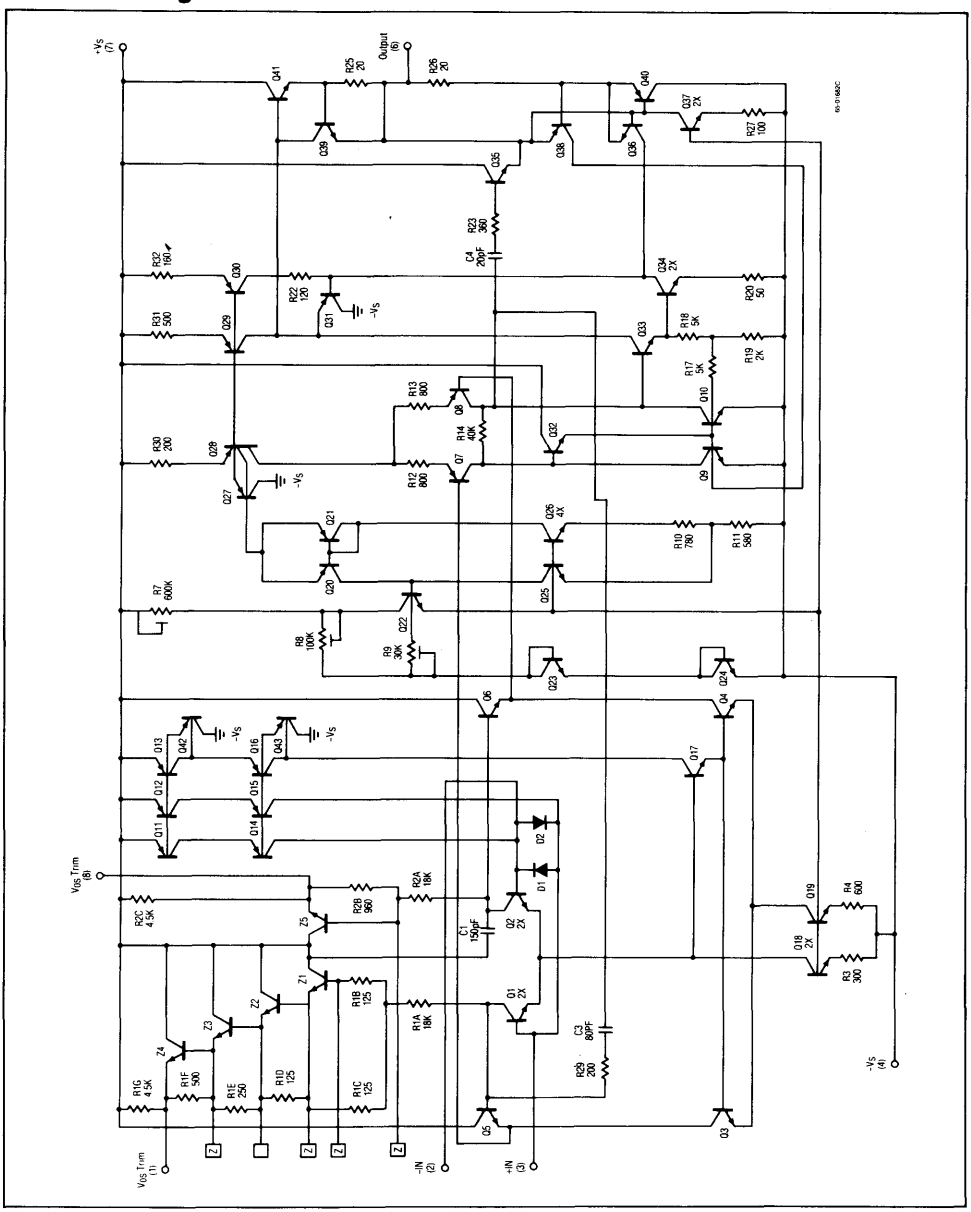
Mask Pattern



65-01681A

Die Size: 85 x 98 mils
Min. Pad Dimensions: 4 x 4 mils

Schematic Diagram

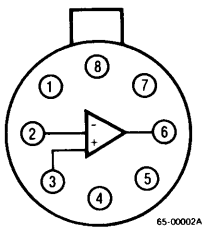


Very Low Noise Operational Amplifier

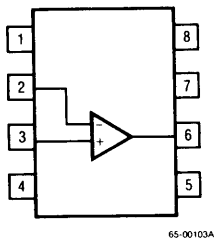
OP-47

Connection Information

8-Lead TO-99 Metal Can



8-Lead Plastic Dual In-Line



Pin	Function
1	V_{OS} Trim
2	Inverting Input
3	Non-Inverting Input
4	$-V_S$
6	Output
7	$+V_S$
8	V_{OS} Trim

Absolute Maximum Ratings

Supply Voltage ..... +22V
Input Voltage ..... ±22V
Differential Input Voltage 0.7V
Internal Power Dissipation 500mW
Output Short Circuit Duration ..... Indefinite
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
OP-47B ..... -55°C to +125°C
OP-47F/G ..... 0°C to +70°C
Lead Soldering Temperature
(60 Sec.) ..... +300°C

Note: 1. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

Thermal Characteristics

	TO-99 8-Lead Metal Can	8-Lead Plastic Dip
Max. Junction Temp.	175°C	125°C
Max. P_D T_A < 50°C	658mW	468mW
Therm. Res. θ_{JC}	50°C/W	
Therm. Res. θ_{JA}	190°C/W	160°C/W
For T_A > 50°C Derate at	5.26mW per °C	6.25mW per °C

Ordering Information

Part Number	Package	Operating Temperature Range
OP-47GT	TO-99	0°C to +70°C
OP-47FT	TO-99	0°C to +70°C
OP-47GNB	Plastic	0°C to +70°C
OP-47BT	TO-99	-55°C to +125°C
OP-47BT/883B*	TO-99	-55°C to +125°C

*MIL-STD-883, Level B Processing

Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	OP-47B/F			OP-47G			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[5]			20	60		30	100	μV
Long Term Input Offset Voltage Stability[1,2]			0.3	1.5		0.4	2.0	μV/Mo
Input Offset Current			9.0	50		12	75	nA
Input Bias Current			±12	±55		±15	±80	nA
Input Noise Voltage[2]	0.1Hz to 10Hz		0.08	0.18		0.09	0.25	μV_{p-p}
Input Noise Voltage Density[2]	f_O = 10Hz		3.5	5.5		3.8	8.0	$\frac{nV}{\sqrt{Hz}}$
	f_O = 30Hz		3.1	4.5		3.3	5.6	
	f_O = 1000Hz		3.0	3.8		3.2	4.5	
Input Noise Current Density[2]	f_O = 10Hz		1.7	4.0		1.7		$\frac{pA}{\sqrt{Hz}}$
	f_O = 30Hz		1.0	2.3		1.0		
	f_O = 1000Hz		0.4	0.6		0.4	0.6	
Input Resistance (Differential Mode)[4]		1.2	5.0		0.8	4.0		MΩ
Input Resistance (Common Mode)			2.5			2.0		GΩ
Input Voltage Range[3]		±11	±12.3		±11	±12.3		V
Common Mode Rejection Ratio	V_{CM} = ±11V	106	123		100	120		dB
Power Supply Rejection Ratio	V_S = ±4V to ±18V	100	120		94	118		dB
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_O = ±10V	1000	1800		700	1500		V/mV
	$R_L \geq 1k\Omega$, V_O = ±10V	800	1500			1500		
	V_O = ±1V, V_S = ±4V[4]	250	700		200	500		
Output Voltage Swing[6]	$R_L \geq 2k\Omega$	±12	±13.8		±11.5	±13.5		V
	$R_L \geq 600\Omega$	±11	±12		±11	±12		
Slew Rate[4]	$R_L \geq 2k\Omega$	25	50		25	50		V/μS
Gain Bandwidth Product[4]	f_O = 10kHz	45	70		45	70		MHz
	f_O = 1MHz		45			45		
Open Loop Output Resistance	V_O = 0, I_O = 0		70			70		Ω
Power Consumption			90	140		100	170	mW
Offset Adjustment Range	R_P = 10kΩ		±4.0			±4.0		mV

Notes:
1. Long term input offset voltage stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV.
2. This parameter is tested on a sample basis only, and guaranteed to an LTPD of 10.
3. Caution the common mode input range is a function of supply voltage, see typical performance curves. Also, the input protection diodes do not allow the device to be removed or inserted into the circuit without first removing power.
4. Parameter is guaranteed by design and is not tested.
5. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
6. CAUTION: positive output voltage swing should never exceed the minimum specified limits or large oscillation voltages will occur.

Electrical Characteristics (V_S = ±15V, -55°C ≤ T_A ≤+125°C unless otherwise noted)

Parameters	Test Conditions	OP-47B			Units
		Min	Typ	Max	
Input Offset Voltage[1]			50	200	μV
Average Input Offset Voltage Drift[2]			0.3	1.3	μV/°C
Input Offset Current			22	85	nA
Input Bias Current			±28	±95	nA
Input Voltage Range		±10.3	±11.5		V
Common Mode Rejection Ratio	V_{CM} = ±10V	100	119		dB
Power Supply Rejection Ratio	V_S = ±4.5V to ±18V	94	114		dB
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_O = ±10V	500	1000		V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	±11	±13.2		V

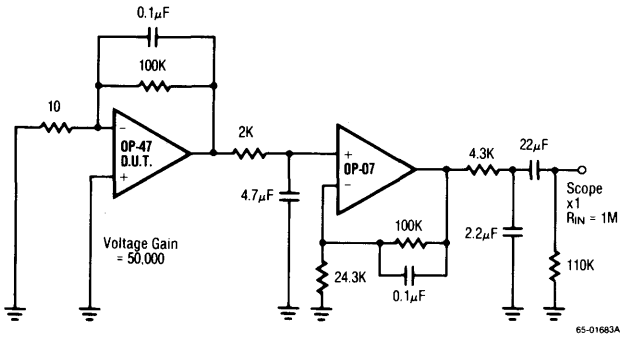
Electrical Characteristics (V_S = ±15V, 0°C ≤ T_A ≤ +70°C unless otherwise noted)

Parameters	Test Conditions	OP-47F			OP-47G			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[1]			40	140		55	220	μV
Average Input Offset Voltage Drift			0.3	1.3		0.4	1.8	μV/°C
Input Offset Current			14	85		20	135	nA
Input Bias Current			±18	±95		±25	±150	nA
Input Voltage Range		±10.5	±11.8		±10.5	±11.8		V
Common Mode Rejection Ratio	V_{CM} = ±10V	102	121		96	118		dB
Power Supply Rejection Ratio	V_S = ±4.5V to ±18V	96	116		90	114		dB
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_O = ±10V	700	1300		450	1000		V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	±11.4	±13.5		±11.0	±13.3		V

Notes: 1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. $T_C V_{OS}$ performance is guaranteed unnulled or when nulled with R_P = 8kΩ to 20kΩ.

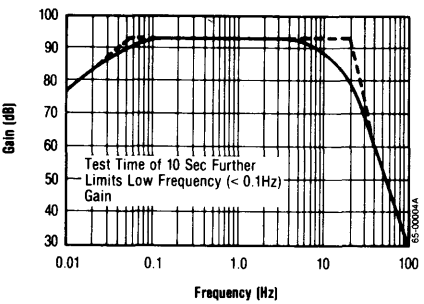
Typical Performance Characteristics

0.1Hz to 10Hz Noise Test Circuit

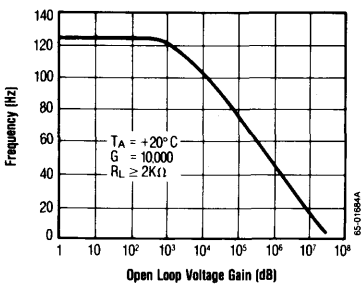


Note: All Capacitor values are for non polarized capacitors only

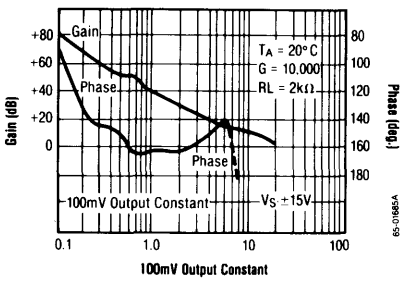
0.1Hz to 10Hz Peak-to-Peak Noise Tester Frequency Response



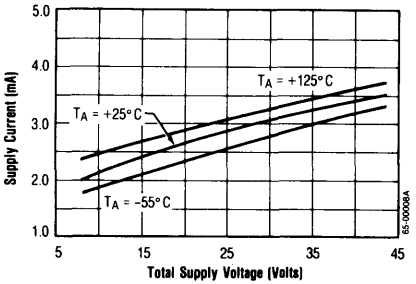
Open Loop Gain vs. Frequency



Gain and Phase Shift vs. Frequency

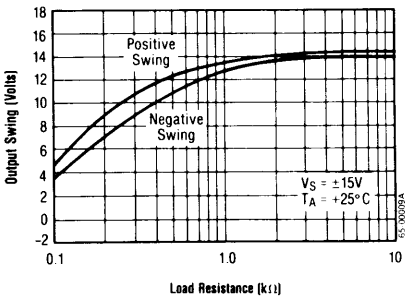


Supply Current vs. Supply Voltage

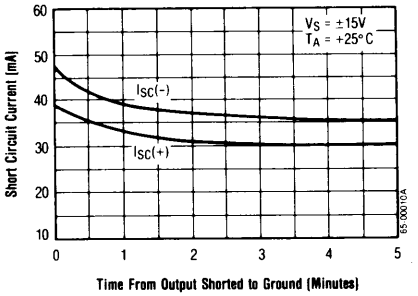


Typical Performance Characteristics (Continued)

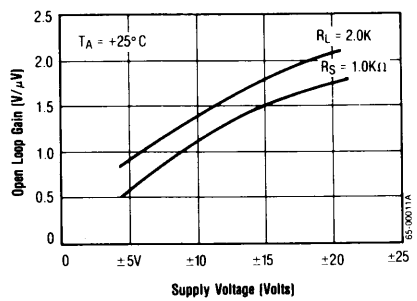
Maximum Output Swing vs. Resistive Load



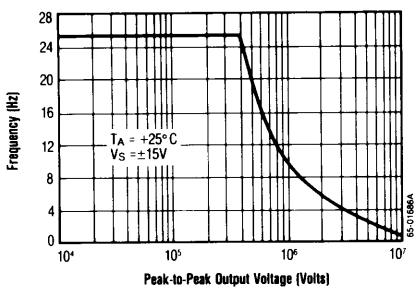
Short Circuit Current vs. Time



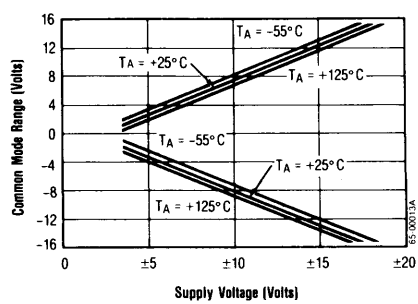
Open Loop Voltage Gain vs. Supply Voltage



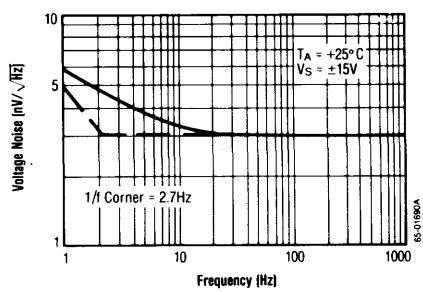
Maximum Undistorted Output vs. Frequency



Common Mode Input Range vs. Supply Voltage

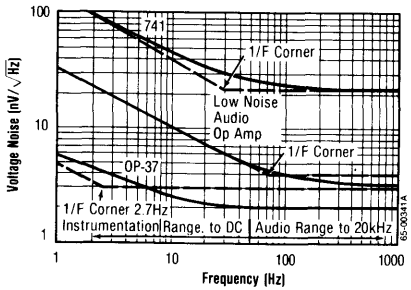


OP-47 Voltage Noise vs. Frequency

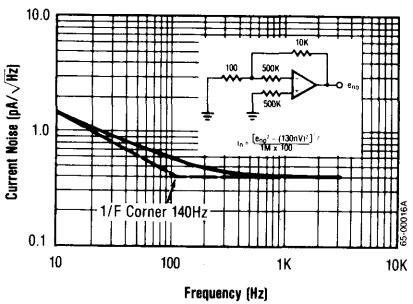


Typical Performance Characteristics (Continued)

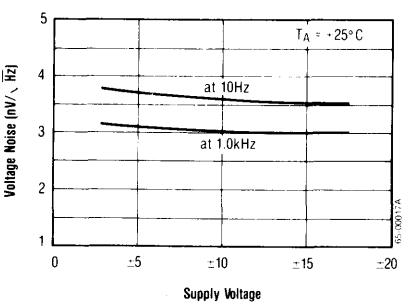
A Comparison of Op Amp Voltage Noise Spectrums



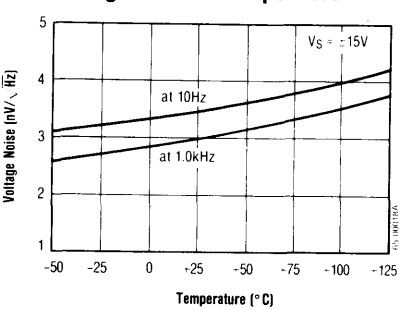
Current Noise vs. Frequency



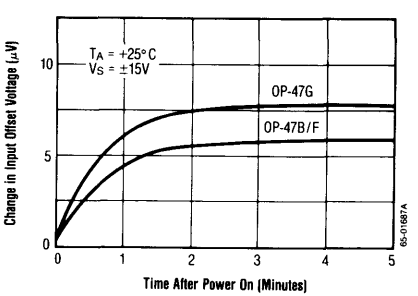
Voltage Noise vs. Supply Voltage



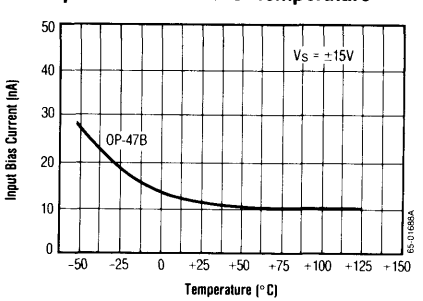
Voltage Noise vs. Temperature



Warm-Up Drift

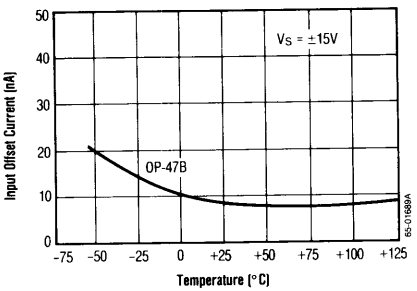


Input Bias Current vs. Temperature

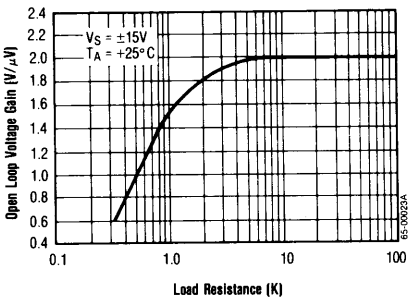


Typical Performance Characteristics (Continued)

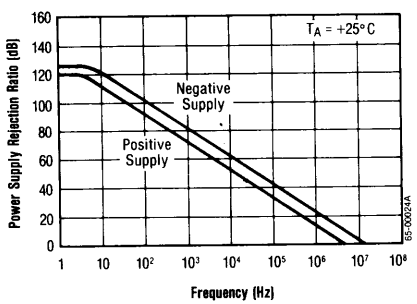
Input Offset Current vs. Temperature



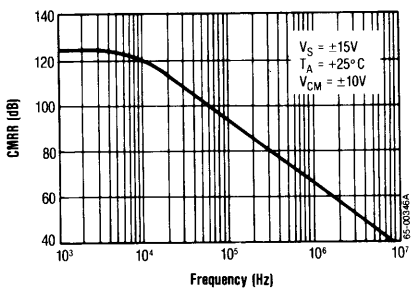
Open Loop Voltage Gain vs. Load Resistance



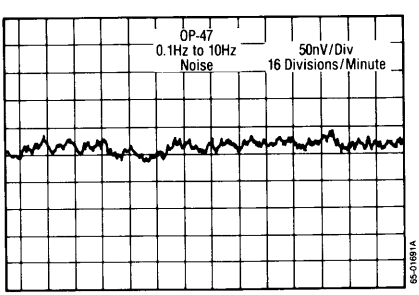
PSRR vs. Frequency



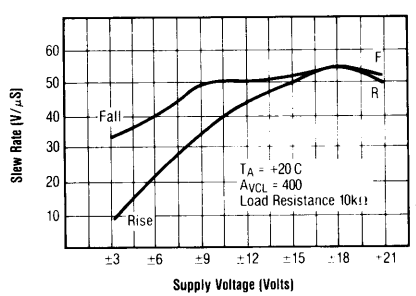
CMRR vs. Frequency



OP-47 0.1Hz to 10Hz Peak-to-Peak Noise
Vertical Scale 50nV/Division
Recorder Speed 8 Divisions/Min

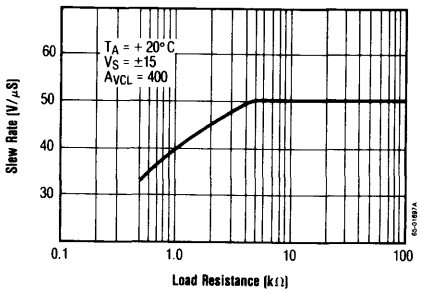


Supply Voltage vs. Slew Rate

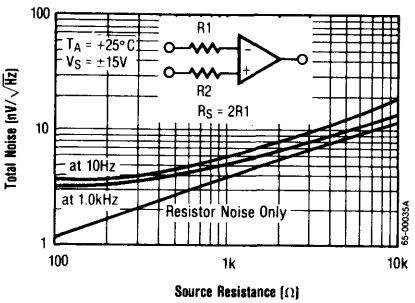


Typical Performance Characteristics (Continued)

Load Resistance vs. Slew Rate

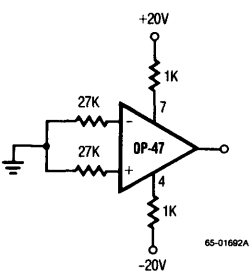


Total Noise vs. Source Resistance

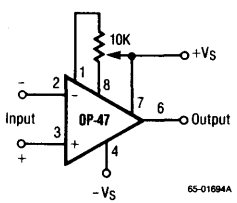


Voltage noise vs source resistance for the difference amplifier. Noise performance shown is for V_S = ±15V, T_A = +25°C, and $R_S = R_1 + R_2$

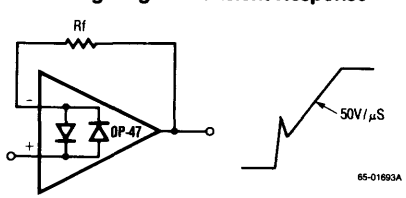
Burn-In Circuit



Offset Nulling Circuit



Large Signal Transient Response



When Rf ≤ 100Ω and the input is driven with a fast, large signal pulse (≥ 1V), the output waveform will look as shown.

Typical Applications

Low Impedance Microphone Preamp (Figure 1)
In this preamp the transformer converts the low microphone impedance up to a value that is close to the optimum source impedance required by the OP-47 for best noise performance. The optimum source impedance can be calculated as the ratio of e_n/i_n which for the OP-47 is approximately 7000Ω. Fortunately the noise performance does not degrade appreciably until the source impedance is four or five times this optimum value. The source impedance at the output of this transformer of 15kΩ still provides near optimum noise performance. (A high quality audio transformer with a step up ratio of 6.7 to one is not available.) C1 rolls off the high frequency response at 90kHz giving a power bandwidth of 140kHz.

Instrumentation
The OP-47 is particularly adaptable to instrumentation applications. When wired into a single op amp difference amplifier configuration, the OP-47 exhibits outstanding common mode rejection ratio. The spot voltage noise is so low that it is dominated almost entirely by the resistor Johnson noise.

The three op amp instrumentation amplifier of Figure 2 avoids the low input impedance characteristics of difference amplifiers. The noise increases because two amplifiers are contributing to the input voltage spectral noise. The noise contribution, exclusive of resistor Johnson noise, increases by slightly more than the $\sqrt{2}$. The spectral noise voltage increases from approximately $3nV/\sqrt{Hz}$ to approximately $4.9nV/\sqrt{Hz}$, with the third amplifier contributing about 10% of the noise. The gain of the input amplifier is set at 25 and the second stage at 400 for an overall gain of 10000. R7 is trimmed to optimize the common mode rejection (CMRR) with frequency. With balanced source resistors a CMRR of 100dB is achieved. With a 1kΩ source impedance imbalance CMRR is degraded to 80dB at 5kHz due to the finite (3GΩ) input impedance.

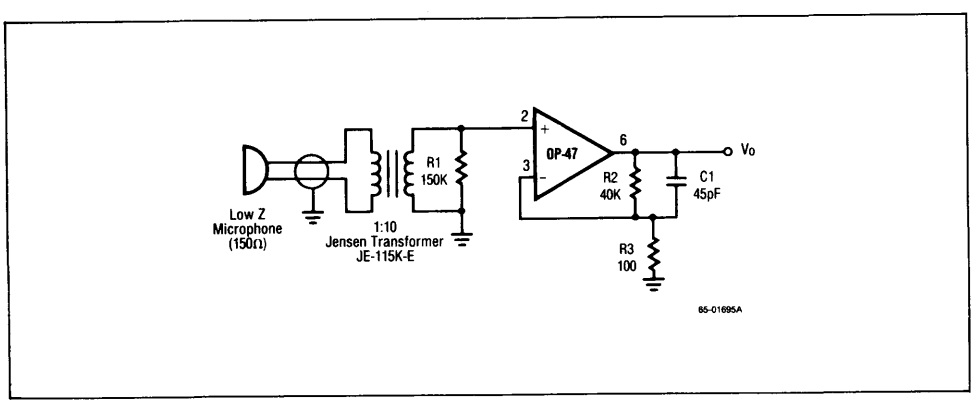


Figure 1. Low Impedance Microphone Preamplifier

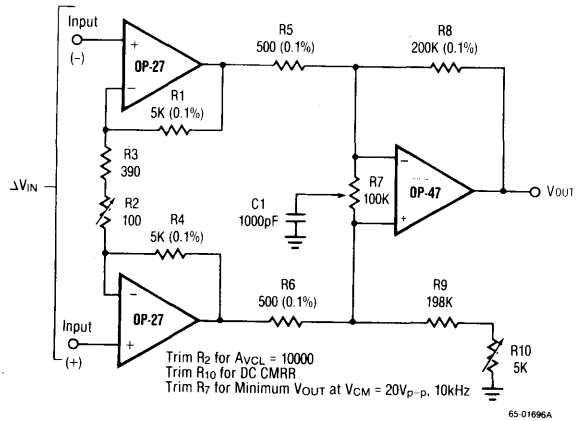


Figure 2. Three Op Amp IC Instrumentation Amplifier

Raytheon

Instrumentation Grade Operational Amplifier

RC714

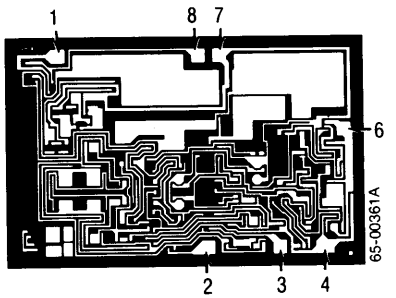
Features

- Low noise 0.1Hz to 10Hz — 0.35μV_{p-p}
- Ultra-low V_{OS} — 30μV
- Ultra-low V_{OS} drift — 0.3$\mu V/°C$
- Fits 725, 108A, 741, AD510 sockets
- Long term stability — 0.2μV/Mo

Description

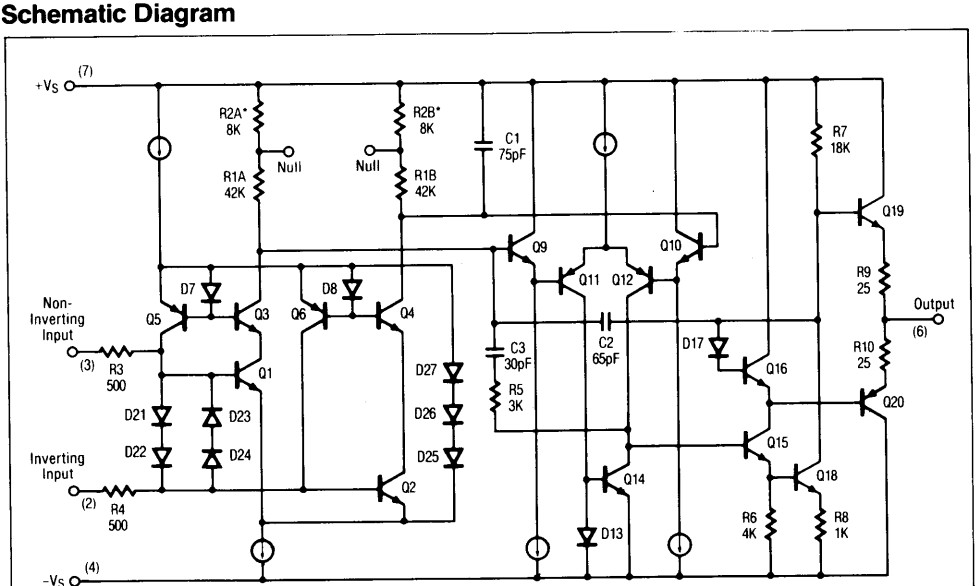
The RC/RM714 amplifier is designed for precision low level signal conditioning where ultra low V_{OS} and TCV_{OS} are required along with very low bias currents. Internal compensation eliminates the need for external components. Novel circuit design and tight process controls are used to obtain very low values of V_{OS}. V_{OS} is further reduced by a computer controlled digital nulling technique at test. Low frequency noise is minimized. Internal biasing techniques reduce external bias and offset currents to values in the order of ±1nA over the military temperature range. The 714 is a direct replacement for the OP-07, 108A, 725 and 5507. It can replace chopper stabilized amplifiers in many applications.

Mask Pattern



Die Size: 65 x 101 mils
Min. Pad Dimensions: 4 x 4 mils

Schematic Diagram

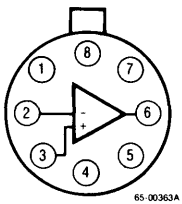


*R2A and R2B are electronically adjusted during factory test for minimum V_{OS}.

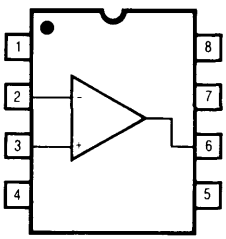
65-00362B

Connection Information

TO-99
Metal Can Package
(Top View)



8-Lead Ceramic
Dual In-Line Package
(Top View)



Pin	Function
1	V_{OS} Trim
2	Inverting Input
3	Non-Inverting Input
4	$-V_S$
5	NC
6	Output
7	$+V_S$
8	V_{OS} Trim

Thermal Characteristics

	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can
Max. Junction Temp.	175°C	175°C
Max. P_D T_A < 50°C	833mW	658mW
Therm. Res. θ_{JC}	45°C/W	50°C/W
Therm. Res. θ_{JA}	150°C/W	190°C/W
For T_A > 50°C Derate at	8.33mW per °C	5.26mW per °C

Ordering Information

Part Number	Package	Operating Temperature Range
RC714CDE	Ceramic	0°C to +70°C
RC714EDE	Ceramic	0°C to +70°C
RC714LDE	Ceramic	0°C to +70°C
RC714CH	TO-99	0°C to +70°C
RC714EH	TO-99	0°C to +70°C
RC714LH	TO-99	0°C to +70°C
RM714DE	Ceramic	-55°C to +125°C
RM714DE/883B*	Ceramic	-55°C to +125°C
RM714H	TO-99	-55°C to +125°C
RM714H/883B*	TO-99	-55°C to +125°C

*MIL-STD-883, Level B Processing

Absolute Maximum Ratings

Supply Voltage ..... ±22V
Input Voltage[1] ..... ±22V
Differential Input Voltage ..... +30V
Internal Power Dissipation[2] 500mW
Output Short Circuit Duration ..... Indefinite
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
RM714 ..... -55°C to +125°C
RC714E/C/L ..... 0°C to +70°C
Lead Soldering Temperature
(60 Sec) ..... +300°C

Notes: 1. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
2. See Thermal Characteristics Table.

Electrical Characteristics (V_S = ±15V and T_A = +25° C unless otherwise noted)

Parameters	Test Conditions	RM714 Min	RM714 Typ	RM714 Max	Units
Input Offset Voltage[4]			30	75	μV
Long Term Input Offset Voltage Stability[1,2]			0.2	1.0	μV/Mo
Input Offset Current			0.4	2.8	nA
Input Bias Current			±1.0	±3.0	nA
Input Noise Voltage[2]	0.1Hz to 10Hz		0.35	0.6	μV_{p-p}
Input Noise Voltage Density[2]	f_0 = 10Hz		10.3	18	$\frac{nV}{\sqrt{Hz}}$
	f_0 = 100Hz		10	13	
	f_0 = 1000Hz		9.6	11	
Input Noise Current[2]	0.1Hz to 10Hz		14	30	pA_{p-p}
Input Noise Current Density[2]	f_0 = 10Hz		0.32	0.80	$\frac{pA}{\sqrt{Hz}}$
	f_0 = 100Hz		0.14	0.23	
	f_0 = 1000Hz		0.12	0.17	
Input Resistance (Differential Mode)[3]		20	60		MΩ
Input Voltage Range		±13	±14		V
Common Mode Rejection Ratio	V_{CM} = ±13V	110	126		dB
Power Supply Rejection Ratio	V_S = ±3V to ±18V	100	110		dB
Large Signal Voltage Gain[3]	$R_L \geq 2k\Omega$, V_0 = ±10V	200	500		V/mV
	$R_L \geq 500\Omega$, V_0 = ±0.5V, V_S = ±3V	150	500		
Output Voltage Swing	$R_L \geq 10k\Omega$	±12.5	±13		V
	$R_L \geq 2k\Omega$	±12	±12.8		
	$R_L \geq 1k\Omega$	±10.5	±12		
Slew Rate	$R_L \geq 2k\Omega$	0.1	0.17		V/μS
Unity Gain Bandwidth			0.5		MHz
Open Loop Output Resistance	V_0 = 0, I_0 = 0		60		Ω
Power Consumption	V_S = ±15V		75	120	mW
	V_S = ±3V		4.0	6.0	
Offset Adjustment Range	R_P = 20kΩ		±4.0		mV

Notes:
1. Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV.
2. This parameter is tested on a sample basis only, and guaranteed to an LTPD of 10.
3. Guaranteed by design.
4. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

Electrical Characteristics (Continued)

(V_S = ±15V and -55°C ≤ T_A ≤ +125°C unless otherwise noted)

Parameters	Test Conditions	RM714			Units
		Min	Typ	Max	
Input Offset Voltage[2]			60	200	μV
Average Input Offset Voltage Drift[1]					μV/°C
Without External Trim			0.3	1.3	
With External Trim	R_P = 20kΩ		0.3	1.3	
Input Offset Current			1.2	5.6	nA
Average Input Offset Current Drift[1]			8.0	50	pA/°C
Input Bias Current			±2.0	±6.0	nA
Average Input Bias Current Drift[1]			13	50	pA/°C
Input Voltage Range		±13	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ±13V	106	123		dB
Power Supply Rejection Ratio	V_S = ±3V to ±18V	94	106		dB
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_O = ±10V	150	400		V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	±12	±12.6		V

Notes: 1. This parameter is tested on a sample basis only, and guaranteed to an LPTD of 10.
2. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	RC714E			RC714C			RC714L			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[4]			30	75		60	150		100	250	μV
Long Term Input Offset Voltage Stability[1,2]			0.3	1.5		0.4	2.0		0.5	3.0	μV/Mo
Input Offset Current			0.5	3.8		0.8	6.0		0.8	20	nA
Input Bias Current			±1.2	±4.0		±1.8	±7.0		±2.0	±30	nA
Input Noise Voltage[2]	0.1Hz to 10Hz		0.35	0.6		0.38	0.65		0.38		μV_{p-p}
Input Noise Voltage Density[2]	f_0 = 10Hz f_0 = 100Hz f_0 = 1000Hz		10.3 10 9.6	18 13 11		10.5 10.2 9.8	20 13.5 11.5		10.5 10.2 9.8		$\frac{nV}{\sqrt{Hz}}$
Input Noise Current[2]	0.1Hz to 10Hz		14	30		15	35		15		pA_{p-p}
Input Noise Current Density[2]	f_0 = 10Hz f_0 = 100Hz f_0 = 1000Hz		0.32 0.14 0.12	0.8 0.23 0.17		0.35 0.15 0.13	0.9 0.27 0.18		0.35 0.15 0.13		$\frac{pA}{\sqrt{Hz}}$
Input Resistance (Differential Mode)[3]		15	50		8.0	33		7.0	31		MΩ
Input Resistance (Common Mode)			160			120			120		GΩ
Input Voltage Range		±13	±14		±13	±14		±13	±14		V
Common Mode Rejection Ratio	V_{CM} = ±13V	106	123		100	120		90	110		dB
Power Supply Rejection Ratio	V_S = ±3V to ±18V	94	107		90	104		90	104		dB
Large Signal Voltage Gain[3]	$R_L \geq 2k\Omega$, V_O = ±10V	200	500		100	400		100	400		V/mV
	$R_L \geq 500\Omega$, V_O = ±0.5V, V_S = ±3V	150	500		100	400					
Output Voltage Swing	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12 ±10.5	±13 ±12.8 ±12		±12 ±11.5	±13 ±12.8 ±12		±12 ±11	±13 ±12.8		V
Slew Rate	$R_L \geq 2k\Omega$	0.1	0.17		0.1	0.17			0.17		V/μS
Unity Gain Bandwidth			0.5			0.5			0.5		MHz
Open Loop Output Resistance	V_O = 0, I_O = 0		60			60			60		Ω
Power Consumption	V_S = ±15V V_S = ±3V		75 4.0	120 6.0		80 4.0	150 8.0		80 5.0	180 12	mW
Offset Adjustment Range	R_P = 20kΩ		±4.0			±4.0			±4.0		mV

Notes:
1. Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV.
2. This parameter is tested on a sample basis only, and guaranteed to an LTPD of 10.
3. Guaranteed by design.
4. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

Electrical Characteristics (Continued)

(V_S = ±15V and 0°C ≤ T_A ≤ +70°C unless otherwise noted)

Parameters	Test Conditions	RC714E			RC714C			RC714L			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[2]			45	130		85	250		85	400	µV
Average Input Offset[1] Voltage Drift Without External Trim			0.3	1.3		0.5	1.8		0.7	3.0	µV/°C
With External Trim	R_P = 20kΩ		0.3	1.3		0.4	1.6		0.7		
Input Offset Current			0.9	5.3		1.6	8.0		1.6	40	nA
Average Input Offset Current Drift[1]			8.0	35		12	50		12	100	pA/°C
Input Bias Current			±1.5	±5.5		±2.2	±9.0		±3.0	±60	nA
Average Input Bias Current Drift[1]			13	35		18	50		18	150	pA/°C
Input Voltage Range		±13	±13.5		±13	±13.5		±13	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ±13V	103	123		97	120		94	106		dB
Power Supply Rejection Ratio	V_S = ±3V to ±18V	90	104		86	100		83	100		dB
Large Signal Voltage Gain	R_L ≥ 2kΩ, V_O = ±10V	180	450		100	400		80	400		V/mV
Output Voltage Swing	R_L = 2kΩ	±12	±12.6		±11	±12.6		±10	±12.6		V

Notes: 1. This parameter is tested on a sample basis only, and guaranteed to an LTPD of 10.

2. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

Digital Nulling Technique

The digital nulling technique involves the zener diode nulling network of Figure 1. The zener diodes have relatively high breakdown voltages and never operate in the zener mode. The purpose of the zeners is to short out resistors R_1, $2R_1$, $4R_1$, or $8R_1$ by forcing a high reverse current through the diode to metalize the junction. The input offset voltage can be adjusted by varying the collector resistor ratio. If the difference in the two collector resistors (R_C) is a small increment ΔR_C, V_{OS} can be written as:

$$V_{OS} = V_T \ln \frac{R_C + \Delta R_C}{R_C} = V_T \ln 1 + \frac{\Delta R_C}{R_C}$$

for $\Delta R_C/R_C \ll 1.0$ $\ln (1 + \Delta R_C/R_C) \approx \Delta R_C/R_C$, thus:

$$V_{OS} \approx V_T \frac{\Delta R_C}{R_C}$$

For Figure 1 $R_2 + R_3 \gg 8R_1$, thus

$$V_{OS} \approx -V_T \frac{R_1}{8R_1 + R_2 + R_3} (7 - B_3B_2B_1) \quad (B_0 = 1)$$

or:

$$V_{OS} \approx V_T \frac{R_1}{R_2 + R_3} (1 + B_3B_2B_1) \quad (B_0 = 0)$$

where $B_3B_2B_1$ is a binary number which corresponds to the state of zener diodes Z_1, Z_2 and Z_3 as per Figure 1.

All this is accomplished during testing at the factory under computer control.

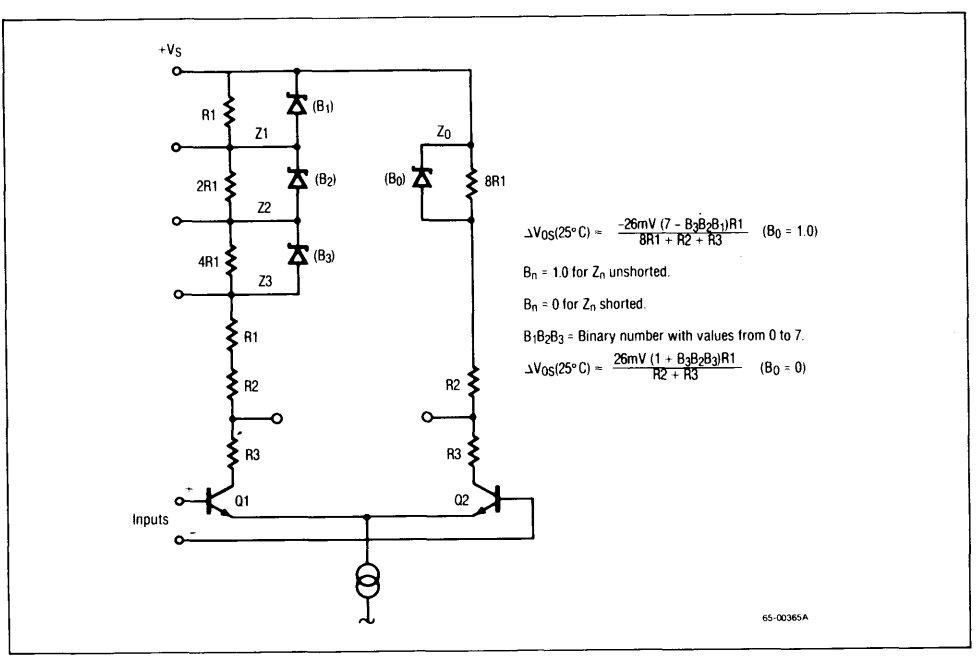
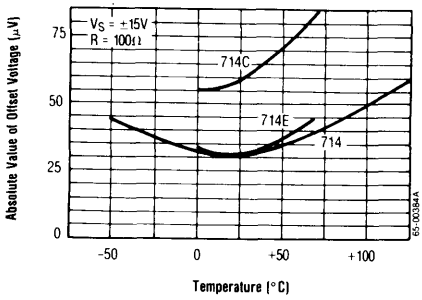


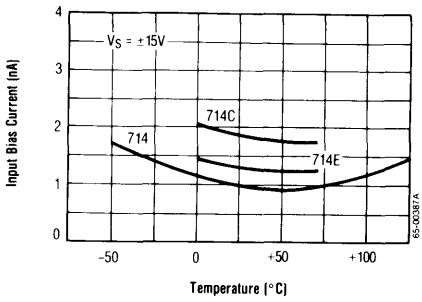
Figure 1. Digital Nulling Network

Typical Performance Characteristics

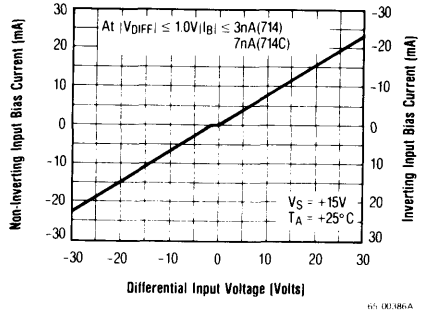
Untrimmed Offset Voltage vs. Temperature



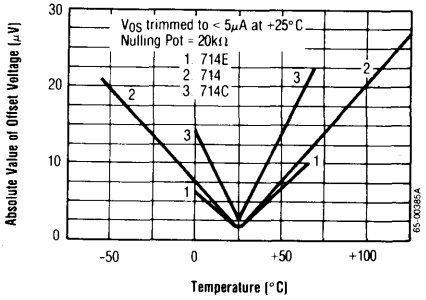
Input Bias Current vs. Temperature



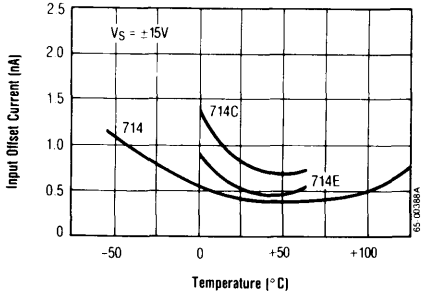
Input Bias Current vs. Differential Input Voltage



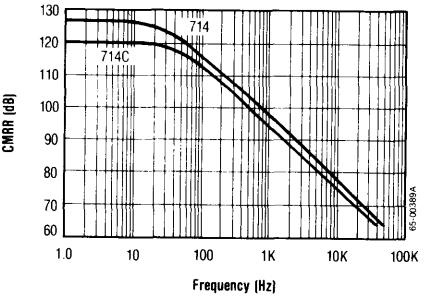
Trimmed Offset Voltage vs. Temperature



Input Offset Current vs. Temperature

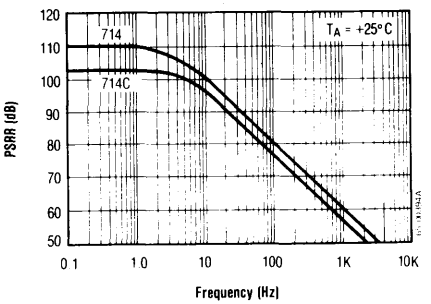


CMRR vs. Frequency

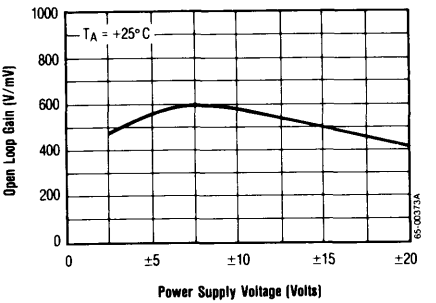


Typical Performance Characteristics (Continued)

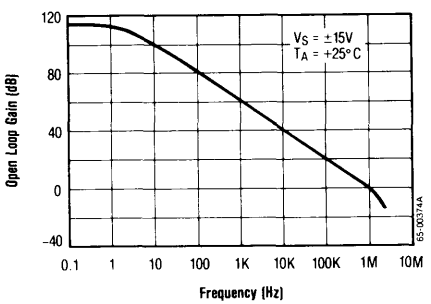
PSRR vs. Frequency



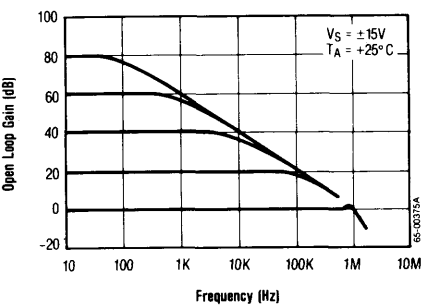
Open Loop Gain vs. Power Supply Voltage



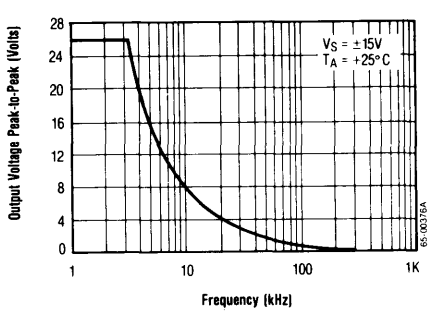
Open Loop Frequency Response



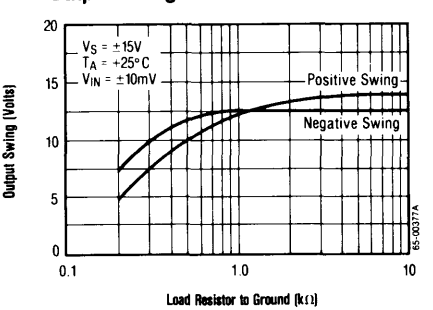
Closed Loop Response for Various Gain Configurations



Maximum Undistorted Output vs. Frequency

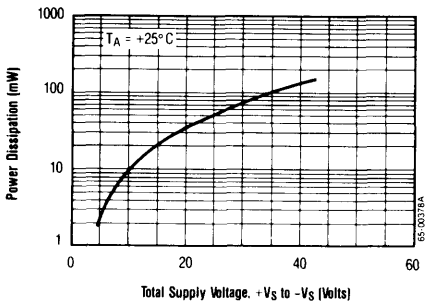


Output Voltage vs. Load Resistance

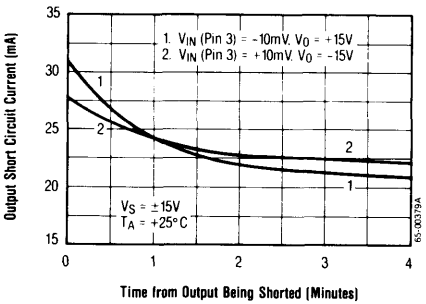


Typical Performance Characteristics (Continued)

Power Consumption vs. Power Supply

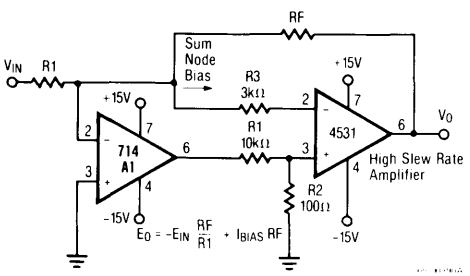


Output Short Circuit Current vs. Time

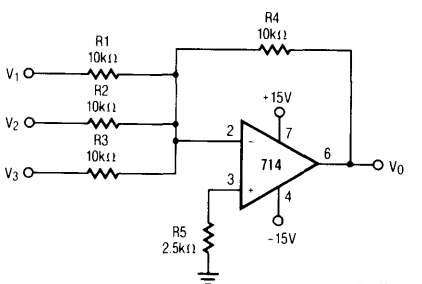


Typical Applications

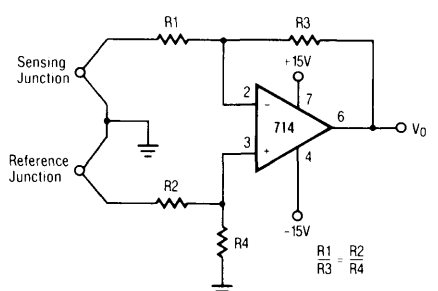
High Speed, Low V_{OS} Composite Amplifier



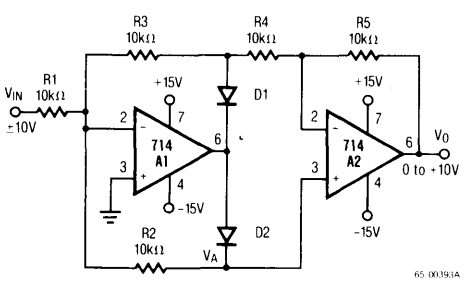
Adjustment-Free Precision Summing Amplifier



High Stability Thermocouple Amplifier



Precision Absolute Value Circuit



Raytheon

General Purpose Operational Amplifier

RC741

Features

- Supply voltages
  RC/RV741 — ±18V
  RM741 — ±22V
- Offset voltage null capability
- Short-circuit protection
- No frequency compensation required
- No latch-up
- Large common-mode and differential voltage ranges
- Low power consumption

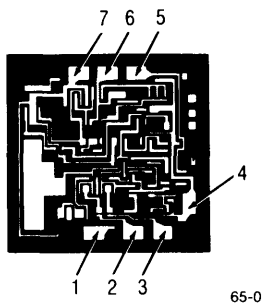
Description

The RC741 integrated circuit is a high-performance, high-gain, internally compensated monolithic operational amplifier fabricated on a single silicon chip using an advanced epitaxial process.

High common-mode voltage range and absence of latch-up tendencies make the RC741 ideal for use as a voltage follower. High gain and wide ranges of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications.

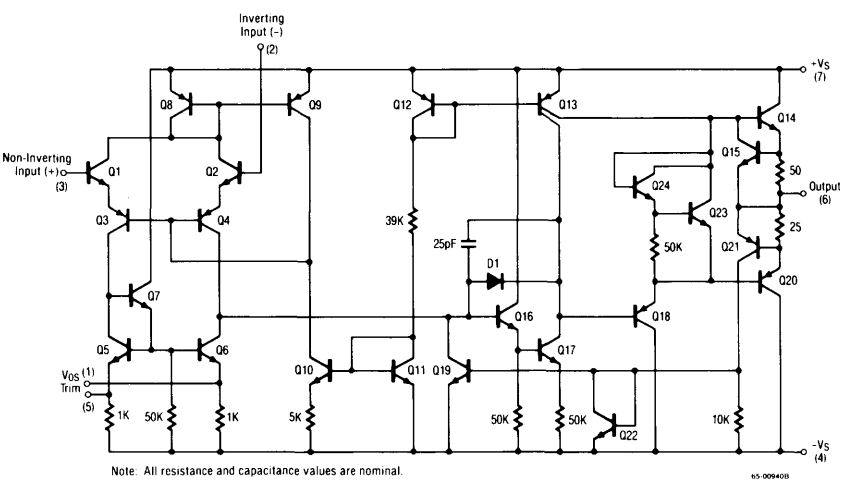
The RC741 is pin compatible with the RM709, LM101A and the LM107. The military version, RM741 operates over a temperature range from -55°C to +125°C. The commercial version, RC741, operates from 0°C to +70°C.

Mask Pattern



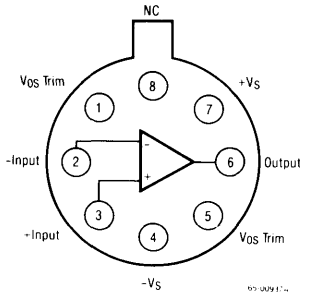
Die Size: 55 x 55 mils
Min. Pad Dimension: 4 x 4 mils

Schematic Diagram

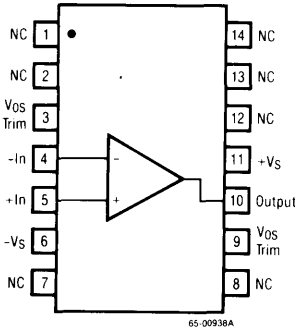


Connection Information

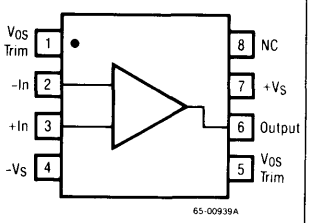
8-Lead
Metal Can TO-99
(Top View)



14-Lead
Dual In-Line Package
(Top View)



8-Lead
Dual In-Line Package
(Top View)



Absolute Maximum Ratings

Supply Voltage
- RC/RV741 ..... ±18V
- RM741 ..... ±22V

Differential Input Voltage 30V

Input Voltage[1] ..... ±15V

Output Short Circuit Duration[2] ..... Indefinite

Storage Temperature
- Range ..... -65°C to +150°C

Operating Temperature Range
- RC741 ..... 0°C to +70°C
- RM741 ..... -55°C to +125°C
- RV741 ..... -40°C to +85°C

Lead Soldering Temperature
- (60 Sec) ..... +300°C

Notes:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature for RM741.

Ordering Information

Part Number	Package	Operating Temperature Range
RC741DC	Ceramic	0°C to +70°C
RC741DE	Ceramic	0°C to +70°C
RC741H	TO-99	0°C to +70°C
RC741NB	Plastic	0°C to +70°C
RC741T	TO-99	0°C to +70°C
RV741NB	Plastic	-40°C to +85°C
RM741DC	Ceramic	-55°C to +125°C
RM741DC/883B*	Ceramic	-55°C to +125°C
RM741DE	Ceramic	-55°C to +125°C
RM741DE/883B*	Ceramic	-55°C to +125°C
RM741T	TO-99	-55°C to +125°C
RM741T/883B*	TO-99	-55°C to +125°C

*MIL-STD-883, Level B Processing

Thermal Characteristics

	8-Lead Plastic DIP	8-Lead Ceramic DIP	14-Lead Ceramic DIP	8-Lead TO-99 Metal Can
Max. Junction Temp.	125°C	175°C	175°C	175°C
Max. P_D T_A < 50°C	468mW	833mW	1042mW	658mW
Therm. Res. θ_{JC}	—	45°C/W	60°C/W	50°C/W
Therm. Res. θ_{JA}	160°C/W	150°C/W	120°C/W	190°C/W
For T_A > 50°C Derate at	6.25mW per °C	8.33mW per °C	8.33mW per °C	5.26mW per °C

Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	RM741			RC/RV741			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[1]	$R_S \leq 10k\Omega$		1.0	5.0		2.0	6.0	mV
Input Offset Current			20	200		20	200	nA
Input Bias Current			80	500		80	500	nA
Input Resistance (Differential Mode)		0.3	2.0		0.3	2.0		MΩ
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	50	200		20	200		V/mV
Output Voltage Swing	$R_L \geq 10k\Omega$	±12	±14		±12	±14		V
	$R_L \geq 2k\Omega$	±10	±13		±10	±13		V
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	90		70	90		dB
Power Supply Rejection Ratio	$R_S \leq 10k\Omega$	76	90		76	30		dB
Power Consumption			50	85		50	85	mW
Transient Response Rise Time	V_{IN} = 20mV, R_L = 2kΩ		0.3			0.3		μS
Overshoot	$C_L \leq 100pF$		5.0			5.0		%
Slew Rate	$R_L \geq 2k\Omega$		0.5			0.5		V/μS

Note: 1. Offset voltage is nulled by connecting a 10kΩ potentiometer across the balance pins and connecting the wiper pin to $-V_S$.

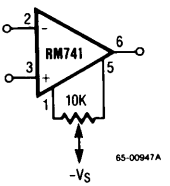
Electrical Characteristics (Continued)

($-55°C \leq T_A \leq +125°C$ for RM741; $0°C \leq T_A + 70°C$ for RC/RV741)

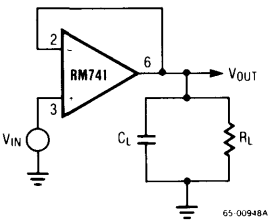
Parameters	Test Conditions	RM741			RC/RV741			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_L \geq 10k\Omega$			6.0			7.5	mV
Input Offset Current				200			300	nA
Input Bias Current				1500			800	nA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$	25			15			V/mV
Output Voltage Swing	$R_L \geq 10k\Omega$	±12			±12			V
	$R_L \geq 2k\Omega$	±10			±10			V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70			70			dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$	76				94		dB
Supply Current	+125°C			2.5				mA
	-55°C			3.3				
Power Consumption	+125°C			75				mW
	-55°C			100				

Typical Performance Characteristics

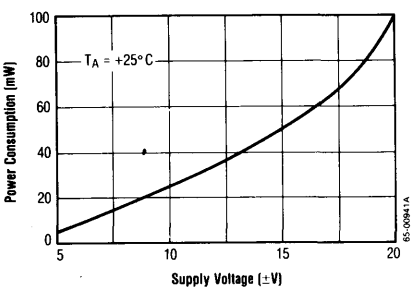
Voltage Offset Null Circuit



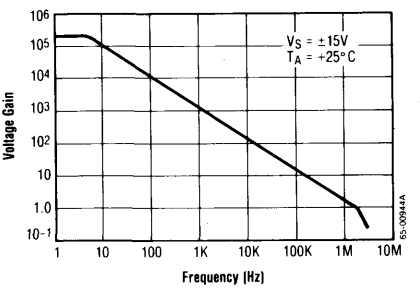
Transient Response Test Circuit



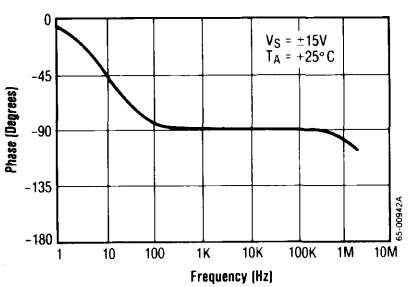
Power Consumption as a Function of Supply Voltage



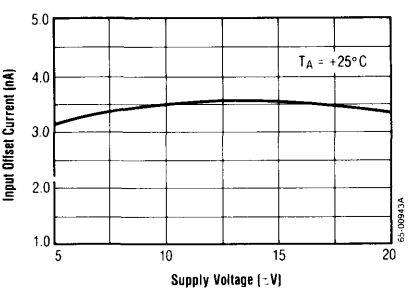
Open Loop Voltage Gain as a Function of Frequency



Open Loop Phase Response as a Function of Frequency

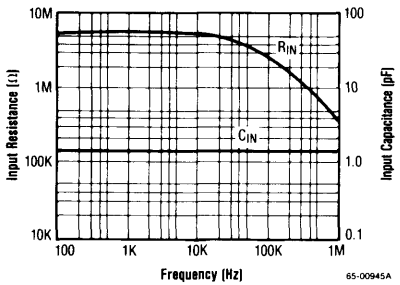


Input Offset Current as a Function of Supply Voltage

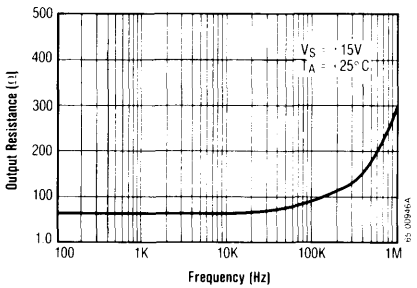


Typical Performance Characteristics (Continued)

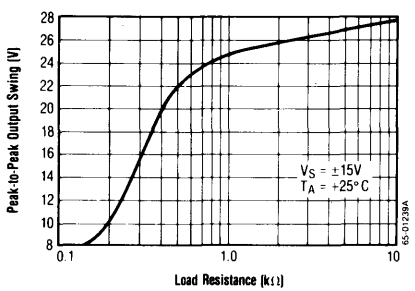
Input Resistance and Input Capacitance as a Function of Frequency



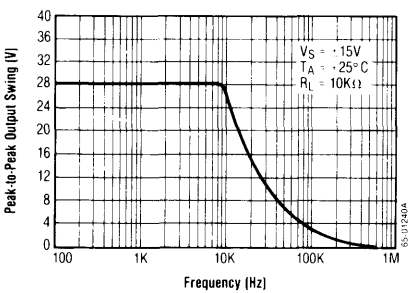
Output Resistance as a Function of Frequency



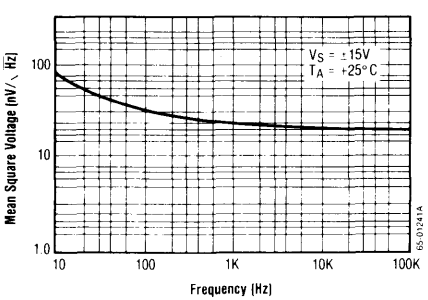
Output Voltage Swing as a Function of Load Resistance



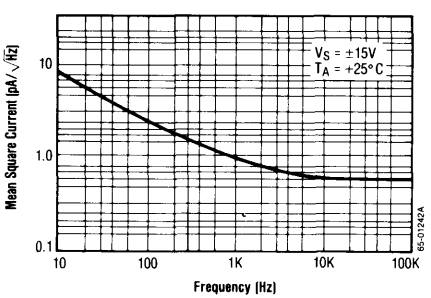
Output Voltage Swing as a Function of Frequency



Input Noise Voltage as a Function of Frequency

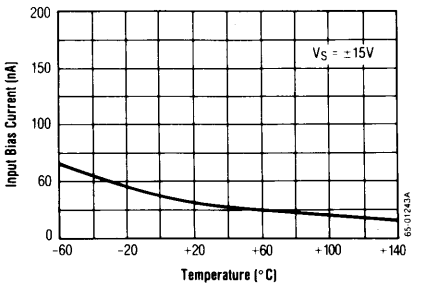


Input Noise Current as a Function of Frequency

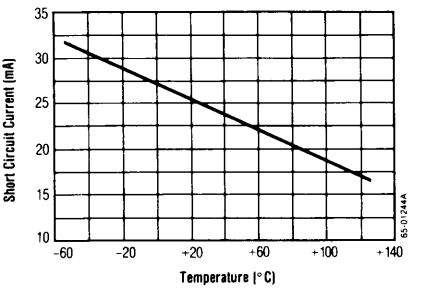


Typical Performance Characteristics (Continued)

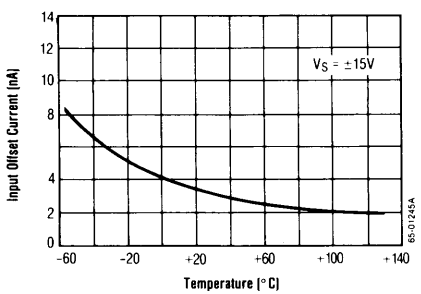
Input Bias Current as a Function of Ambient Temperature



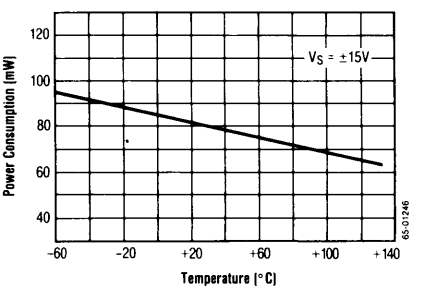
Output Short Circuit Current as a Function of Ambient Temperature



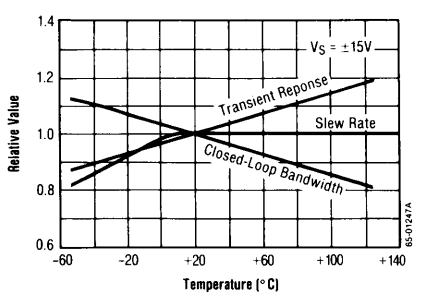
Input Offset Current as a Function of Ambient Temperature



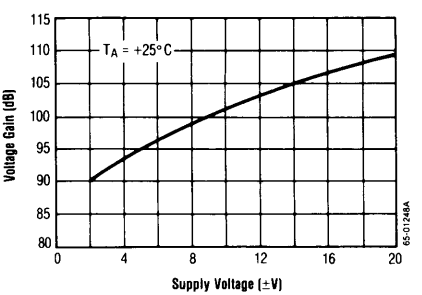
Power Consumption as a Function of Ambient Temperature



Frequency Characteristics as a Function of Ambient Temperature

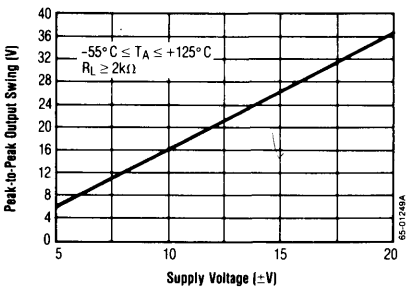


Open Loop Voltage Gain as a Function of Supply Voltage

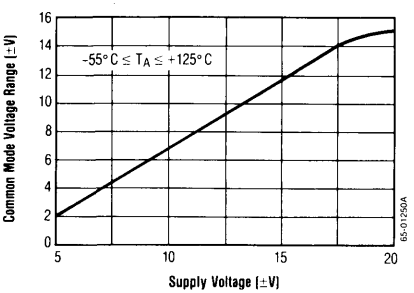


Typical Performance Characteristics (Continued)

Output Voltage Swing as a Function of Supply Voltage



Input Common Mode Voltage Range as a Function of Supply Voltage



Raytheon

General Purpose Dual Operational Amplifier

RC747/747S

Features

- Short circuit protection
- No frequency compensation required
- No latch-up
- Large common mode and differential voltage ranges
- Low power consumption
- Parameter tracking over temperature range
- Gain and phase match between amplifiers

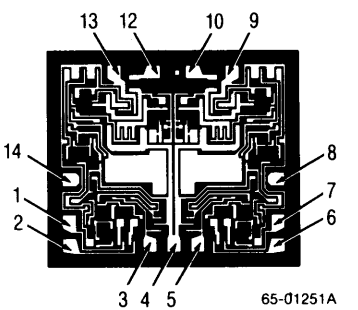
Description

The RC/RM747 integrated circuits are high gain, operational amplifiers internally compensated and constructed on a single silicon chip using an advanced epitaxial process.

The military version, RM747, operates over a temperature range from -55°C to +125°C. The commercial version, RC747, operates from 0°C to +70°C.

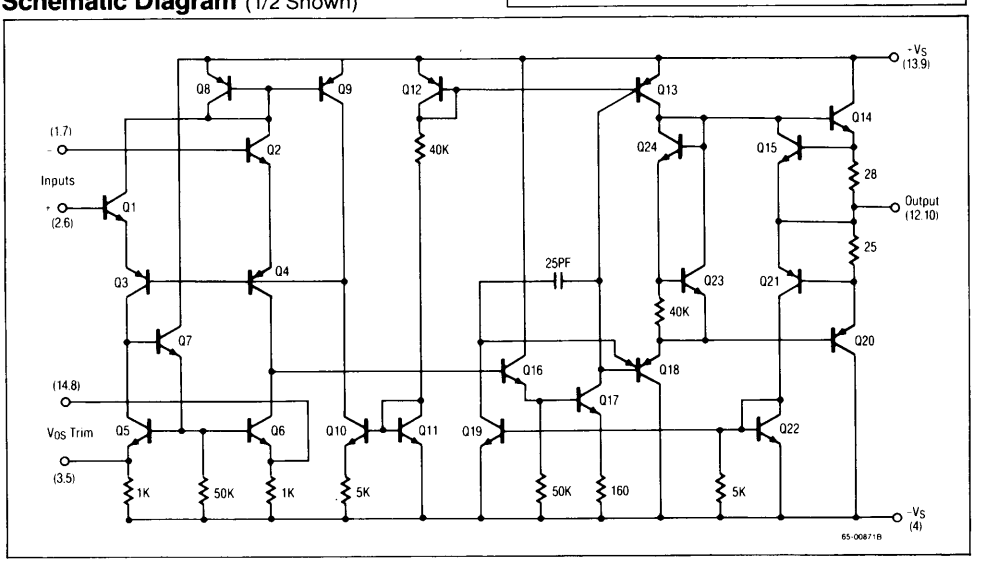
Combining the features of the 741 with the close parameter matching and tracking of a dual device on a monolithic chip results in unique performance characteristics. Excellent channel separation allows the use of the dual device in all single 741 operational amplifier applications providing high packaging density. It is especially well suited for applications in differential-in, differential-out as well as in potentiometric amplifiers and where gain and phase matched channels are mandatory.

Mask Pattern



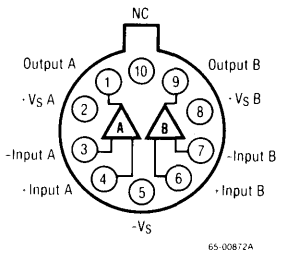
Die Size: 62 x 72 mils
Min. Pad Dimension: 4 x 4 mils

Schematic Diagram (1/2 Shown)

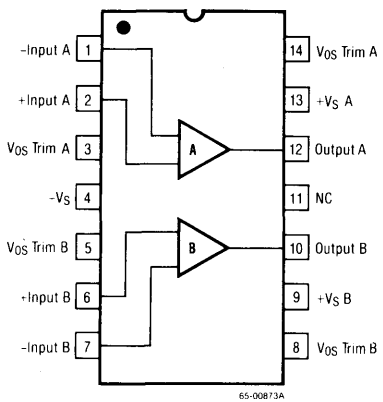


Connection Information

10-Lead
Metal Can TO-100
(Top View)



14-Lead
Dual In-Line Package
(Top View)



+VS A is internally connected to +VS B for the 747S

Absolute Maximum Ratings

Supply Voltage
- RM747 ..... ±22V
- RC747 ..... ±18V

Differential Input Voltage 30V
Input Voltage[1] ..... ±15V
Output Short-Circuit Duration[2] ..... Indefinite
Storage Temperature
- Range ..... -65°C to +150°C

Operating Temperature Range
- RM747 ..... -55°C to +125°C
- RC747 ..... 0°C to +70°C

Lead Soldering Temperature
- (60 Sec) ..... +300°C

Notes: 1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Short-circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature for RC747.

Thermal Characteristics

	14-Lead Plastic DIP	14-Lead Ceramic DIP	10-Lead TO-100 Metal Can
Max. Junc. Temp.	125°C	175°C	175°C
Max. P_D T_A < 50°C	468mW	1042mW	658mW
Therm. Res. θ_{JC}	—	60°C/W	50°C/W
Therm. Res. θ_{JA}	160°C/W	120°C/W	190°C/W
For T_A > 50°C Derate at	6.25mW per °C	8.33mW per °C	5.26mW per °C

Ordering Information

Part Number	Package	Operating Temperature Range
RC747DC	Ceramic	0°C to +70°C
RC747DB	Ceramic	0°C to +70°C
RC747T	TO-100	0°C to +70°C
RM747DC	Ceramic	-55°C to +125°C
RM747DC/883B*	Ceramic	-55°C to +125°C
RM747T	TO-100	-55°C to +125°C
RM747T/883B*	TO-100	-55°C to +125°C

*MIL-STD-883, Level B Processing

Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise specified)

Parameters	Test Conditions	RM747			RC747			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 10k\Omega$		1.0	5.0		2.0	6.0	mV
Input Offset Current			20	200		20	200	nA
Input Bias Current			80	500		80	500	nA
Input Resistance (Differential Mode)		0.3	2.0		0.3	2.0		MΩ
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	50	200		50	200		V/mV
Output Voltage Swing	$R_L \geq 10k\Omega$	±12	±14		±12	±14		V
	$R_L \geq 2k\Omega$	±10	±13		±10	±13		V
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	80	90		70	90		dB
Power Supply Rejection Ratio	$R_S \leq 10k\Omega$	76	90		76	90		dB
Power Consumption			100	170		100	170	mW
Transient Response Risetime	V_{IN} = 20mV, R_L = 2kΩ, $C_L \leq$ 100pF		0.3			0.3		μS
Overshoot			5.0			5.0		%
Slew Rate	$R_L \geq 2k\Omega$		0.5			0.5		V/μS
Channel Separation	f = 1kHz		98			98		dB

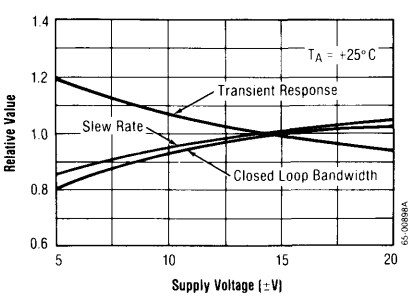
Electrical Characteristics

($-55°C \leq T_A \leq +125°C$ for RM747; $0°C \leq T_A \leq +70°C$ for RC747 unless otherwise specified)

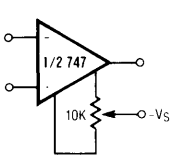
Parameters	Test Conditions	RM747			RC747			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 10k\Omega$			6.0			7.5	mV
Input Offset Current	$T_A = +125°C$, $T_A = +70°C$			200			300	nA
	$T_A = -55°C$, $T_A = 0°C$			500			300	
Input Bias Current	$T_A = +125°C$, $T_A = +70°C$			500			800	nA
	$T_A = -55°C$, $T_A = 0°C$			1500			800	
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$	25			25			V/mV
Output Voltage Swing	$R_L \geq 10K$	±12			±10			V
	$R_L \geq 2k\Omega$	±10						
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70			70			dB
Power Supply Rejection Ratio	$R_S \leq 10k\Omega$	76			76			dB
Power Consumption	$T_A = +125°C$			150			150	mW
	$T_A = -55°C$			200			200	
Input Voltage Range		±12			±12			V

Typical Performance Characteristics

Frequency Characteristics as a Function of Ambient Temperature

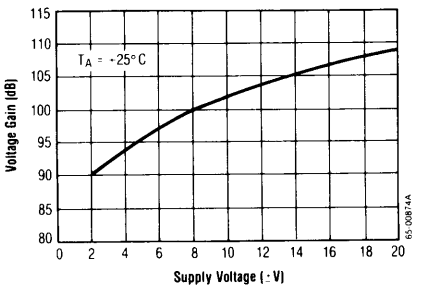


Voltage Offset Null Circuit

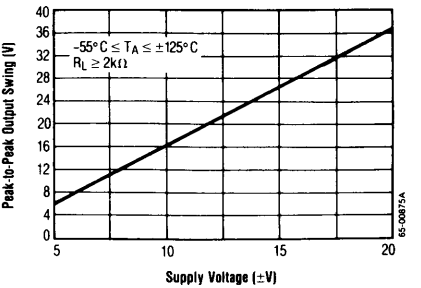


Typical Performance Characteristics (Continued)

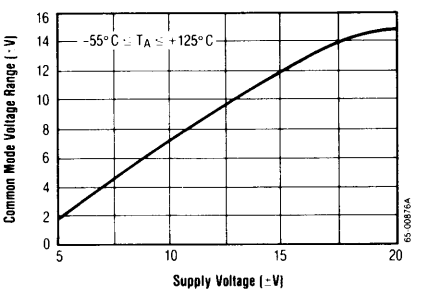
Open Loop Voltage Gain as a Function of Supply Voltage



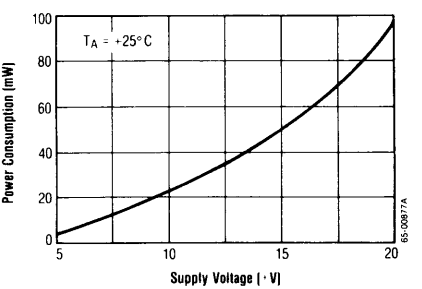
Output Voltage Swing as a Function of Supply Voltage



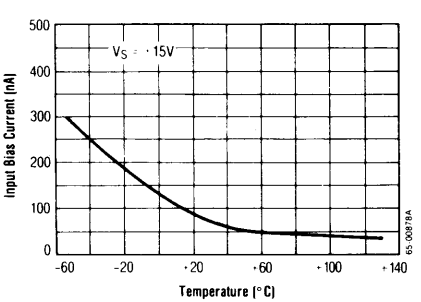
Input Common Mode Voltage Range as a Function of Supply Voltage



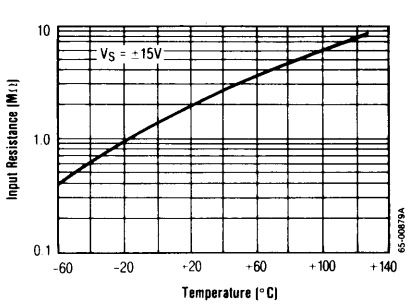
Power Consumption as a Function of Supply Voltage



Input Bias Current as a Function of Ambient Temperature

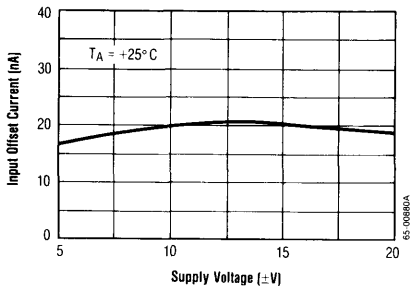


Input Resistance as a Function of Ambient Temperature

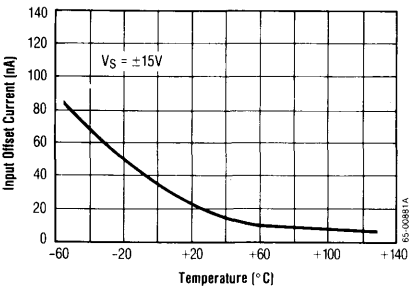


Typical Performance Characteristics (Continued)

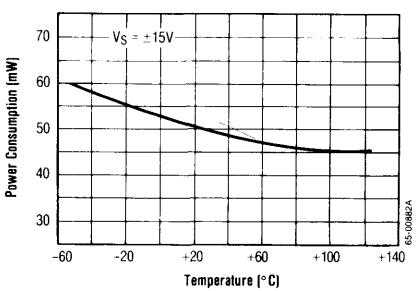
Input Offset Current as a Function of Supply Voltage



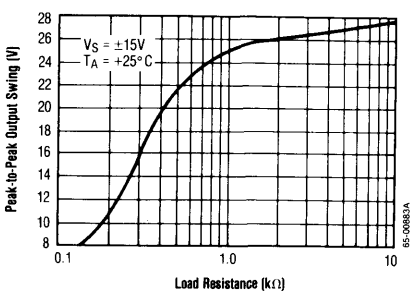
Input Offset Current as a Function of Ambient Temperature



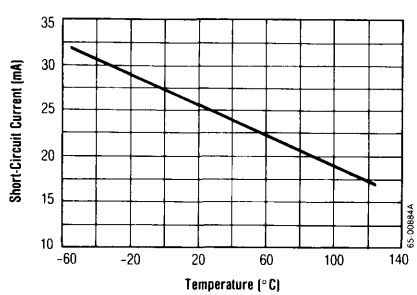
Power Consumption as a Function of Ambient Temperature



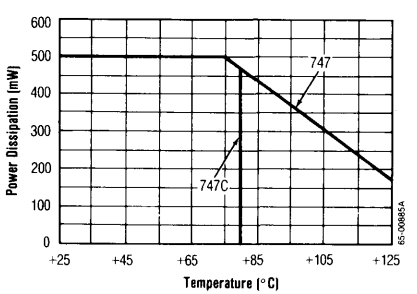
Output Voltage Swing as a Function of Load Resistance



Output Short Circuit Current as a Function of Ambient Temperature

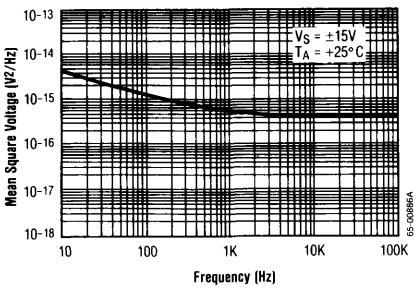


Absolute Maximum Power Dissipation as a Function of Ambient Temperature

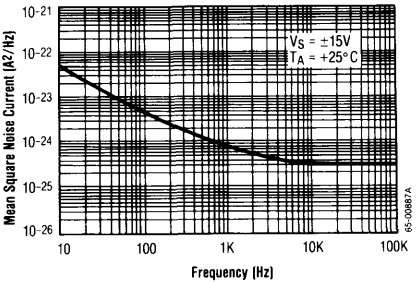


Typical Performance Characteristics (Continued)

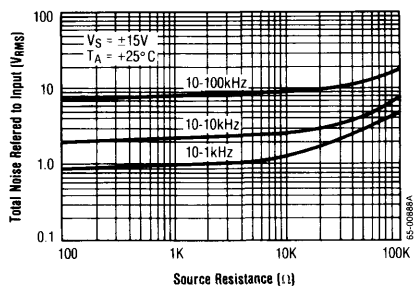
Input Noise Voltage as a Function of Frequency



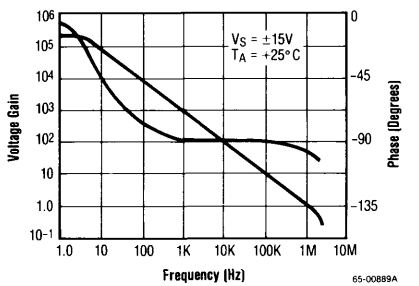
Input Noise Current as a Function of Frequency



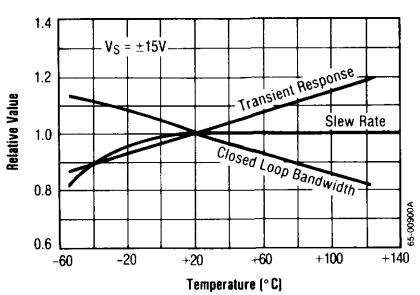
Broadband Noise for Various Bandwidths



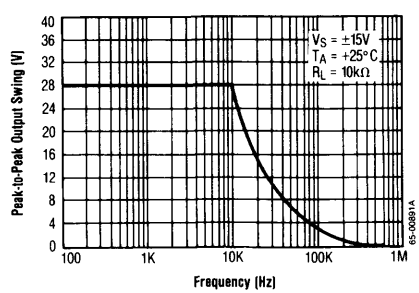
Open Loop Voltage Gain as a Function of Frequency



Frequency Characteristics as a Function of Ambient Temperature

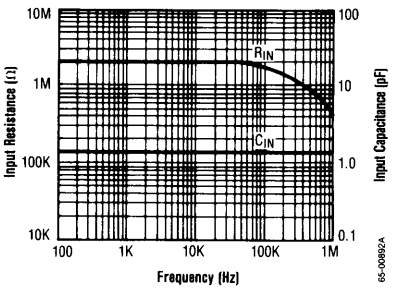


Output Voltage Swing as a Function of Frequency

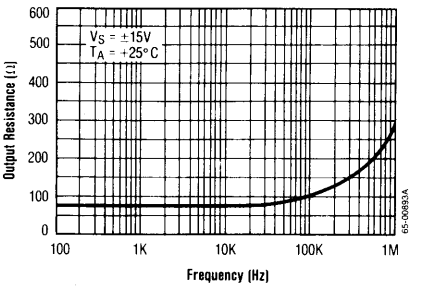


Typical Performance Characteristics (Continued)

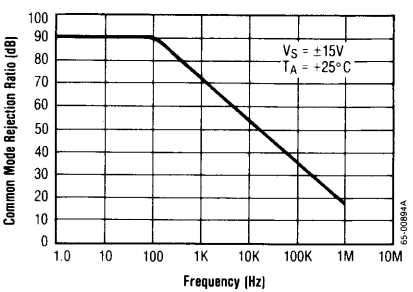
Input Resistance and Input Capacitance as a Function of Frequency



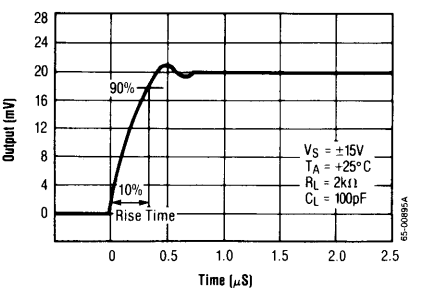
Output Resistance as a Function of Frequency



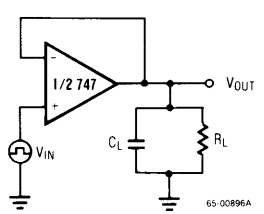
Common Mode Rejection Ratio as a Function of Frequency



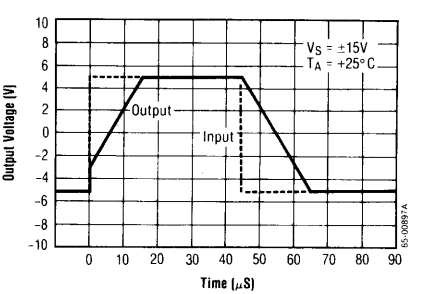
Transient Response



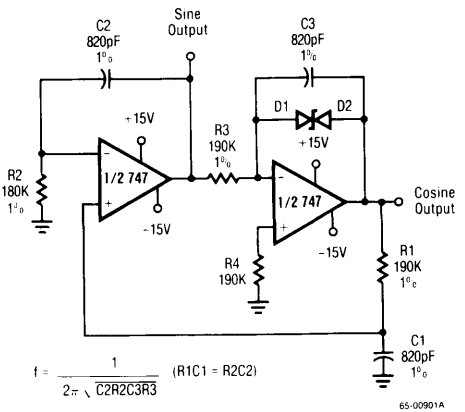
Transient Response Test Circuit



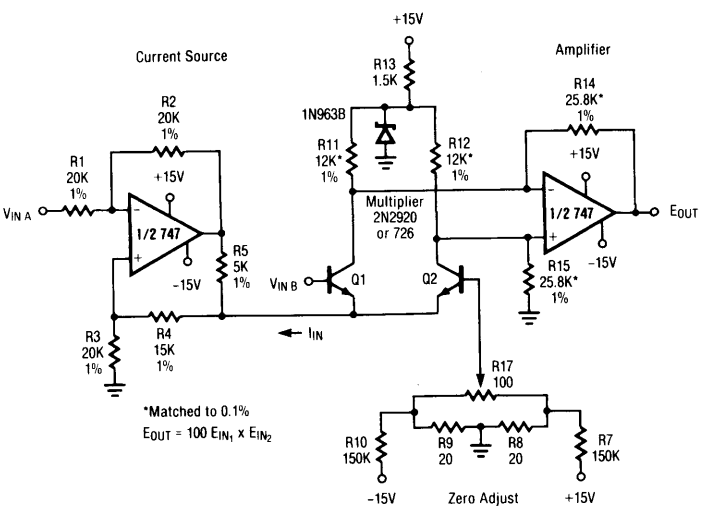
Voltage Follower Large Signal Pulse Response



Typical Applications

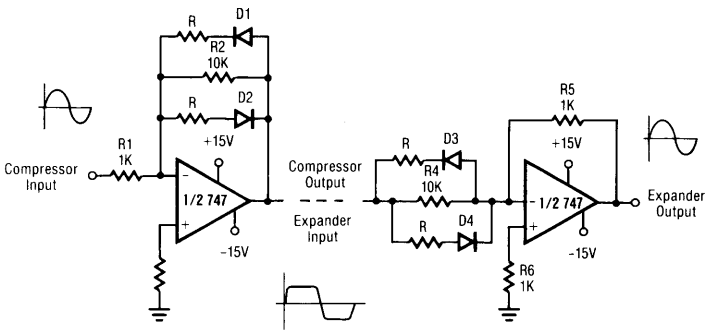


Quadrature Oscillator



Analog Multiplier

Typical Applications (Continued)

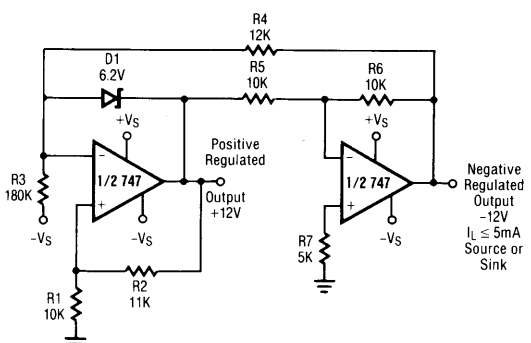


Maximum compression expansion ratio = R1/R (10KΩ > R ≥ 0)

65-00903A

Note: Diodes D1 through D4 are matched FD6666 or equivalent

Compressor/Expander Amplifiers



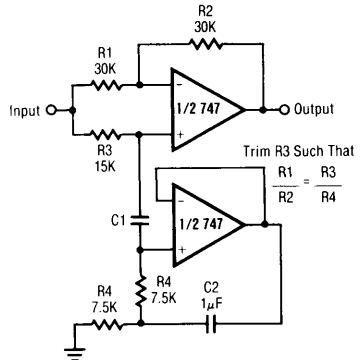
$$\text{Positive Output} = V_{D1} \times \frac{R1 + R2}{R2}$$

$$\text{Negative Output} = -\text{Positive Output} \times \frac{R6}{R5}$$

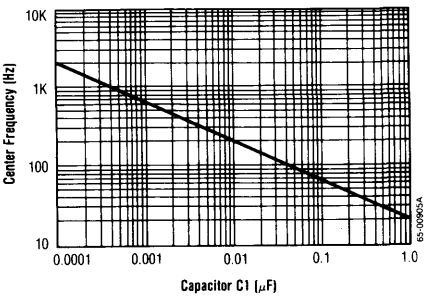
65-00904A

Tracking Positive and Negative Voltage References

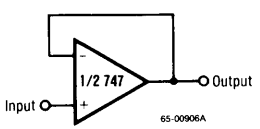
Typical Applications (Continued)



Notch Frequency as a Function of C1

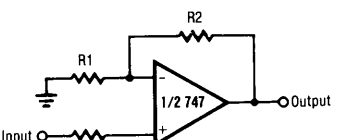


Notch Filter Using the 747 as a Gyrator



R_{IN} = 400MΩ
C_{IN} = 1pF
R_{OUT} << 1Ω
BW = 1MHz

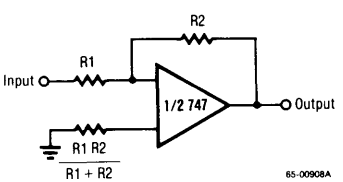
Unity Gain Voltage Follower



$$\frac{R1\ R2}{R1 + R2}$$

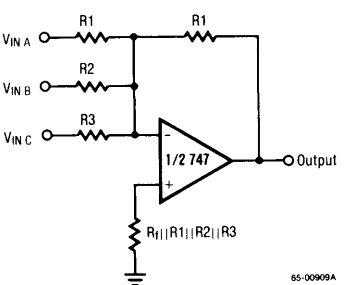
Gain	R1	R2	B.W.	R_{IN}
10	1kΩ	9kΩ	100kHz	400MΩ
100	100Ω	9.9kΩ	10kHz	280MΩ
1000	100Ω	99.9kΩ	1kHz	80MΩ

Non-Inverting Amplifier



Gain	R1	R2	B.W.	R_{IN}
1	10kΩ	10kΩ	1MHz	10kΩ
10	1kΩ	10kΩ	100kHz	1kΩ
100	1kΩ	100kΩ	10kHz	1kΩ
1000	100Ω	100kΩ	1kHz	100Ω

Inverting Amplifier



$$-V_O = V_{IN\ A}\left(\frac{R_f}{R1}\right) - V_{IN\ B}\left(\frac{R_f}{R2}\right) - V_{IN\ C}\left(\frac{R_f}{R3}\right)$$

Weighted Averaging Amplifier

Raytheon

General Purpose Dual 741 Operational Amplifier

RC1458
RM1558

Features

- Short circuit protection
- No frequency compensation required
- No latch-up
- Large common mode and differential voltage ranges
- Low power consumption
- Parameter tracking over temperature range
- Gain and phase match between amplifiers

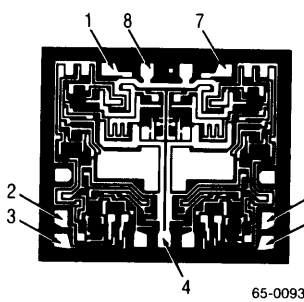
Description

The RC1458 and RM1558 integrated circuits are high gain operational amplifiers internally compensated and constructed on a single silicon chip using an advanced epitaxial process.

The military version (RM1558) operates over a temperature range from -55°C to +125°C. The commercial version (RC1458) operates from 0°C to +70°C.

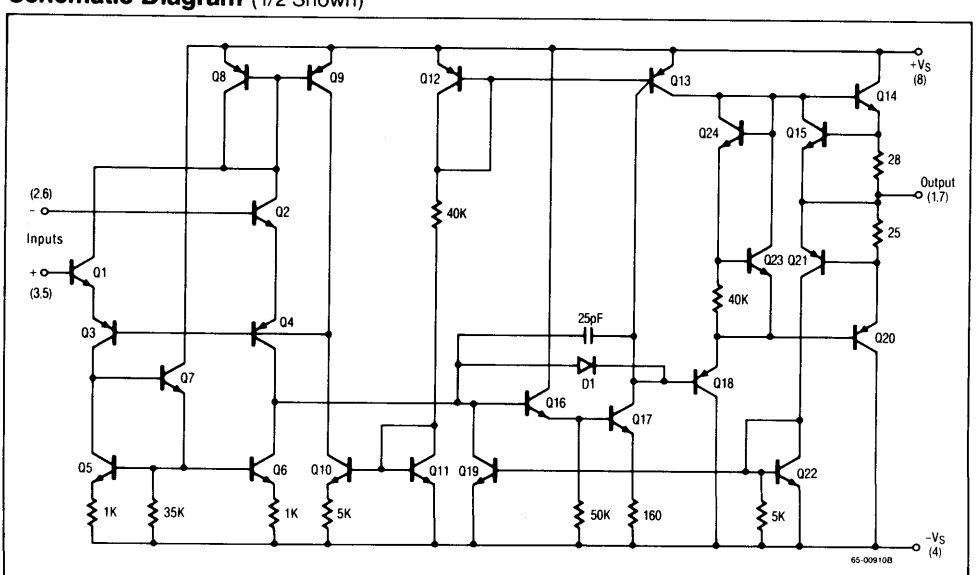
Combining all of the features of the 741 with the close parameter matching and tracking of a dual device on a monolithic chip results in unique performance characteristics. It is especially well suited for applications where gain and phase matched channels are mandatory.

Mask Pattern



Die Size: 62 x 72 mils
Min. Pad Dimension: 4 x 4 mils

Schematic Diagram (1/2 Shown)

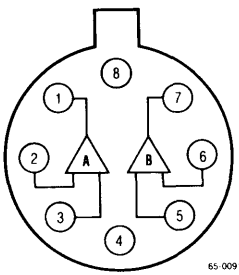


RC1458
RM1558

General Purpose
Dual 741 Operational Amplifier

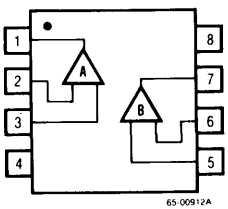
Connection Information

8-Lead
Metal Can TO-99
(Top View)



65-00911A

8-Lead
Dual In-Line Package
(Top View)



65-00912A

Pin	Function
1	Output (A)
2	-Input (A)
3	+Input (A)
4	$-V_S$
5	+Input (B)
6	-Input (B)
7	Output (B)
8	$+V_S$

Absolute Maximum Ratings

Supply Voltage
RM1558 ..... ±22V
RC1458 ..... ±18V
Differential Input Voltage 30V
Input Voltage[1] ..... ±15V
Output Short Circuit Duration[2] ..... Indefinite
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
RM1558 ..... -55°C to +125°C
RC1458 ..... 0°C to +70°C
Lead Soldering Temperature
(60 Sec) ..... +300°C

Notes: 1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Short circuit may be to ground or either supply.

Thermal Characteristics

	8-Lead Plastic DIP	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can
Max. Junc. Temp.	125°C	175°C	175°C
Max. P_D T_A < 50°C	468mW	833mW	658mW
Therm. Res. θ_{JC}	—	45°C/W	50°C/W
Therm. Res. θ_{JA}	160°C/W	150°C/W	190°C/W
For T_A > 50°C Derate at	6.25mW per °C	8.33mW per °C	5.26mW per °C

Ordering Information

Part Number	Package	Operating Temperature Range
RC1458DE	Ceramic	0°C to +70°C
RC1458H	TO-99	0°C to +70°C
RC1458T	TO-99	0°C to +70°C
RC1458NB	Plastic	0°C to +70°C
RV1458NB	Plastic	-40°C to +85°C
RM1558DE	Ceramic	-55°C to +125°C
RM1558DE/883B*	Ceramic	-55°C to +125°C
RM1558T	TO-99	-55°C to +125°C
RM1558T/883B*	TO-99	-55°C to +125°C

*MIL-STD-883, Level B Processing

Electrical Characteristics ($V_S = \pm 15V$ and $T_A = +25°C$ unless otherwise specified)

Parameters	Test Conditions	RM1558			RC1458			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 10k\Omega$		1.0	5.0		2.0	6.0	mV
Input Offset Current			30	200		30	200	nA
Input Bias Current			200	500		200	500	nA
Input Resistance (Differential Mode)		0.3	1.0		0.3	1.0		MΩ
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$	50	200		20	200		V/mV
Output Voltage Swing	$R_L \geq 10k\Omega$	±12	±14		±12	±14		V
	$R_L \geq 2k\Omega$	±10	±13		±10	±13		
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	90		70	90		dB
Power Supply Rejection Ratio	$R_S \leq 10k\Omega$	76	90		76	90		dB
Power Consumption			100	150		100	170	mW
Transient Response Rise Time	$V_{IN} = 20mV$, $R_L = 2k\Omega$		0.3			0.3		μS
Overshoot	$C_L \leq 100pF$		5.0			5.0		%
Slew Rate	$R_L \geq 2k\Omega$		0.5			0.5		V/μS
Channel Separation	f = 1kHz		98			98		dB

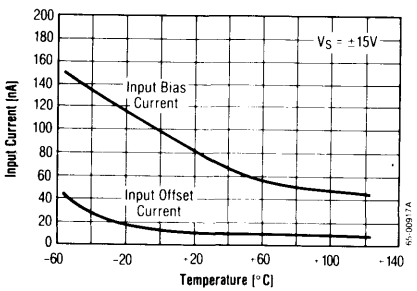
Electrical Characteristics (Continued)

(-55°C ≤ T_A ≤ +125°C for RM1558; 0°C ≤ T_A ≤ +70°C for RC1458)

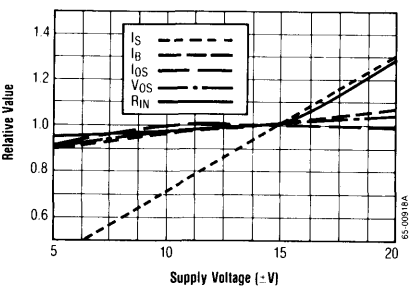
Parameters	Test Conditions	RM1558			RC1458			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_L \geq 10k\Omega$			6.0			7.5	mV
Input Offset Current	+125°C, +70°C			200			300	nA
	-55°C, 0°C			500			300	
Input Bias Current	+125°C, +70°C			500			800	nA
	-55°C, +70°C			1500			800	
Large Signal Voltage Gain	$R_L \geq 2k\Omega$ $V_{OUT} = \pm 10V$	25			15			V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	±10			±10			V
Power Consumption	$V_S = \pm 15V$ T_A = +125°C, +70°C			150			150	mW
	T_A = -55°C, 0°C			200			200	
Input Voltage Range		±12			±12			V

Typical Performance Characteristics

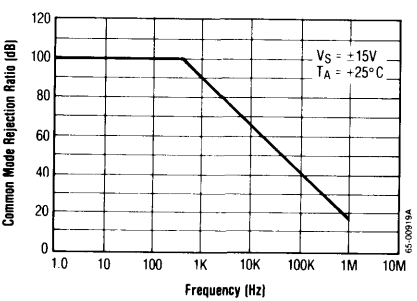
Input Bias and Offset Currents vs. Ambient Temperature



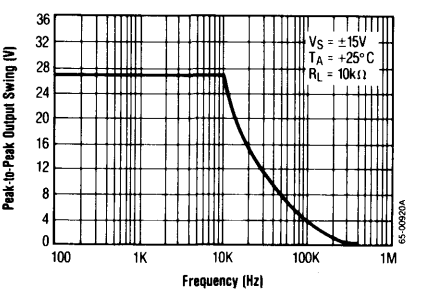
DC Parameters vs. Supply Voltage



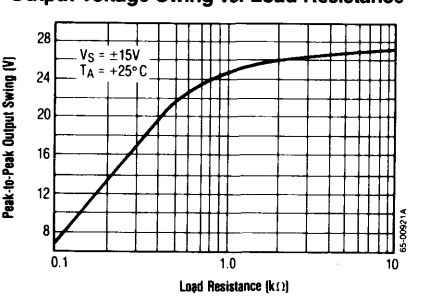
Common Mode Rejection Ratio vs. Frequency



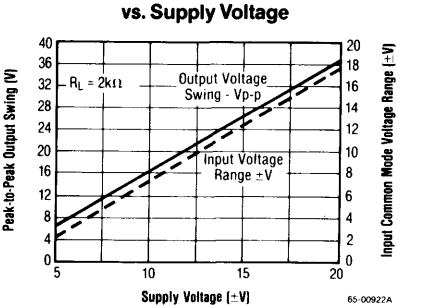
Output Voltage Swing vs. Frequency



Output Voltage Swing vs. Load Resistance

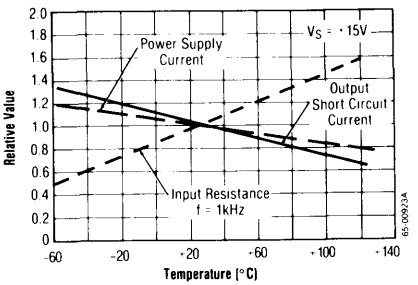


Output Swing and Input Range vs. Supply Voltage

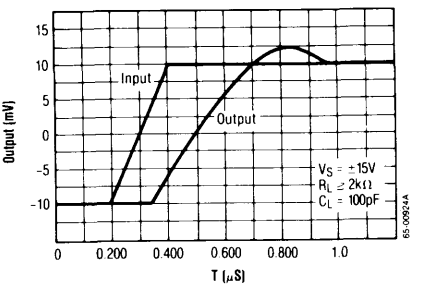


Typical Performance Characteristics (Continued)

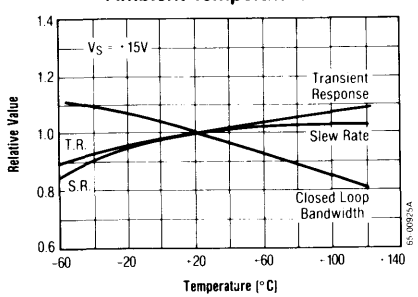
Normalized DC Parameter vs. Ambient Temperature



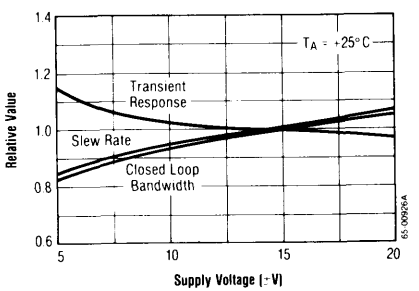
Transient Response



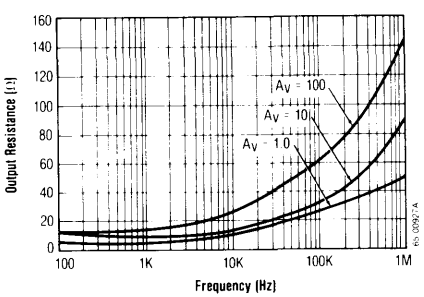
Frequency Characteristics vs. Ambient Temperature

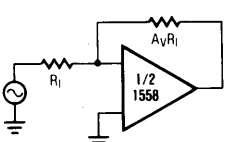


Frequency Characteristics vs. Supply Voltage



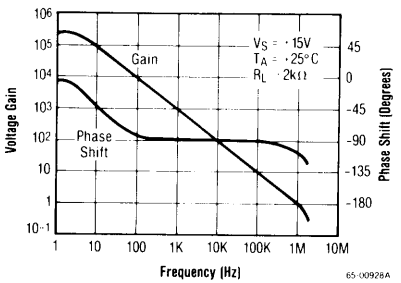
Output Resistance vs. Frequency



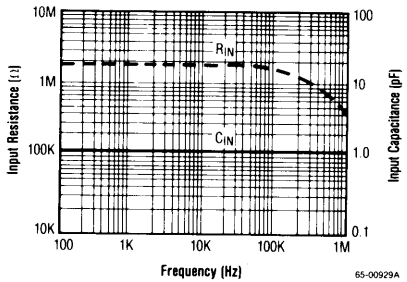


Typical Performance Characteristics (Continued)

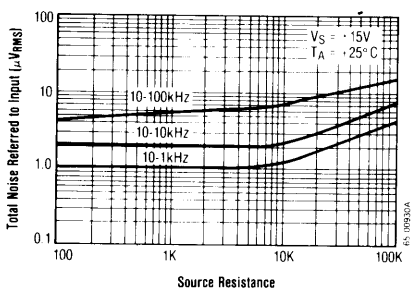
Open Loop Transfer Characteristics vs. Frequency



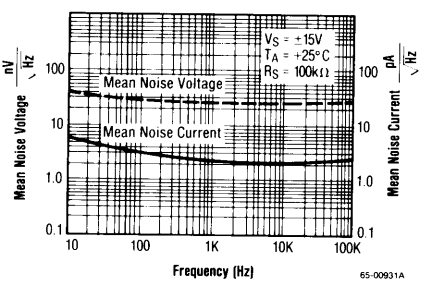
Input Resistance and Input Capacitance vs. Frequency



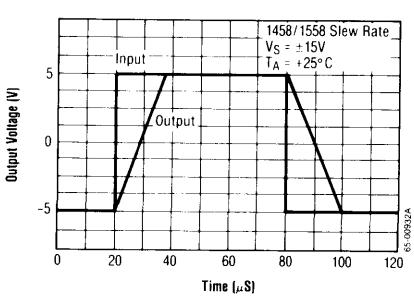
Broadband Noise for Various Bandwidths

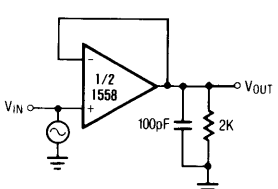


Input Noise Voltage and Current vs. Frequency



Voltage Follower Large Signal Pulse Response





Typical Applications

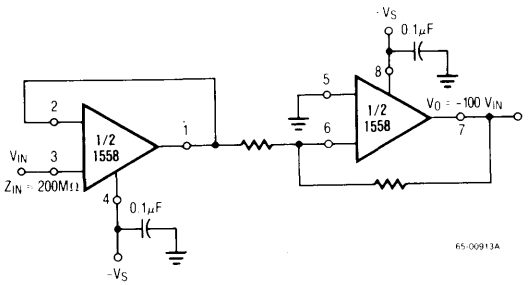


Figure 1. High-Impedance, High-Gain Inverting Amplifier

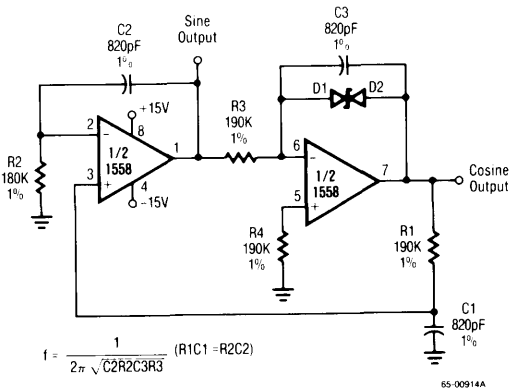


Figure 2. Quadrature Oscillator

Typical Applications (Continued)

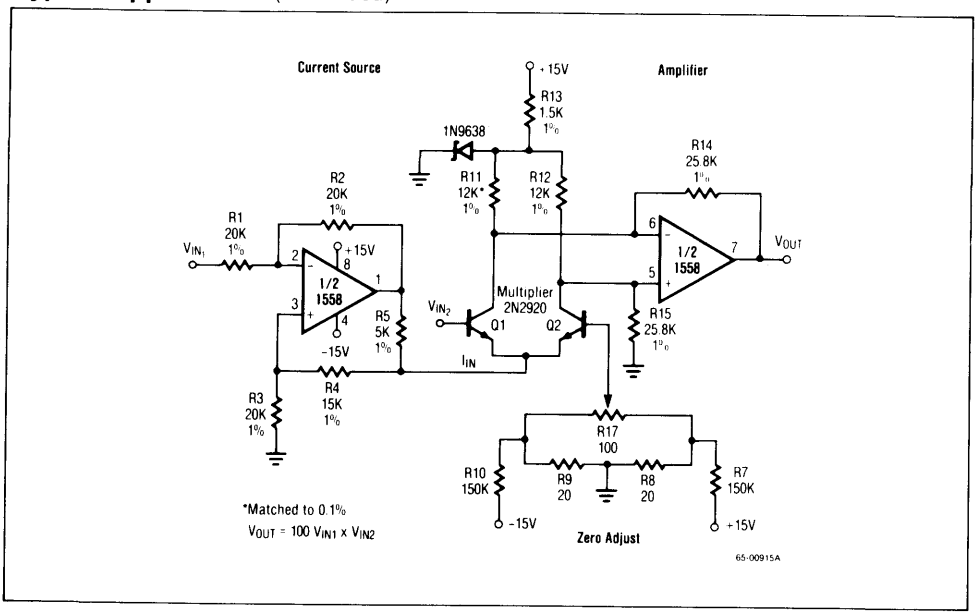


Figure 3. Analog Multiplier

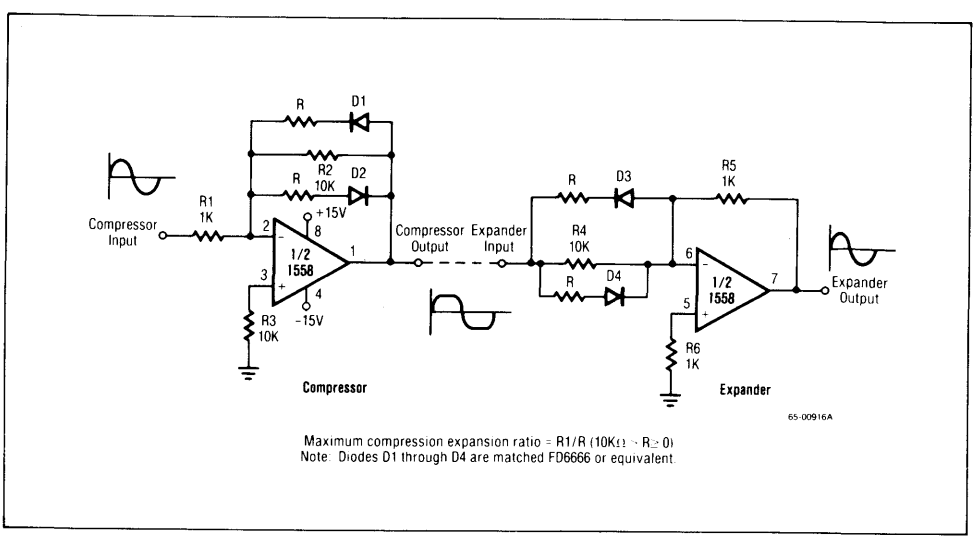


Figure 4. Compressor/Expander Amplifiers

Raytheon

High Performance, Low Noise, Dual Operational Amplifier

RC2041

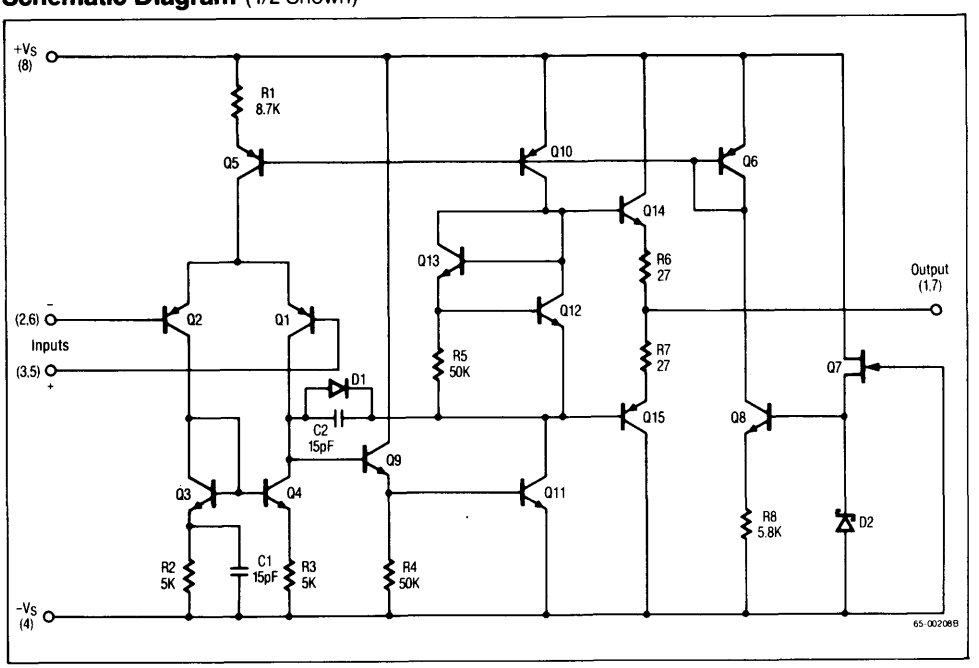
Features

- 7.0MHz unity gain bandwidth (A_V = 1)
- 3.0V/μS slew rate
- 6.0nV/√Hz noise voltage at 1kHz
- 0.3pA/√Hz noise current at 1kHz
- ±10V output into 400Ω loads (±25mA)
- 0.3mV input offset voltage
- 10nA input offset current
- 200nA input bias current
- Unity gain frequency compensated
- Output short circuit protected

Description

The 2041 integrated circuit is a high gain, wide-bandwidth, low noise dual operational amplifier capable of driving 20V peak-to-peak into 400Ω loads. The 2041 combines many of the features of the 4558 as well as providing a wider bandwidth, lower noise, higher slew rate and higher output drive. The combination of low noise and wide bandwidth make the 2041 ideal for audio preamplifiers, active filters, telecommunications, and many instrumentation applications. The availability of the 2041 in the surface mounted micro package allows very high packing densities in critical applications.

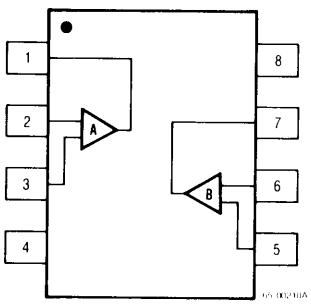
Schematic Diagram (1/2 Shown)



High Performance, Low Noise, Dual Operational Amplifier

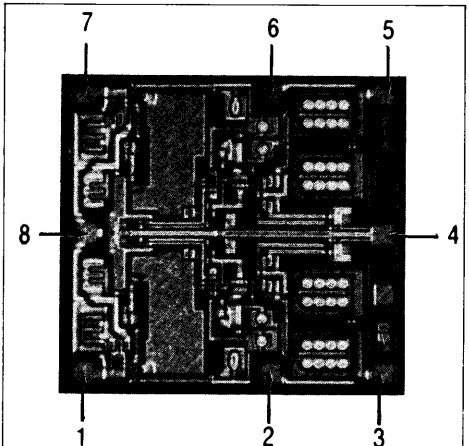
Connection Information

8-Lead
Dual In-Line Package
(Top View)



Pin	Function
1	A Output
2	A -Input
3	A +Input
4	$-V_S$
5	B +Input
6	B -Input
7	B Output
8	$+V_S$

Mask Pattern



Die Size: 52 x 61 mils
Min. Pad Dimensions: 4 x 4 mils

65-02067A

Thermal Characteristics

	8-Lead Micro-Pak Plastic DIP	8-Lead Plastic DIP
Max. Junction Temp.	125°C	125°C
Max. P_D $T_A < 50°C$	300mW	468mW
Therm. Res. θ_{JC}	—	—
Therm. Res. θ_{JA}	240°C/W	160°C/W
For $T_A > 50°C$ Derate at	4.17mW per °C	6.25mW per °C

Absolute Maximum Ratings

Supply Voltage ..... ±18V
Differential Input Voltage 30V
Input Voltage[1] ..... ±15V
Operating Temperature
Range ..... -20°C to +75°C
Lead Soldering Temperature (10 Sec)
RC2041NB ..... +300°C
RC2041M ..... +260°C
Output Short Circuit Duration[2] ..... Indefinite

Notes: 1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Short circuit may be to ground on one amp only. Rating applies to +75°C ambient temperature.

Matching Characteristics

(V_S = ±15V, T_A = +25°C)

Parameter	Conditions	Typ	Units
Voltage Gain	$R_L \geq 2k\Omega$	±1.0	dB
Input Bias Current		±15	nA
Input Offset Current		±7.5	nA
Input Offset Voltage	$R_L \geq 10k\Omega$	±0.2	mV

Ordering Information

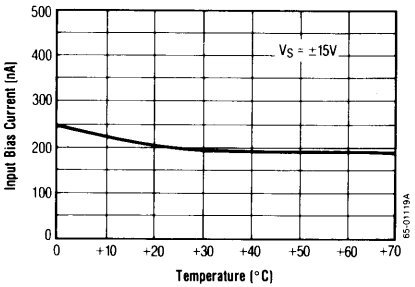
Part Number	Package	Operating Temperature Range
RC2041M	Micro-Plastic	-20°C to +75°C
RC2041NB	Plastic	-20°C to +75°C

Electrical Characteristics (V_S = ±15V, T_A = +25°C unless otherwise specified)

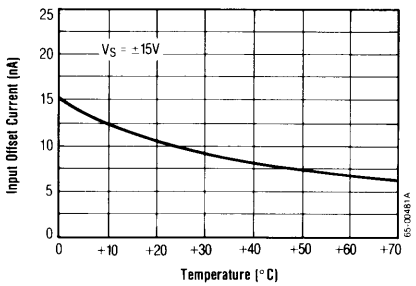
Parameters	Test Conditions	Min	Typ	Max	Units
Input Offset Voltage	$R_S \leq 10k\Omega$		0.3	3.0	mV
Input Offset Current			10	200	nA
Input Bias Current			200	500	nA
Input Resistance (Differential Mode)		0.3	1.0		MΩ
Large-Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	20	300		V/mV
Output Voltage Swing	$R_L \geq 10k\Omega$	±12	±14		V
	I_O = 25mA	±10	±11.5		
Input Voltage Range		±12	±14		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	100		dB
Power Supply Rejection Ratio	$R_S \leq 10k\Omega$	76	100		dB
Power Consumption	$R_L = \infty$		180	240	mW
Transient Response Rise Time	V_{IN} = 20mV, R_L = 2kΩ		50		nS
Overshoot	$C_L \leq 100pF$		40		%
Slew Rate	$R_L \geq 2k\Omega$		3.0		V/μS
Channel Separation	f = 10kHz, R_S = 1kΩ, Gain = 100		90		dB
Unity Gain Bandwidth	Gain = 1	4.0	7.0		MHz
The following specifications apply for $-20°C \leq T_A \leq +75°C$					
Input Offset Voltage	$R_S \leq 10k\Omega$			4.5	mV
Input Offset Current				300	nA
Input Bias Current				800	nA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	15			V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	±10			V
Power Consumption	T_A = +75°C		160	220	mW
	T_A = -20°C		210	260	

Typical Performance Characteristics

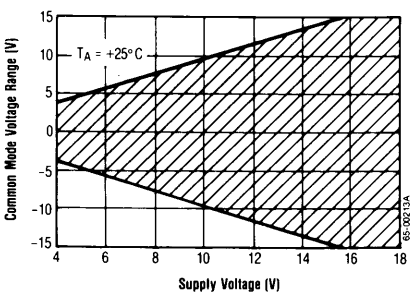
Input Bias Current as a Function of Ambient Temperature



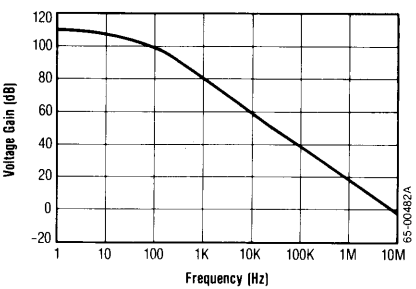
Input Offset Current as a Function of Ambient Temperature



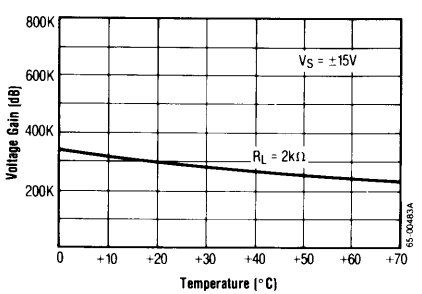
Common Mode Range as a Function of Supply Voltage



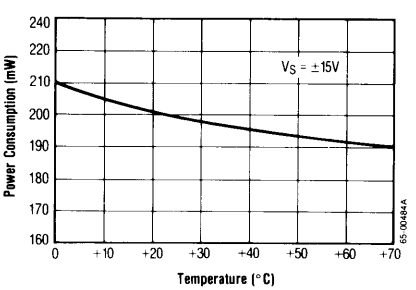
Open Loop Voltage Gain as a Function of Frequency



Open Loop Gain as a Function of Temperature

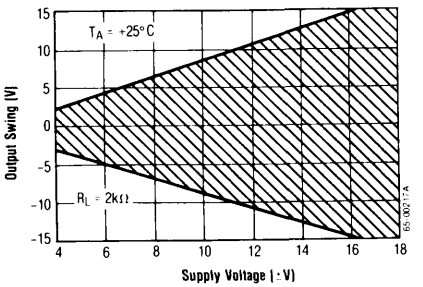


Power Consumption as a Function of Ambient Temperature

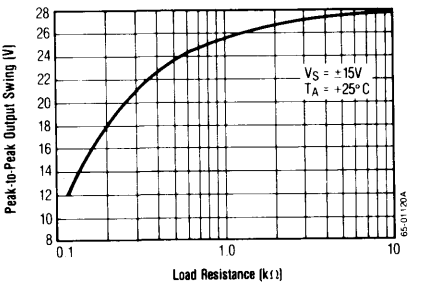


Typical Performance Characteristics (Continued)

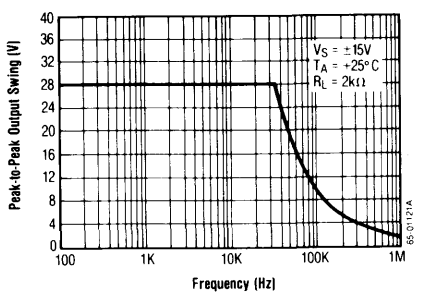
Typical Output Voltage as a Function of Supply Voltage



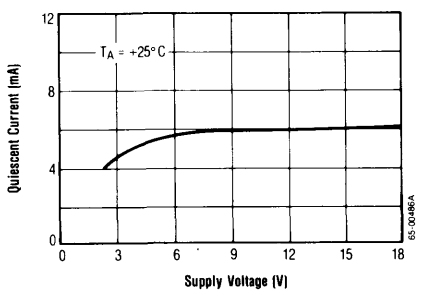
Output Voltage Swing as a Function of Load Resistance



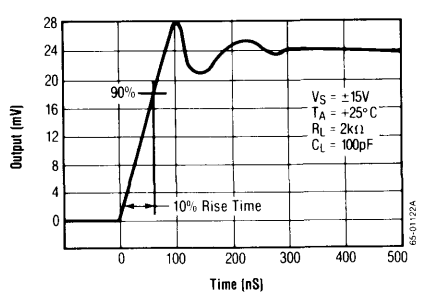
Output Voltage Swing as a Function of Frequency



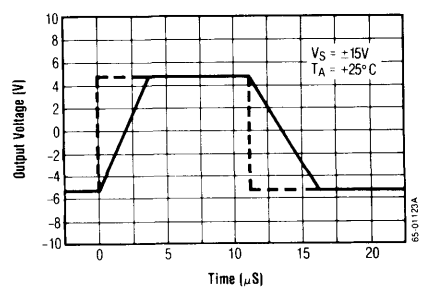
Quiescent Current as a Function of Supply Voltage



Transient Response

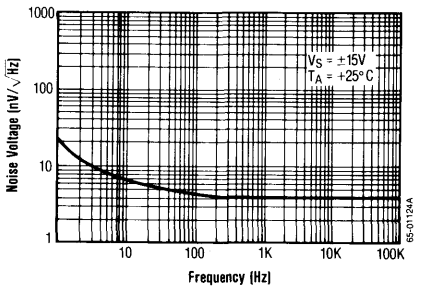


Voltage Follower Large Signal Pulse Response

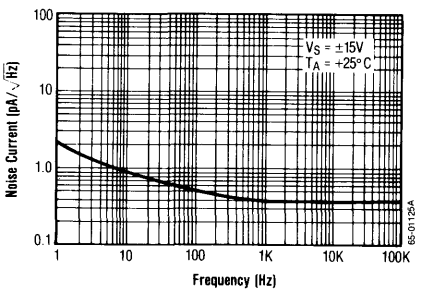


Typical Performance Characteristics (Continued)

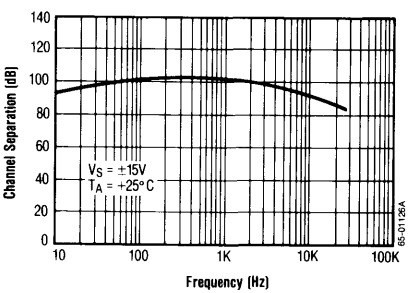
Input Noise Voltage as a Function of Frequency



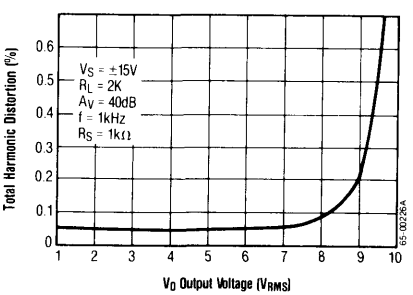
Input Noise Current as a Function of Frequency



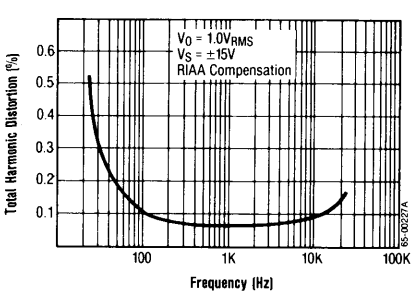
Channel Separation



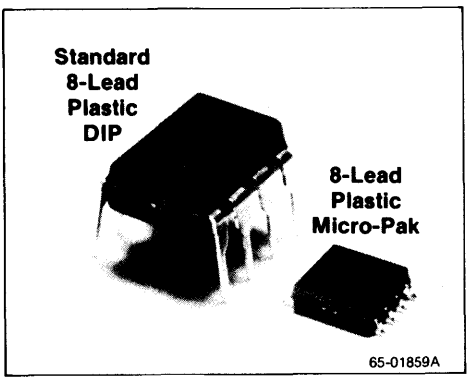
Total Harmonic Distortion vs. Output Voltage



Distortion vs. Frequency



Comparison of Standard vs. Micro-Package



Raytheon

High-Performance, Low-Noise Dual Operational Amplifier

RC2043

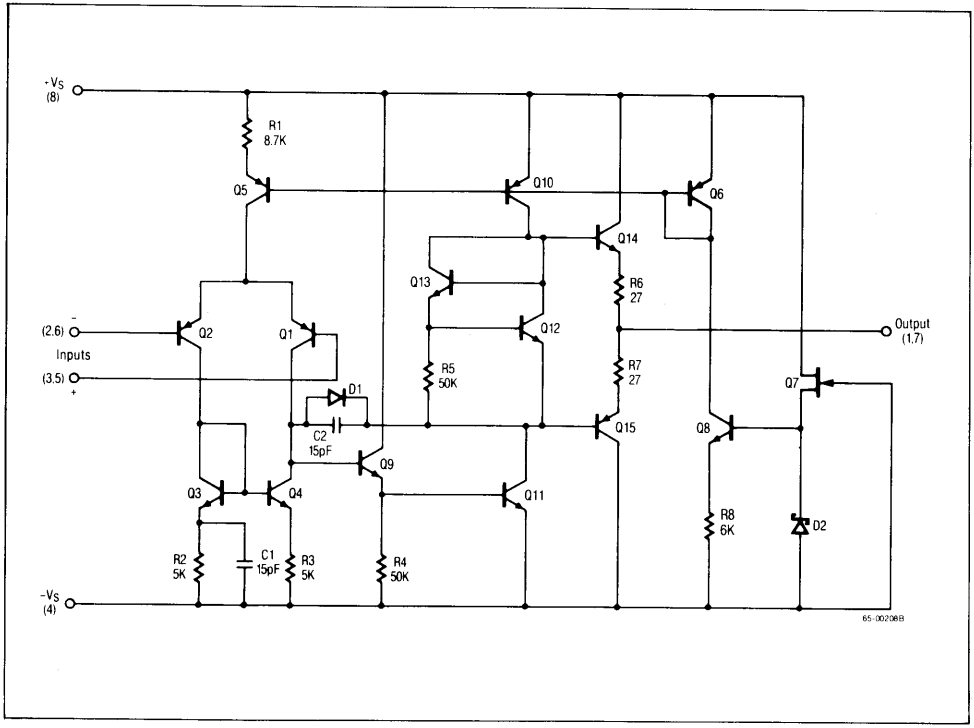
Features

- 14MHz unity gain bandwidth (A_V = 1)
- 6.0V/μS slew rate
- 3.5nV/$\sqrt{Hz}$ noise voltage at 1kHz
- 0.4pA/$\sqrt{Hz}$ noise current at 1kHz
- ±10V output into 400Ω loads (±25mA)
- 3.0mA supply current per amplifier
- Unity gain frequency compensated
- Output short circuit protected

Description

The 2043 integrated circuit is a high gain, wide-bandwidth, low-noise dual operational amplifier capable of driving 20V peak-to-peak into 400Ω loads. The 2043 combines many of the features of the 4558 as well as providing a wider bandwidth, lower noise, higher slew rate and higher output drive capability. The combination of low noise and wide bandwidth make the 2043 ideal for audio preamplifiers, active filters, telecommunications, and many instrumentation applications. The availability of the 2043 in the surface mounted micro package allows very high packing densities in critical applications.

Schematic Diagram (1/2 Shown)

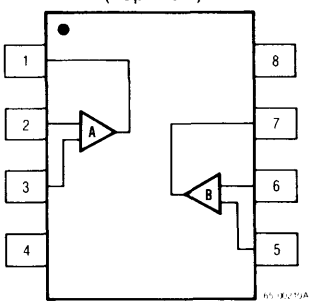


RC2043

High-Performance, Low-Noise Dual Operational Amplifier

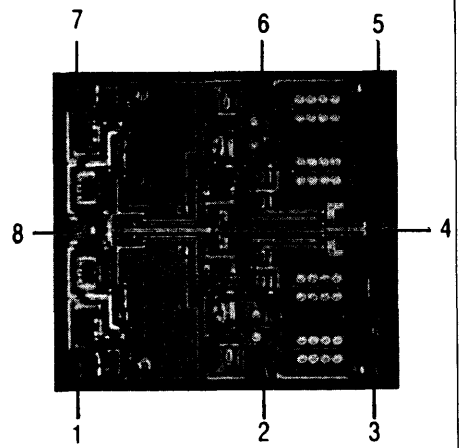
Connection Information

8-Lead
Dual In-Line Package
(Top View)



Pin	Function
1	A Output
2	A -Input
3	A +Input
4	$-V_S$
5	B +Input
6	B -Input
7	B Output
8	$+V_S$

Mask Pattern



Die Size: 52 x 61 mils
Min. Pad Dimensions: 4 x 4 mils

Thermal Characteristics

	8-Lead Micro-Pak Plastic DIP	8-Lead Plastic DIP
Max. Junction Temp.	125°C	125°C
Max. P_D $T_A < 50°C$	300mW	468mW
Therm. Res. θ_{JC}	—	—
Therm. Res. θ_{JA}	240°C/W	160°C/W
For $T_A > 50°C$ Derate at	4.17mW per °C	6.25mW per °C

Ordering Information

Part Number	Package	Operating Temperature Range
RC2043M	Micro-Plastic	-20°C to +75°C
RC2043NB	Plastic	-20°C to +75°C

Absolute Maximum Ratings

Supply Voltage ..... ±18V
Input Voltage[1] ..... ±15V
Differential Input Voltage 30V
Output Short Circuit Duration[2] ..... Indefinite
Operating Temperature
Range ..... -20°C to +75°C
Lead Soldering Temperature (10 Sec)
RC2043NB ..... +300°C
RC2043M ..... +260°C

Notes: 1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Short circuit may be to ground on one amp only. Rating applies to +75°C ambient temperature.

Matching Characteristics

(V_S = ±15V, T_A = +25°C)

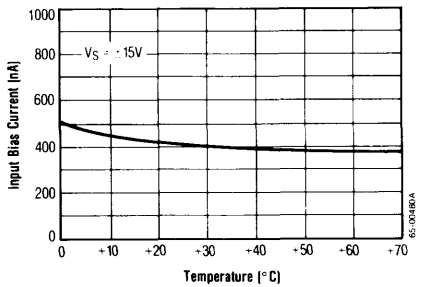
Parameter	Conditions	Typ	Units
Large Signal Voltage Gain	$R_L \geq 2k\Omega$	±1.0	dB
Input Bias Current		±15	nA
Input Offset Current		±7.5	nA
Input Offset Voltage	$R_L \geq 10k\Omega$	±0.2	mV

Electrical Characteristics (V_S = ±15V and T_A = +25° C unless otherwise specified)

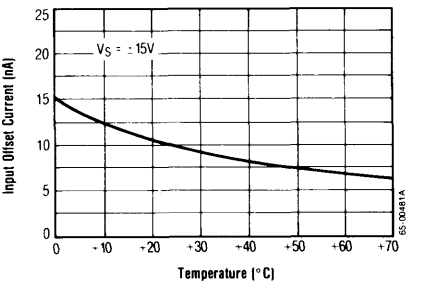
Parameters	Test Conditions	Min	Typ	Max	Units
Input Offset Voltage	$R_S \leq 10k\Omega$		0.3	3.0	mV
Input Offset Current			10	200	nA
Input Bias Current			400	1000	nA
Input Resistance (Differential Mode)		0.3	1.0		MΩ
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	20	100		V/mV
Output Voltage Swing	$R_L \geq 10k\Omega$	±12	±14		V
	I_O = 25mA	±10	±11.5		
Input Voltage Range		±12	±14		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	100		dB
Power Supply Rejection Ratio	$R_S \leq 10k\Omega$	76	100		dB
Power Consumption	$R_L = \infty$		180	240	mW
Transient Response Rise Time	V_{IN} = 20mV, R_L = 2kΩ		40		nS
Overshoot	$C_L \leq 100pF$		70		%
Slew Rate	$R_L \geq 2k\Omega$		6.0		V/μS
Channel Separation	f = 10kHz, R_S = 1kΩ, Gain = 100		90		dB
Unity Gain Bandwidth	Gain = 1	8.0	14		MHz
The following specifications apply for -20° C ≤ T_A ≤ +75° C					
Input Offset Voltage	$R_S \leq 10k\Omega$			4.5	mV
Input Offset Current				300	nA
Input Bias Current				1300	nA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	15			V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	±10			V
Power Consumption	T_A = +75° C		160	220	mW
	T_A = -20° C		210	260	

Typical Performance Characteristics

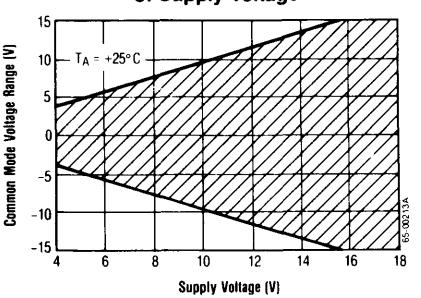
Input Bias Current as a Function of Ambient Temperature



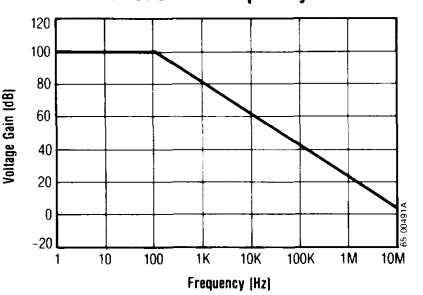
Input Offset Current as a Function of Ambient Temperature



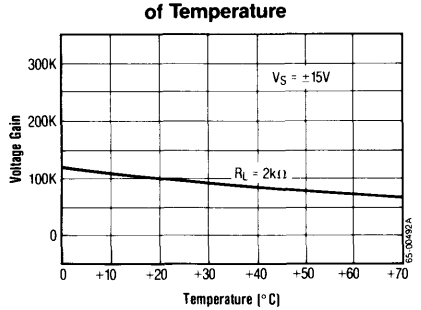
Common Mode Range as a Function of Supply Voltage



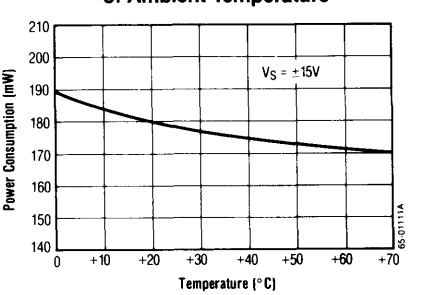
Open Loop Voltage Gain as a Function of Frequency



Open Loop Gain as a Function of Temperature

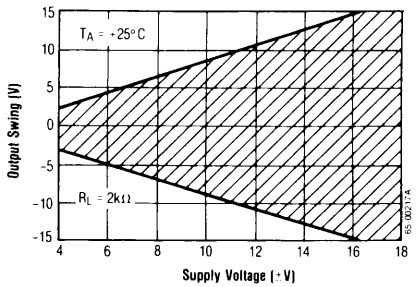


Power Consumption as a Function of Ambient Temperature

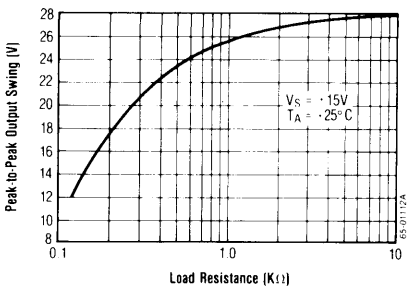


Typical Performance Characteristics (Continued)

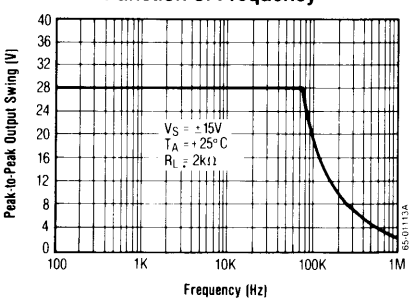
Typical Output Voltage as a Function of Supply Voltage



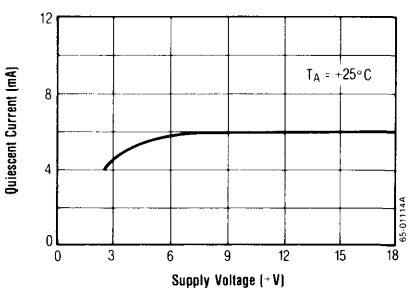
Output Voltage Swing as a Function of Load Resistance



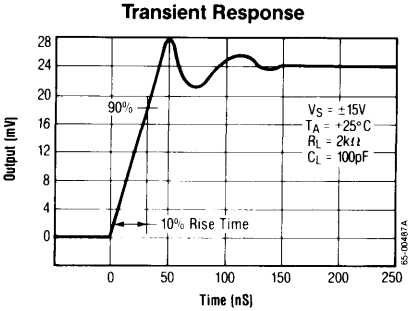
Output Voltage Swing as a Function of Frequency



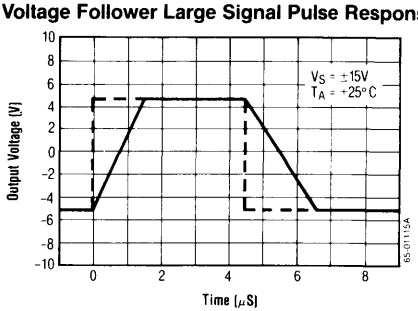
Quiescent Current as a Function of Supply Voltage



Transient Response

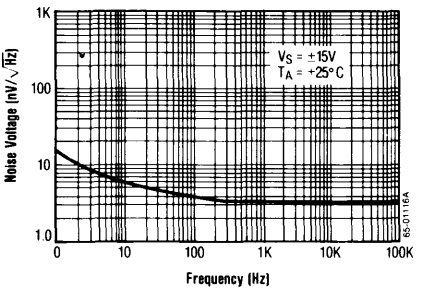


Voltage Follower Large Signal Pulse Response

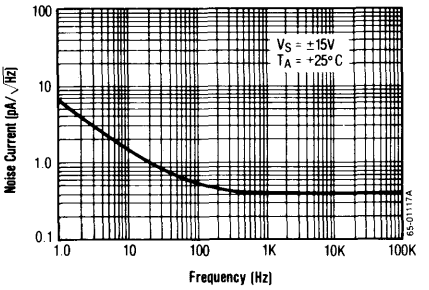


Typical Performance Characteristics (Continued)

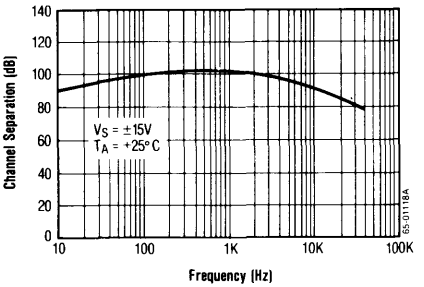
Input Noise Voltage as a Function of Frequency



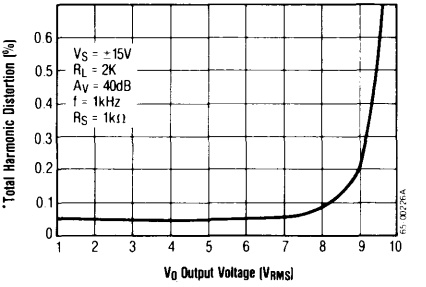
Input Noise Current as a Function of Frequency



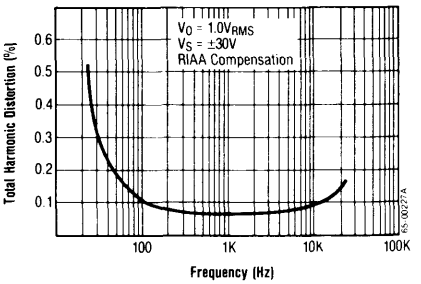
Channel Separation



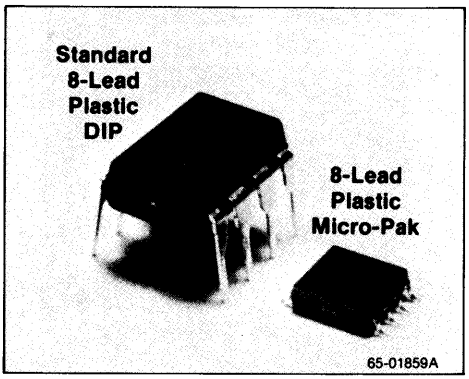
Total Harmonic Distortion vs. Output Voltage



Distortion vs. Frequency



Comparison of Standard vs. Micro-Package



Raytheon

Micro-Power Operational Amplifier

RC3078, RM3078A

Features

- Low standby power — as low as 700nW
- Wide supply voltage range — ±0.75V to ±15V
- High peak output current — 6.5mA minimum
- Adjustable quiescent current
- Output short circuit protection

Applications

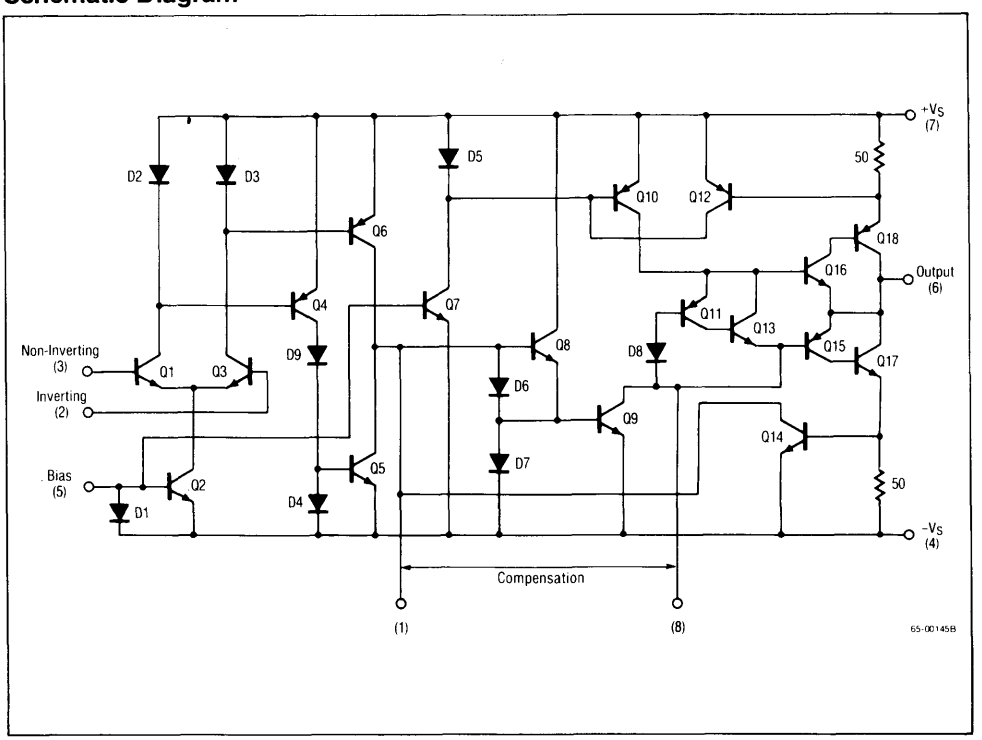
- Portable electronics
- Medical electronics
- Instrumentation
- Telemetry

Description

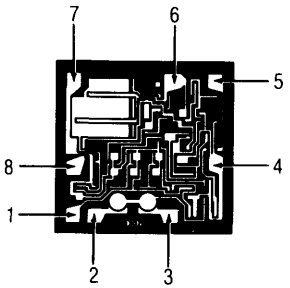
The 3078 and 3078A are high gain monolithic operational amplifiers which can deliver milliamperes of current yet only consume microwatts of standby power. Their operating points are externally adjustable and frequency compensation may be accomplished with one external capacitor. The 3078 and 3078A provide the designer with the opportunity to tailor the frequency response and improve the slew rate without sacrificing power. Operation with a single 1.5V battery is a practical reality with these devices.

The 3078A is a premium device having a supply voltage range of V_S = ±0.75V to V_S = ±15V and an operating temperature range of -55° C to +125° C. The 3078 has the same lower supply voltage limit but the upper limit is $+V_S$ = +6V and $-V_S$ = -6V. The operating temperature range is from 0° C to +70° C

Schematic Diagram



Mask Pattern



Die Size: 49 x 48 mils
Min. Pad Dimensions: 4 x 4 mils

Absolute Maximum Ratings

Supply Voltage
RC3078 ..... ±7V
RM3078A ..... ±18V
Input Voltage ..... $+V_S$ to $-V_S$
Differential Input Voltage 6V
Input Signal Current 0.1mA
Output Short Circuit
Duration* ..... No Limitation
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
RC3078 ..... 0°C to +70°C
RM3078A ..... -55°C to +125°C
Lead Soldering Temperature
(10 Sec) ..... +300°C

*Short circuit may be applied to ground or to either supply.

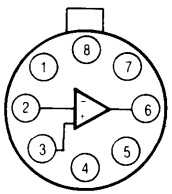
Ordering Information

Part Number	Package	Operating Temperature Range
RC3078DE	Ceramic	0°C to +70°C
RC3078NB	Plastic	0°C to +70°C
RC3078T	TO-99	0°C to +70°C
RM3078ADE	Ceramic	-55°C to +125°C
RM3078AT	TO-99	-55°C to +125°C
RM3078AT/883B*	TO-99	-55°C to +125°C

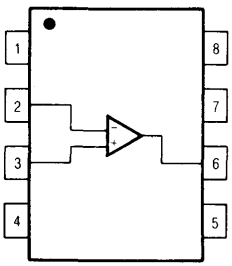
*MIL-STD-883, Level B Processing

Connection Information

8-Lead Metal Can TO-99 (Top View)



8-Lead Dual In-Line Package (Top View)



65-00147A

Pin	Function
1	Compensation
2	Inverting Input
3	Non-Inverting Input
4	$-V_S$
5	Bias
6	Output
7	$+V_S$
8	Compensation

Thermal Characteristics

	8-Lead Plastic DIP	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can
Max. Junction Temp.	125°C	175°C	175°C
Max. P_D T_A < 50°C	468mW	833mW	658mW
Therm. Res. θ_{JC}	—	45°C/W	50°C/W
Therm. Res. θ_{JA}	160°C/W	150°C/W	190°C/W
For T_A > 50°C Derate at	6.25mW per °C	8.33mW per °C	5.26mW per °C

Electrical Characteristics (V_S = ±6V)

Parameters	Test Conditions	RM3078A R_{SET} = 5.1MΩ, I_Q = 20μA					RC3078 R_{SET} = 1MΩ, I_Q = 100μA					Units
		T_A = +25°C			T_A = -55°C to +125°C		T_A = +25°C			T_A = 0°C to +70°C		
		Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	
Input Offset Voltage	$R_S \leq 10k\Omega$		0.70	3.5		4.5		1.3	4.5		5.0	mV
Input Offset Current			0.50	2.5		5.0		6.0	32		40	nA
Input Bias Current			7.0	12		50		60	170		200	nA
Large Signal Voltage Gain	$R_L \geq 10k\Omega$	39	100		31		25	39		20		V/mV
Supply Current			20	35		100		100	130		150	μA
Power Consumption			240	300		540		1200	1560		1800	μW
Output Voltage Swing	$R_L \geq 10k\Omega$	±5.1	±5.3		±5.0		±5.1	±5.3		±5.0		V
Input Voltage Range	$R_S \leq 10k\Omega$		-5.5 to +5.8		-5 to +5			-5.5 to +5.8		-5 to +5		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	80	115				80	110				dB
Output Current			12		5.0	30		12		5.0	30	mA
Power Supply Rejection Ratio Positive Supply	$R_S \leq 10k\Omega$	76	104				76	93				dB
NegativeSupply		76	104				76	93				

(R_{SET} = 13MΩ, I_Q = 20μA, V_S = ±15V)

Input Offset Voltage	$R_S \leq 10k\Omega$		1.4	3.5		4.5						mV
Large Signal Voltage Gain	$R_L \geq 10k\Omega$	32	100		25							V/mV
Supply Current			20	35		100						μA
Power Dissipation			600	750		1350						μW
Output Voltage Swing	$R_L \geq 10k\Omega$	13.7	14.1		13.5							V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	80	106									dB
Input Bias Current			7.0	14		55						nA
Input Offset Current			0.50	2.7		5.5						nA

Electrical Characteristics (At T_A = +25°C)

Parameters	Typical Values				Units
	RM3078A		RC3078		
	V_S = ±1.3V, R_{SET} = 2MΩ	V_S = ±0.75V, R_{SET} = 10MΩ	V_S = ±1.3V, R_{SET} = 2MΩ	V_S = ±0.75V, R_{SET} = 10MΩ	
Input Offset Voltage	0.7	0.9	1.3	1.5	mV
Input Offset Current	0.3	0.054	1.7	0.5	nA
Input Bias Current	3.7	0.45	9.0	1.3	nA
Large Signal Voltage Gain	16	1.8	10	1.0	V/mV
Supply Current	10	1.0	10	1.0	μA
Power Consumption	26	1.5	26	1.5	μW
Output Voltage Swing	1.4	0.3	1.4	0.3	V
Input Voltage Range	-0.8 to +1.1	-0.2 to +0.5	-0.8 to +1.1	-0.2 to +0.5	V
Common Mode Rejection Ratio	100	90	100	90	dB
Output Current	12	0.5	12	0.5	mA
Power Supply Rejection Ratio	94	86	94	86	dB

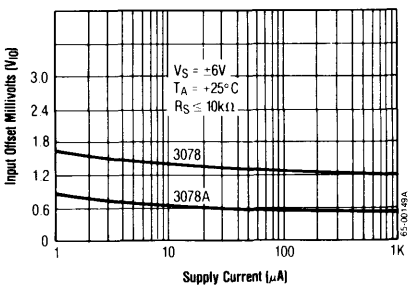
Electrical Characteristics

(Typical values intended only for design guidance at T_A = +25°C and V_S = ±6V)

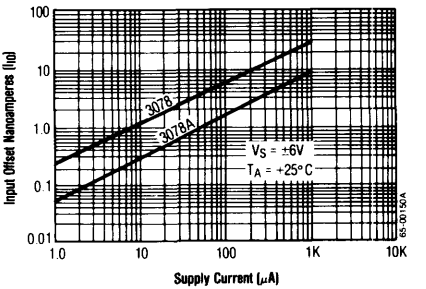
Parameters	Test Conditions	RM3078A		RC3078	Units
		R_{SET} = 5.1MΩ I_Q = 20μA	R_{SET} = 1MΩ I_Q = 100μA	R_{SET} = 5.1MΩ I_Q = 100μA	
Input Offset Voltage Drift	$R_S \leq$ 10kΩ	5.0	6.0	6.0	μV/°C
Input Offset Current Drift	$R_S \leq$ 10kΩ	6.3	70	70	pA/°C
Unity Gain Bandwidth	A_V = -3dB	0.3	2.0	2.0	kHz
Slew Rate					V/μS
Unity Gain		0.027	0.04	0.04	
Comparator	10% to 90%	0.5	1.5	1.5	
Rise Time		3.0	2.5	2.5	μS
Input Resistance (Differential Mode)		7.4	1.7	0.87	MΩ
Open Loop Output Resistance		1.0	0.8	0.8	kΩ
Input Noise Voltage Density	R_S = 0	36		19	nV/$\sqrt{Hz}$
Input Noise Current Density	R_S = 1MΩ	0.4		1.0	pA/$\sqrt{Hz}$

Typical Performance Characteristics

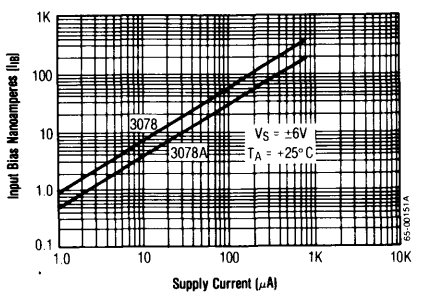
Input Offset Voltage vs. Total Quiescent Current



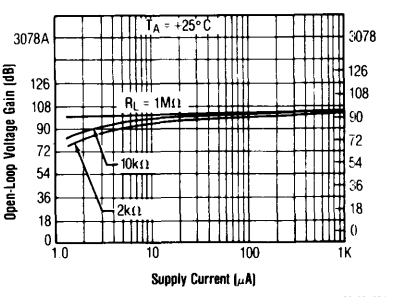
Input Offset Current vs. Total Quiescent Current



Input Bias Current vs. Total Quiescent Current

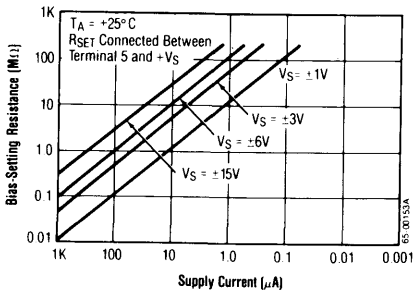


Open Loop Voltage Gain vs. Total Quiescent Current

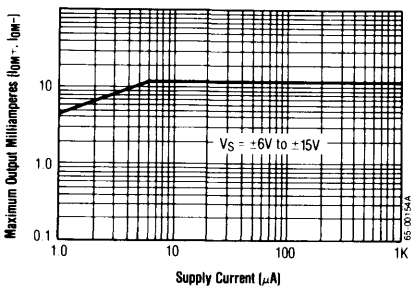


Typical Performance Characteristics (Continued)

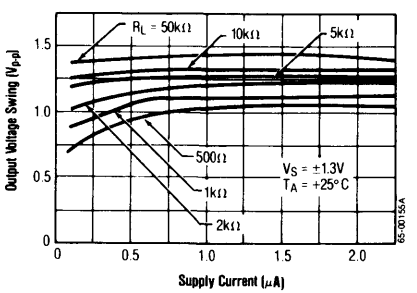
Bias-Setting Resistance vs. Total Quiescent Current



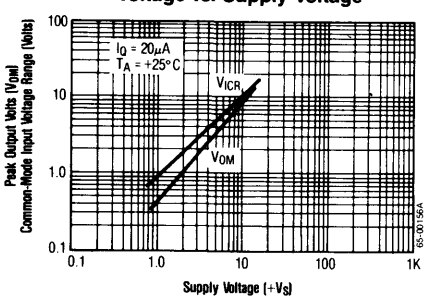
Maximum Output Current vs. Total Quiescent Current



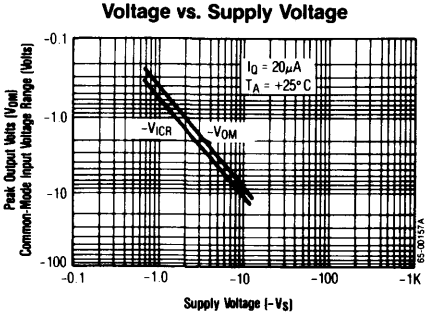
Output Voltage Swing vs. Total Quiescent Current



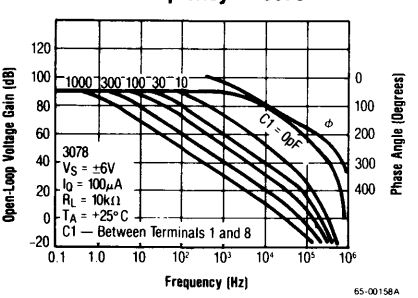
Positive Output and Common Mode Voltage vs. Supply Voltage



Negative Output and Common Mode Voltage vs. Supply Voltage

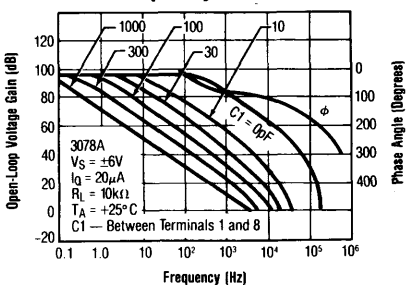


Open Loop Voltage Gain vs. Frequency — 3078

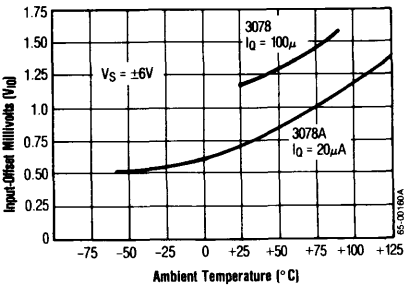


Typical Performance Characteristics (Continued)

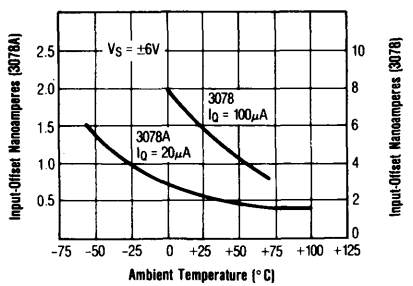
Open Loop Voltage Gain vs. Frequency — 3078A



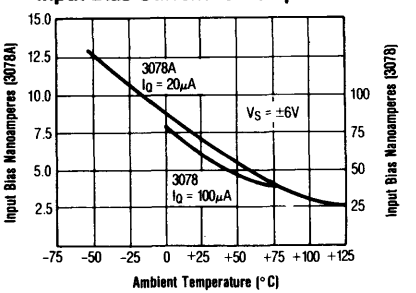
Input Offset Voltage vs. Temperature



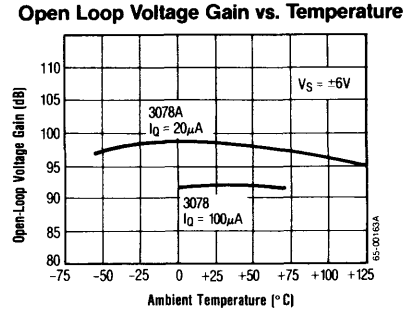
Input Offset Current vs. Temperature



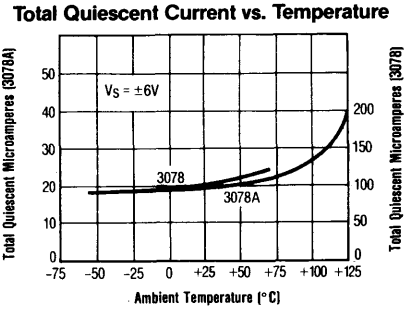
Input Bias Current vs. Temperature



Open Loop Voltage Gain vs. Temperature

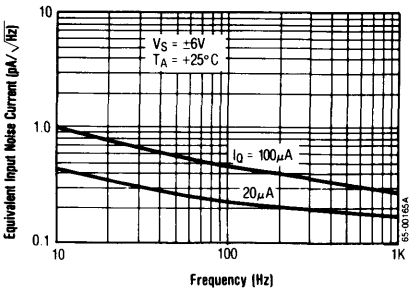


Total Quiescent Current vs. Temperature

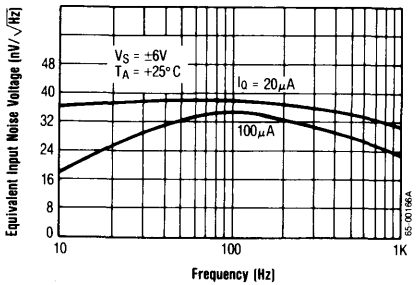


Typical Performance Characteristics (Continued)

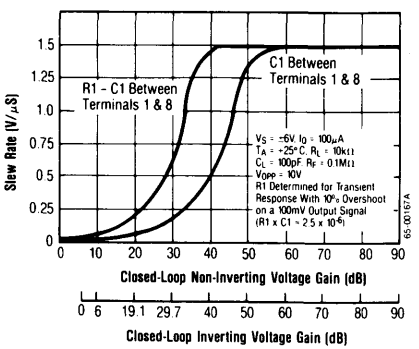
Equivalent Input Noise Current vs. Frequency



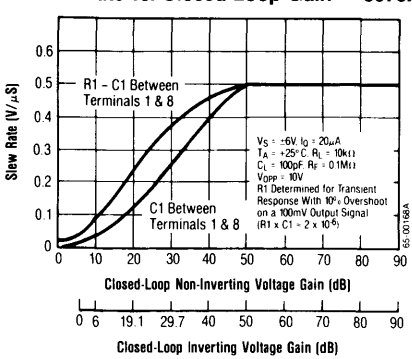
Equivalent Input Noise Voltage vs. Frequency



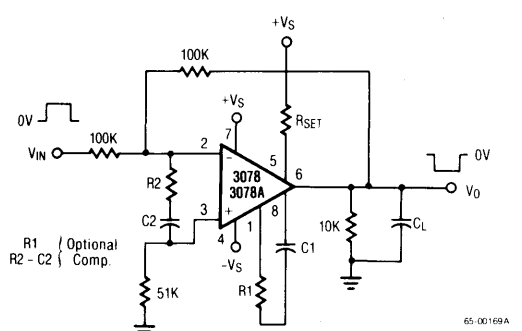
Slew Rate vs. Closed Loop Gain — 3078



Slew Rate vs. Closed Loop Gain — 3078A

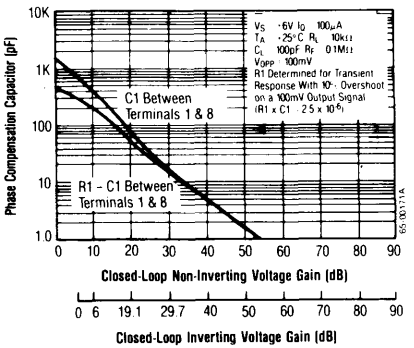


Transient Response and Slew Rate Unity Gain (Inverting) Test Circuit

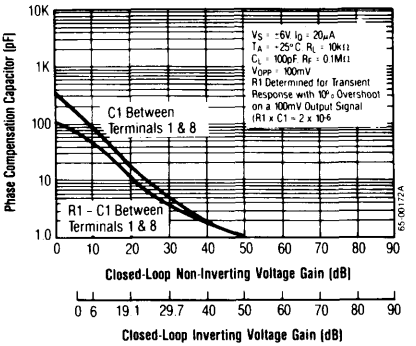


Typical Performance Characteristics (Continued)

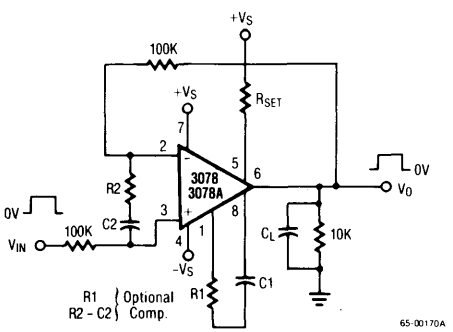
Phase Compensation Capacitance vs. Closed Loop Gain — 3078



Phase Compensation Capacitance vs. Closed Loop Gain — 3078A



Slew Rate, Unity Gain (Non-Inverting) Test Circuit



Operating Considerations

The 3078 and 3078A can be phase-compensated with one or two external components depending upon the closed-loop gain, power consumption, and speed desired. The recommended compensation is a resistor in series with a capacitor connected from terminal 1 to terminal 8. Values of the resistor and capacitor as required for compensation are a function of closed-loop gain. These curves represent the compensation necessary at quiescent currents of 20μA and 100μA, respectively, for a transient with 10% overshoot. The slew rates curves show what can be obtained with the two different compensation techniques. Higher speeds can be achieved with input compensation, but this increases noise output. Compensation can also be accomplished with a single capacitor connected from terminal 1 to terminal 8, with speed being sacrificed for simplicity. Table 1 gives an indication of slew rates that can be obtained with various compensation techniques at quiescent currents of 20μA and 100μA.

Single Supply Operation

The 3078 and 3078A can operate from a single supply with a minimum total supply voltage of 1.5V. Figures 2 and 3 show the 3078 and 3078A in inverting and non-inverting 20dB amplifier configurations utilizing a 1.5V type "A" cell for a supply. The total power consumption for either circuit is approximately 675 nanowatts. The output voltage swing in this configuration is 300mV$_{p-p}$ with a 20kΩ load.

Table 1. Unity Gain Slew Rate Versus Compensation — 3078 and 3078A

V_S = ±6V R_L = 10kΩ	Transient Response: 10% Overshoot for an Output Voltage of 100mV, T_A = +25°C									
	Unity Gain (Inverting)					Unity Gain (Non-Inverting)				
Compensation Technique	$\frac{1}{R1}$	C1	R2	C2	Slew Rate	R1	C1	R2	C2	Slew Rate
3078 — I_Q = 100μA	kΩ	pF	kΩ	μF	V/μS	kΩ	pF	kΩ	μF	V/μS
Single Capacitor	0	750	∞	0	0.0085	0	1500	∞	0	0.0095
Resistor and Capacitor	3.5	350	∞	0	0.04	5.3	500	∞	0	0.024
Input	∞	0	0.25	0.306	0.67	∞	0	0.311	0.45	0.67
3078A — I_Q = 20μA										
Single Capacitor	0	300	∞	0	0.0095	0	800	∞	0	0.003
Resistor and Capacitor	14	100	∞	0	0.027	34	125	∞	0	0.02
Input	∞	0	0.644	0.156	0.29	∞	0	0.77	0.4	-0.4

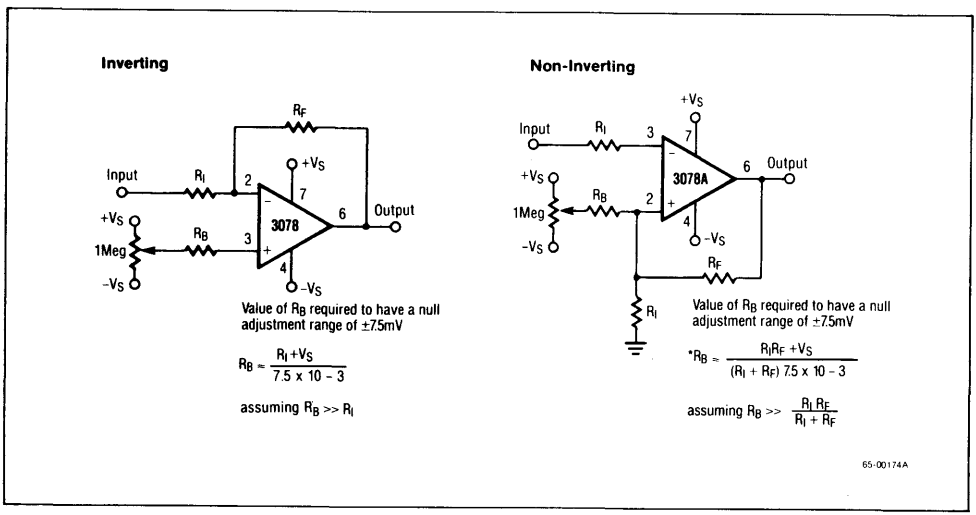


Figure 1. Offset Voltage Null Circuit

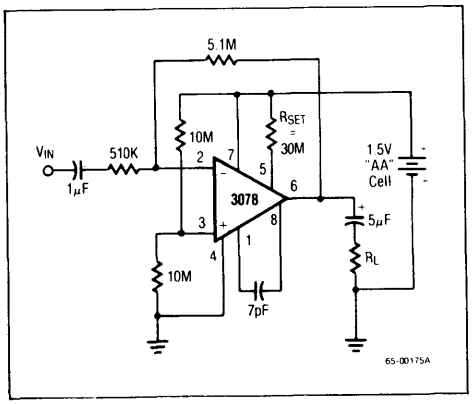


Figure 2. Inverting 20dB Amplifier Circuit

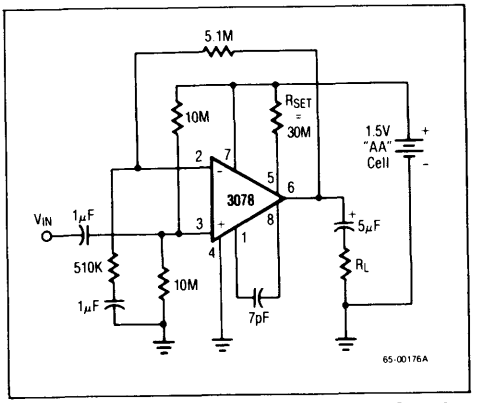


Figure 3. Non-Inverting 20dB Amplifier Circuit

Raytheon

Ground Sensing Quad Operational Amplifier

RC3403A, RM3503A

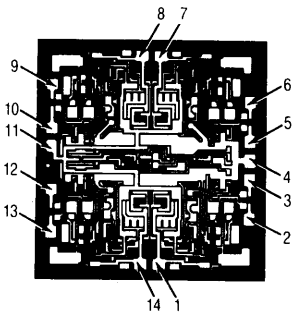
Features

- Class AB output stage — no crossover distortion
- Output voltage swings to ground in single supply operation
- High slew rate — 1.2V/μS
- Single or split supply operation
- Wide supply operation — +2.5V to +36V or ±1.25V to ±18V
- Pin compatible with LM324 and MC3403
- Low power consumption — 0.8mA/amplifier
- Common mode range includes ground

Description

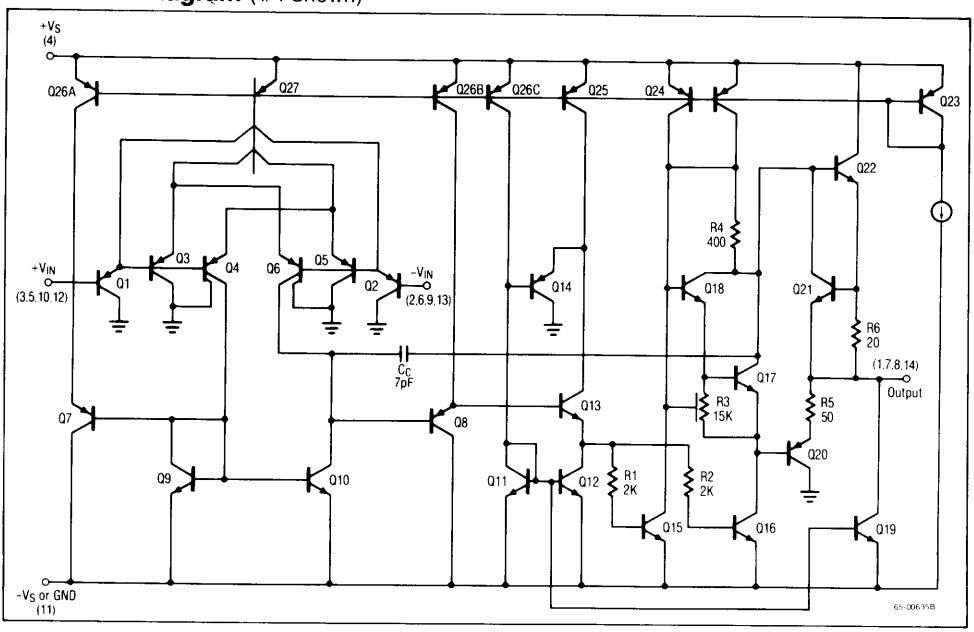
The RC/RV3403A and RM3503A are high performance ground sensing quad operational amplifiers featuring improved DC specifications equal to or better than the standard 741 type general purpose op amp. The ground sensing differential input stage of these op amps provides increased slew rate compared to 741 types.

Mask Pattern



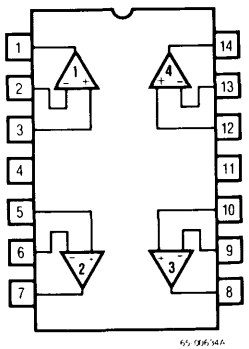
Die Size: 80 x 84 mils
Min. Pad Dimensions: 4 x 4 mils

Schematic Diagram (1/4 Shown)



Connection Information

14-Lead
Dual In-Line Package
(Top View)



Pin	Function
1	Output 1
2	-Input 1
3	+Input 1
4	$+V_S$
5	+Input 2
6	-Input 2
7	Output 2
8	Output 3
9	-Input 3
10	+Input 3
11	$-V_S$ (GND)
12	+Input 4
13	-Input 4
14	Output 4

Thermal Characteristics

	14-Lead Plastic DIP	14-Lead Ceramic DIP
Max. Junction Temp.	125°C	175°C
Max. P_D $T_A < 50°C$	468mW	1042mW
Therm. Res. θ_{JC}	—	60°C/W
Therm. Res. θ_{JA}	160°C/W	120°C/W
For $T_A > 50°C$ Derate at	6.25mW per °C	8.33mW per °C

Absolute Maximum Ratings

Supply Voltage ..... +36V or ±18V
Input Voltage ..... -0.3V to +36V
Differential Input Voltage 36V
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
RM3503A ..... -55°C to +125°C
RC3403A ..... 0°C to +70°C
RV3403A ..... -40°C to +85°C
Lead Soldering Temperature
(60 Sec) ..... +300°C

Ordering Information

Part Number	Package	Operating Temperature Range
RC3403ADC	Ceramic	0°C to +70°C
RC3403ADB	Plastic	0°C to +70°C
RV3403ADB	Plastic	-40°C to +85°C
RM3503ADC	Ceramic	-55°C to +125°C
RM3503ADE/883*	Ceramic	-55°C to +125°C

*MIL-STD-883, Level B Processing

Low Voltage Electrical Characteristics (V_S = +5V, $-V_S$ = GND, and T_A = +25°C)

Parameters	Test Conditions	RM3503A			RC/RV3403A			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 0\Omega$		2.0	5.0		2.0	10	mV
Input Bias Current			-150	-500		-150	-500	nA
Input Offset Current			30	50		30	50	nA
Supply Current	$R_L = \infty$ All Amplifiers		2.5	4.0		2.5	5.0	mA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$	20	200		20	200		V/mV
Output Voltage Swing[1]	$R_L \geq 10k\Omega$	3.5			3.5			V_{p-p}
Channel Separation	1kHz ≤ F ≤ 200kHz (Input Referred)		120			120		dB
Power Supply Rejection Ratio		86			76			dB

Note: 1. Output will swing to ground.

Electrical Characteristics Guaranteed Over Temperature (V_S = ±15V)

Parameters	Test Conditions	RM3503A			RC3403A			RV3403A			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 0\Omega$			6.0			10			10	mV
Input Bias Current				-1500			-800			-1500	nA
Input Offset Current				200			200			200	nA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$	25			15			15			V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	±10			±10			±10			V

Electrical Characteristics ($V_S = \pm 15V$, $T_A = +25°C$)

Parameters	Test Conditions	RM3503A			RC/RV3403A			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 0\Omega$		2.0	4.0*		2.0	6.0*	mV
Input Bias Current			-150	-400*		-150	-500	nA
Input Offset Current			30	±50		±30	±50	nA
Input Voltage Range		0		$+V_S-2$	0		$+V_S-2$	V
Supply Current	$R_L = \infty$ On All Op Amps		3.0	4.0		3.0	5.0*	mA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$	50	100		25*	100		V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	±13	±14		±13	±14		V
Common Mode Rejection Ratio	DC	70	90		70	90		dB
Channel Separation	1kHz to 20kHz		120			120		dB
Output Source Current	$V_{IN+} = 1V$, $V_{IN-} = 0V$	20	40		20	40		mA
Output Sink Current		10	20		10	20		mA
Unity Gain Bandwidth			1.0			1.0		MHz
Slew Rate	$A_V = 1$, $-10 \leq V_I < +10$		1.2*			1.2*		V/μS
Distortion (Crossover)	f = 20kHz, $V_O = 10V_{p-p}$		1.0			1.0		%
Power Bandwidth	$V_O = 10V_{p-p}$		40			40		kHz
Power Supply Rejection Ratio		86	94		80	94		dB

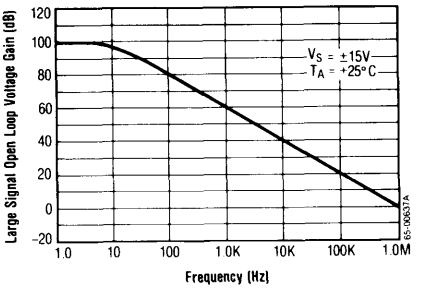
*Significantly improved performance.

Electrical Characteristics Comparison RC3403A, MC3403, LM324

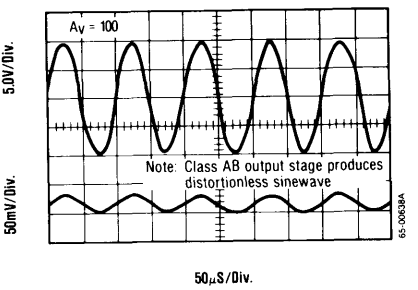
Max Ratings	RC3403A			MC3403			LM324			Units
Supply Voltage	+36 or ±18			+36 or ±18			+32 or ±16			V
Differential Input Voltage	36			36			32			V
Input Voltage	36			36			32			V
Electrical Characteristics	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Test Conditions		±15			±15			+5.0		V
Input Offset Voltage		2.0	6.0		2.0	8.0		2.0	7.0	mV
Input Offset Current		±30	±50		±30	±50		±5.0	±50	nA
Input Bias Current		150	500		200	500		45	500	nA
Input Voltage Range	0		$+V_S$ -2				0		$+V_S$ -1.5	V
Supply Current		3.0	5.0		2.8	7.0		0.8	2.0	mA
Large Signal Voltage Gain	25	100		20	200			100		V/mV
Output Voltage Swing	±13	±14		±1.0	±13				$+V_S$ -1.5	V
Common Mode Rejection Ratio	70	90		70	90			85		dB
Power Supply Rejection Ratio	80	94		76	90			100		dB
Unity Gain Bandwidth		1.0			1.0			1.0		MHz
Slew Rate		1.2			0.6			0.4		V/μS
Output Sink Current	10	20						20		mA
Output Source Current	20	40					20	40		mA
Channel Separation		120			120			120		dB
Distortion (Crossover)		1.0			1.0					%

Typical Performance Characteristics

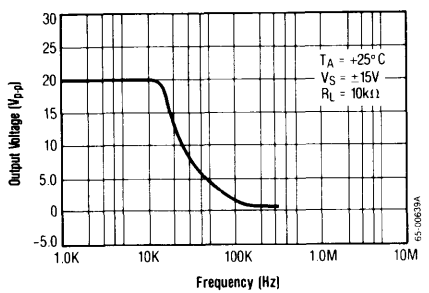
Large Signal Open Loop Voltage Gain as a Function of Frequency



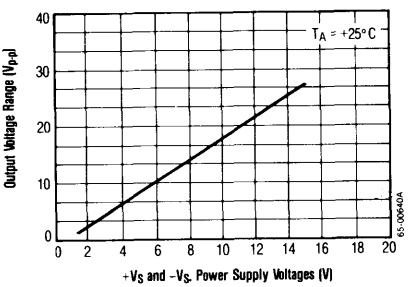
Sinewave Response



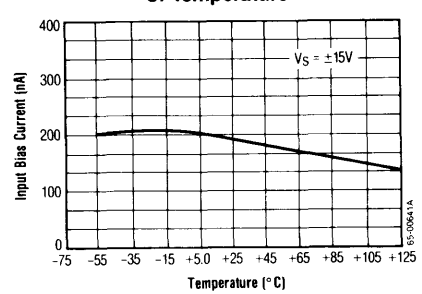
Output Voltage as a Function of Frequency



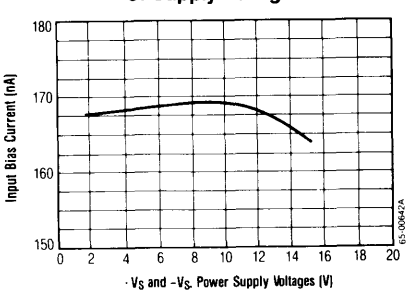
Output Swing as a Function of Supply Voltage



Input Bias Current as a Function of Temperature



Input Bias Current as a Function of Supply Voltage



Typical Applications

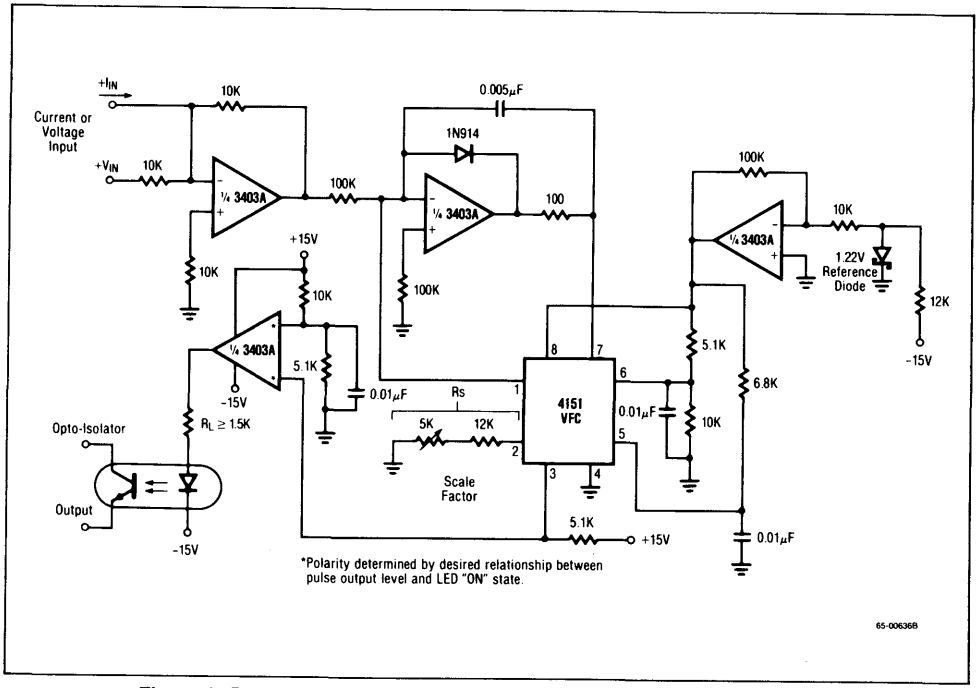


Figure 1. Precision Voltage-to-Frequency Converter With Isolated Output

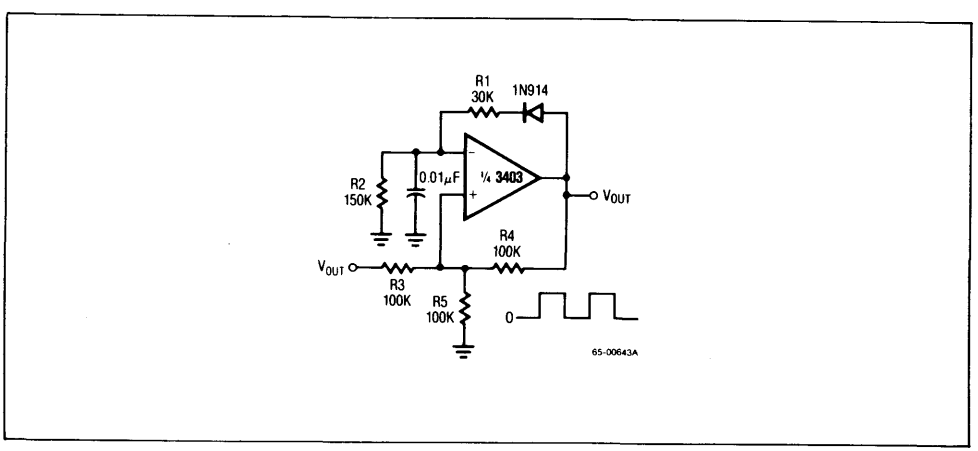


Figure 2. Pulse Generator

Typical Applications (Continued)

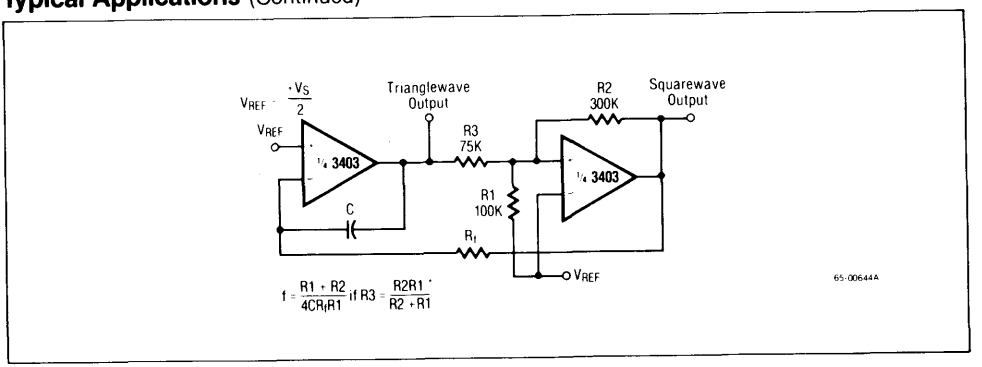


Figure 3. Function Generator

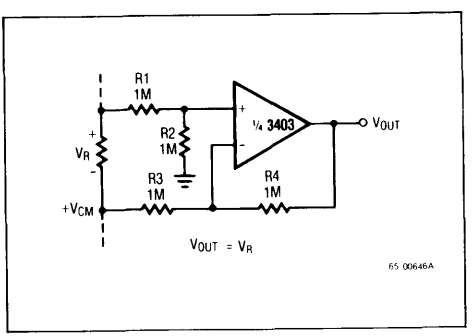


Figure 4. Ground Referencing a Differential Input Signal

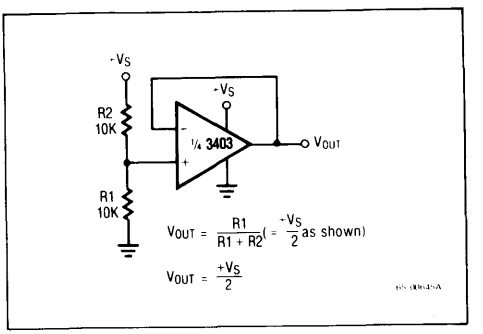


Figure 5. Voltage Reference

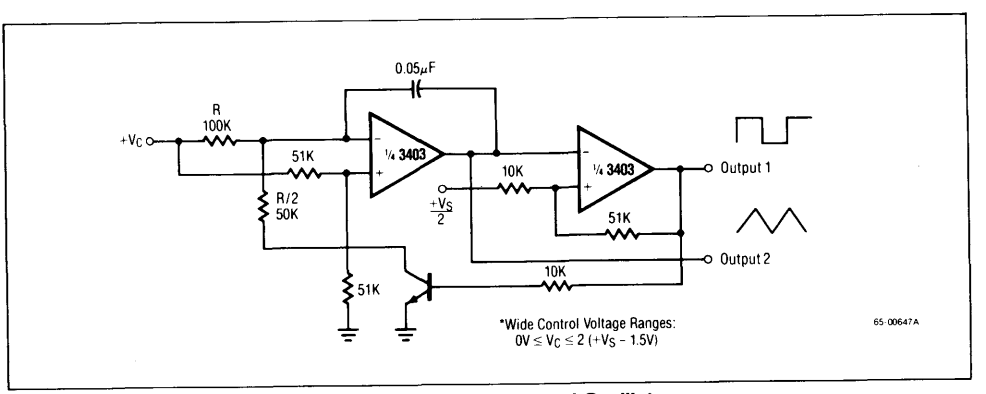


Figure 6. Voltage Controlled Oscillator

Typical Applications (Continued)

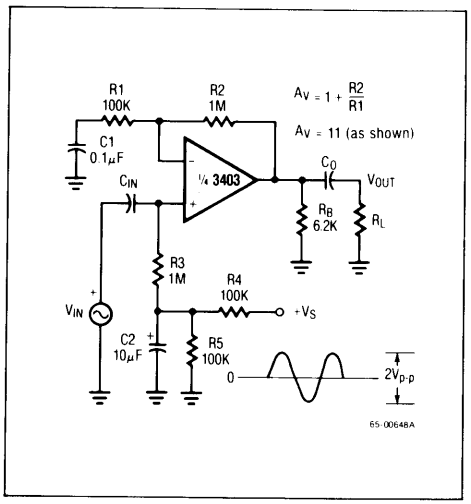


Figure 7. AC Coupled Non-Inverting Amplifier

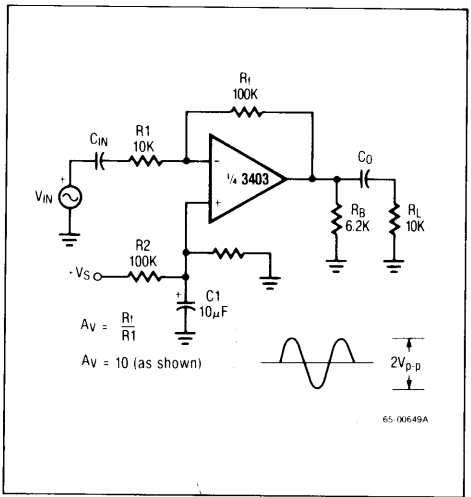


Figure 8. AC Coupled Inverting Amplifier

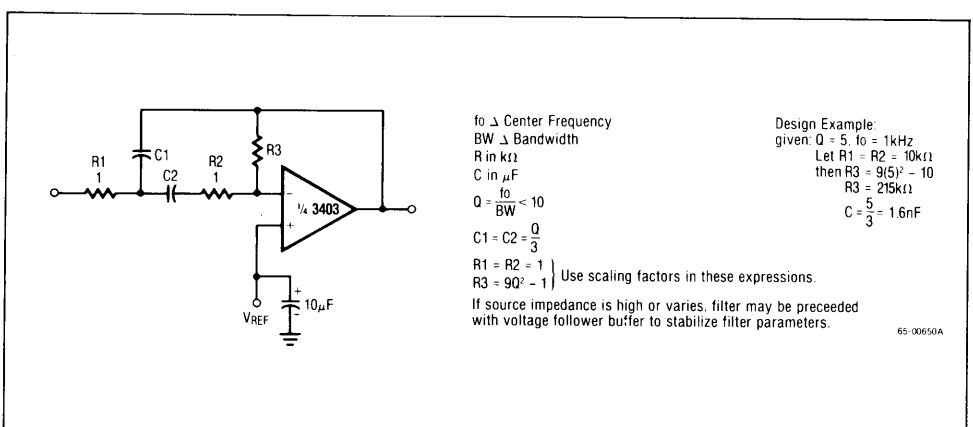


Figure 9. Multiple Feedback Bandpass Filter

Typical Applications (Continued)

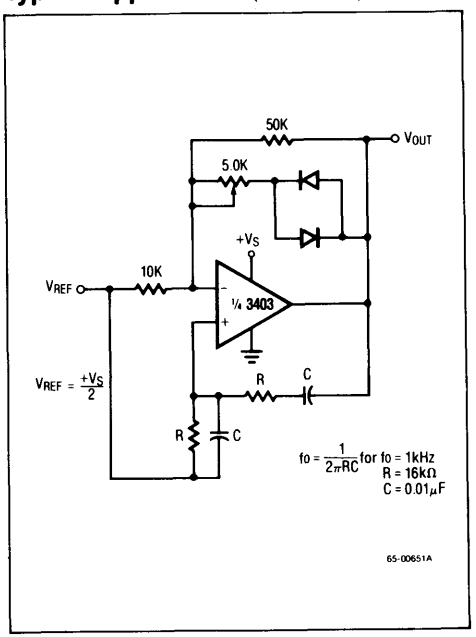


Figure 10. Wein Bridge Oscillator

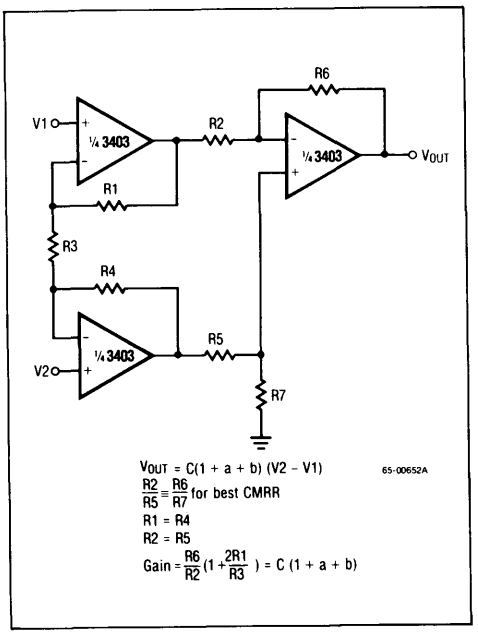


Figure 11. High Impedance Differential Amplifier

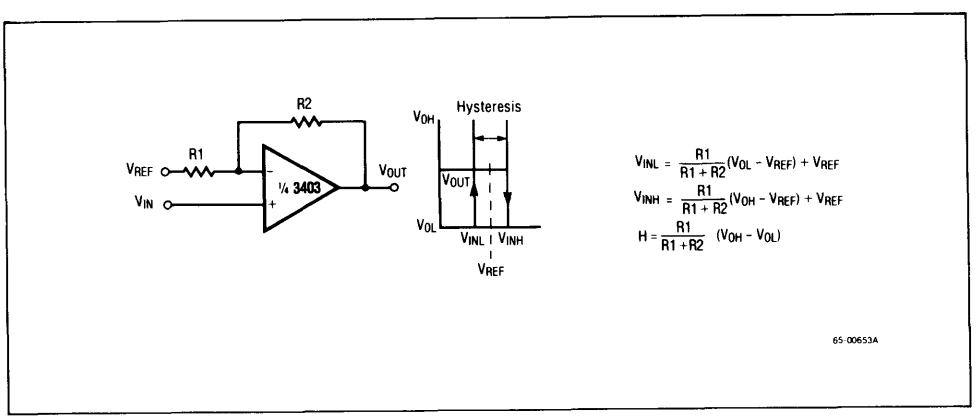


Figure 12. Comparator With Hysteresis

Typical Applications (Continued)

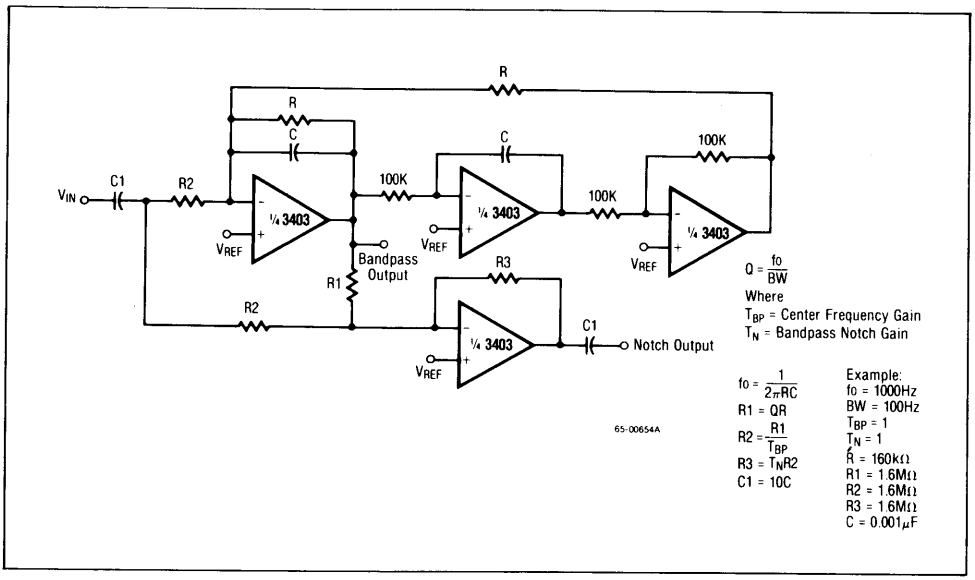


Figure 13. Bi-Quad Filter

Raytheon

General Purpose Quad 741 Operational Amplifier

RC4136

Features

- Unity gain bandwidth — 3MHz
- Short circuit protection
- No frequency compensation required
- No latch-up
- Large common mode and differential voltage ranges
- Low power consumption
- Parameter tracking over temperature range
- Gain and phase match between amplifiers

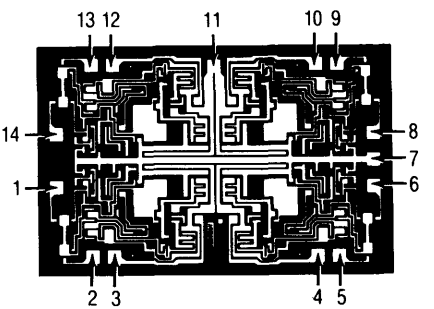
Description

The 4136 is made up of four 741 type independent high gain operational amplifiers internally compensated and constructed on a single silicon chip using the planar epitaxial process.

This amplifier meets or exceeds all specifications for 741 type amplifiers. Excellent channel separation allows the use of the 4136 quad amplifier in all 741 operational amplifier applications providing the highest possible packaging density.

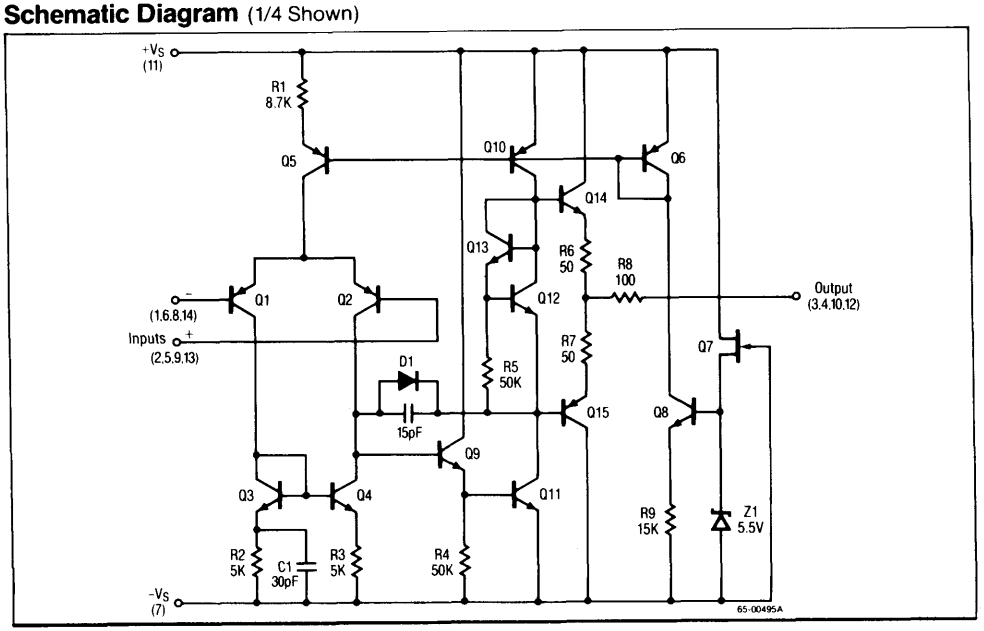
The specially designed low noise input transistors allow the 4136 to be used in low noise signal processing applications such as audio preamplifiers and signal conditioners.

Mask Pattern



Die Size: 99 x 64 mils
Min. Pad Dimensions: 4 x 4 mils

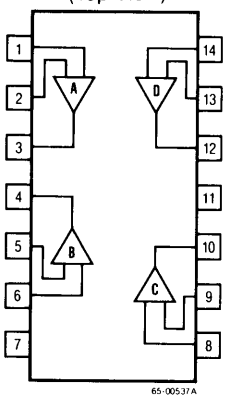
Schematic Diagram (1/4 Shown)



General Purpose Quad 741 Operational Amplifier

Connection Information

14-Lead
Dual In-Line Package
(Top View)



Pin	Function
1	-Input (A)
2	+Input (A)
3	Output (A)
4	Output (B)
5	+Input (B)
6	-Input (B)
7	$-V_S$
8	-Input (C)
9	+Input (C)
10	Output (C)
11	$+V_S$
12	Output (D)
13	+Input (D)
14	-Input (D)

Absolute Maximum Ratings

Supply Voltage
- RM4136 ..... ±22V
- RC4136, RV4136 ..... ±18V

Input Voltage[1] ..... ±15V
Differential Input Voltage 30V
Output Short Circuit Duration[2] ..... Indefinite
Storage Temperature
- Range ..... -65°C to +150°C

Operating Temperature Range
- RM4136 ..... -55°C to +125°C
- RC4136 ..... 0°C to +70°C
- RV4136 ..... -40°C to +85°C

Lead Soldering Temperature
- (60 Sec) ..... +300°C

Notes: 1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Short circuit may be to ground, typically 45mA.

Thermal Characteristics

	14-Lead Plastic DIP	14-Lead Ceramic DIP
Max. Junction Temp.	125°C	175°C
Max. P_D T_A < 50°C	468mW	1042mW
Therm. Res. θ_{JC}	—	60°C/W
Therm. Res. θ_{JA}	160°C/W	120°C/W
For T_A > 50°C Derate at	6.25mW per °C	8.33mW per °C

Ordering Information

Part Number	Package	Operating Temperature Range
RC4136DB	Plastic	0°C to +70°C
RC4136DC	Ceramic	0°C to +70°C
RV4136DB	Plastic	-40°C to +85°C
RV4136DC	Ceramic	-40°C to +85°C
RM4136DC	Ceramic	-55°C to +125°C
RM4136DC/883B*	Ceramic	-55°C to +125°C

*MIL-STD-883, Level B Processing

Electrical Characteristics (V_S = ±15V and T_A = +25°C)

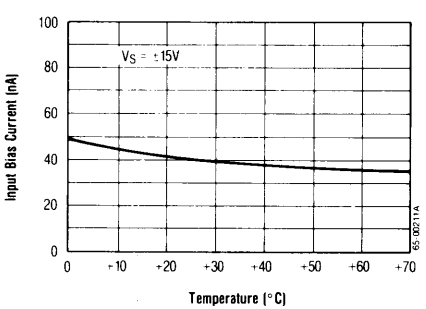
Parameters	Test Conditions	RM4136 Min	RM4136 Typ	RM4136 Max	RC/RV4136 Min	RC/RV4136 Typ	RC/RV4136 Max	Units
Input Offset Voltage	$R_S \leq 10k\Omega$		0.5	5.0		0.5	6.0	mV
Input Offset Current			5.0	200		5.0	200	nA
Input Bias Current			40	500		40	500	nA
Input Resistance		0.3	5.0		0.3	5.0		MΩ
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	50	300		20	300		V/mV
Output Voltage Swing	$R_L \geq 10k\Omega$	±12	±14		±12	±14		V
	$R_L \geq 2k\Omega$	±10	±13		±10	±13		
Input Voltage Range		±12	±14		±12	±14		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	100		70	100		dB
Power Supply Rejection Ratio	$R_S \leq 10k\Omega$	76	100		76	100		dB
Power Consumption	$R_L = \infty$, All Outputs		210	340		210	340	mW
Transient Response Rise Time	V_{IN} = 20mV, R_L = 2kΩ		0.13			0.13		μS
Overshoot	$C_L \leq 100pF$		5.0			5.0		%
Unity Gain Bandwidth			3.0			3.0		MHz
Slew Rate	$R_L \geq 2k\Omega$		1.5			1.0		V/μS
Channel Separation	f = 1.0kHz, R_S = 1kΩ		90			90		dB
The following specification apply for $-55°C \leq T_A \leq +125°C$ for RM4136; $0°C \leq T_A \leq +70°C$ for RC4136; $-40°C \leq T_A \leq +85°C$ for RV4136, V_S = ±15V								
Input Offset Voltage	$R_S \leq 10k\Omega$			6.0			7.5	mV
Input Offset Current RM/RC4136				500			300	nA
RV4136							500	
Input Bias Current RM/RC4136				1500			800	nA
RV4136							1500	
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	25			15			V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	±10			±10			V
Power Consumption			240	400		240	400	mW

Electrical Characteristics Comparison (V_S = ±15V and T_A = +25°C)

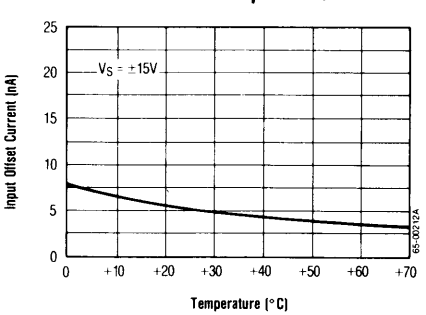
Parameter	RC4136 (Typ)	RC741 (Typ)	LM324 (Typ)	Units
Input Offset Voltage	0.5	2.0	2.0	mV
Input Offset Current	5.0	10	5.0	nA
Input Bias Current	40	80	55	nA
Input Resistance	5.0	2.0		MΩ
Large Signal Voltage Gain (R_L = 2kΩ)	300	200	100	V/mV
Output Voltage Swing (R_L = 2kΩ)	±13V	±13V	$\lvert+V_S - 1.2V\rvert$ to $-V_S$	V
Input Voltage Range	±14V	±13V	$\lvert+V_S - 1.5V\rvert$ to $-V_S$	V
Common Mode Rejection Ratio	100	90	85	dB
Power Supply Rejection Ratio	100	90	100	dB
Transient Response Rise Time	0.13	0.3		μS
Overshoot	5.0	5.0		%
Unity Gain Bandwidth	3.0	0.8	0.8	MHz
Slew Rate	1.0	0.5	0.5	V/μS
Input Noise Voltage Density (f = 1kHz)	10	22.5		nV/$\sqrt{Hz}$
Short Circuit Current	±45	±25		mA

Typical Performance Characteristics

Input Bias Current as a Function of Ambient Temperature

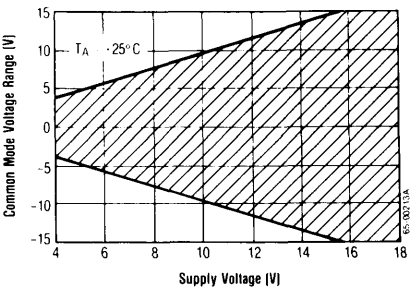


Input Offset Current as a Function of Ambient Temperature

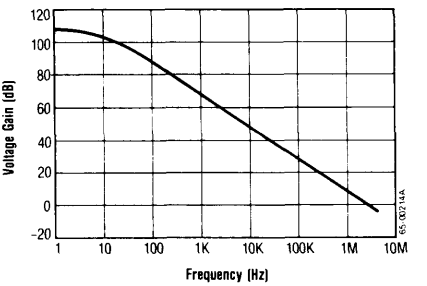


Typical Performance Characteristics (Continued)

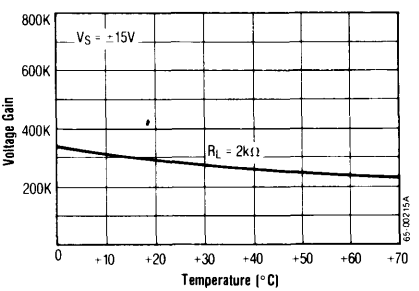
Common Mode Range as a Function of Supply Voltage



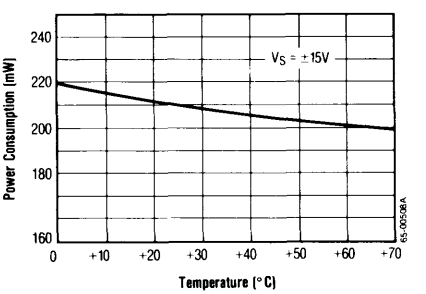
Open Loop Voltage Gain as a Function of Frequency



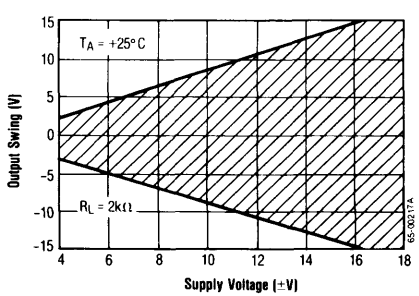
Open Loop Gain as a Function of Temperature



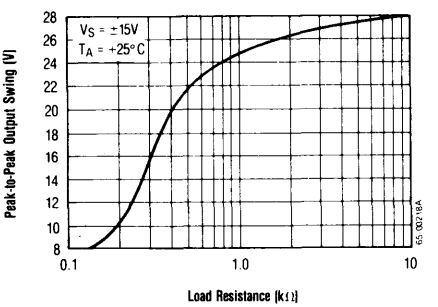
Power Consumption as a Function of Ambient Temperature



Typical Output Voltage as a Function of Supply Voltage

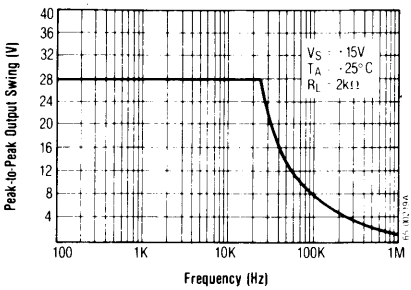


Output Voltage Swing as a Function of Load Resistance

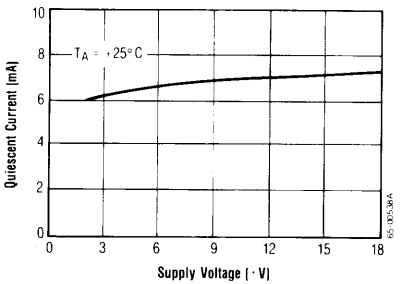


Typical Performance Characteristics (Continued)

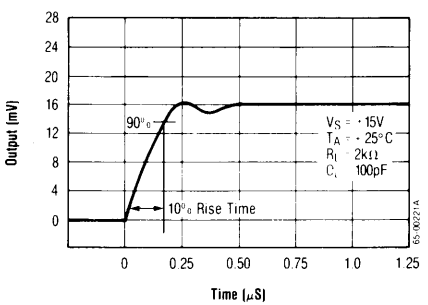
Output Voltage Swing as a Function of Frequency



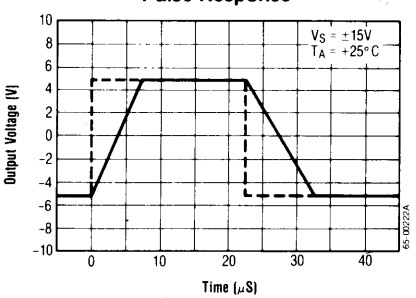
Quiescent Current as a Function of Supply Voltage



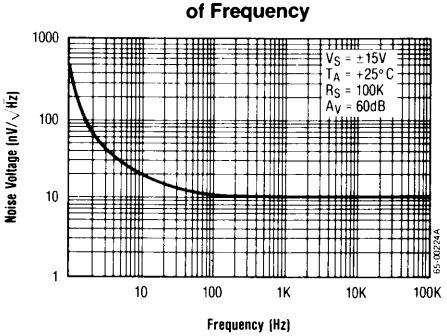
Transient Response



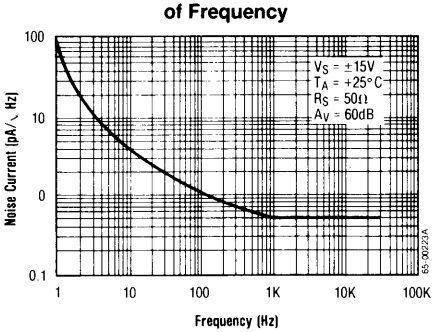
Voltage Follower Large Signal Pulse Response



Input Noise Voltage as a Function of Frequency

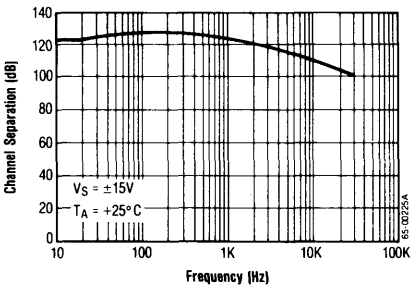


Input Noise Current as a Function of Frequency

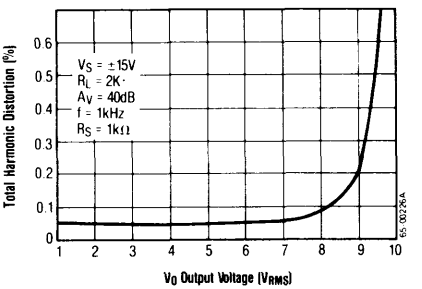


Typical Performance Characteristics (Continued)

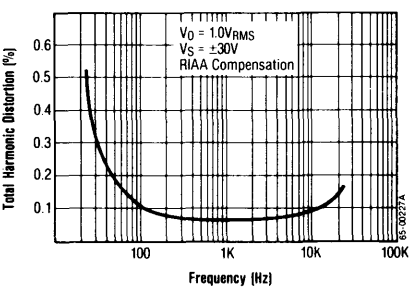
Channel Separation



Total Harmonic Distortion vs. Output Voltage



Distortion vs. Frequency

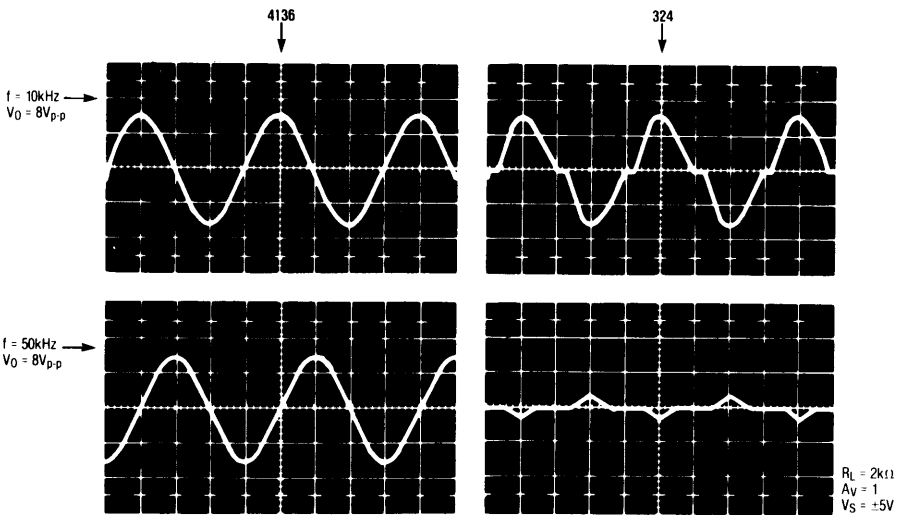


4136 Versus 741

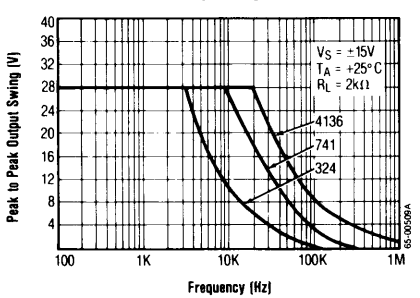
Although the 324 is an excellent device for single-supply applications where ground sensing is important, it is a poor substitute for four 741s in split supply circuits.

The simplified input circuit of the 4136 exhibits much lower noise than that of the 324 and exhibits no crossover distortion as compared with the 324 (see illustration). The 324 shows serious crossover distortion and pulse delay in attempting to handle a large signal input pulse.

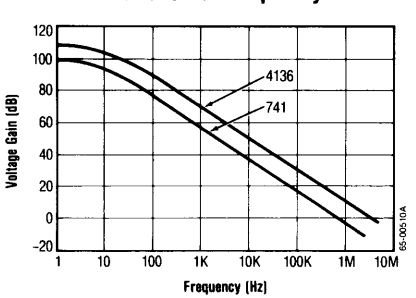
Comparative Crossover Distortion



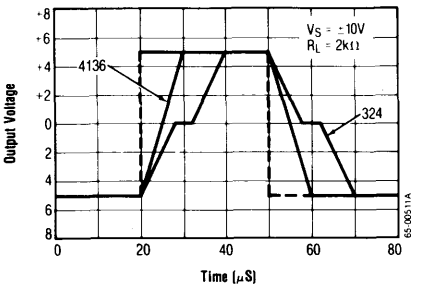
Output Voltage Swing as a Function of Frequency



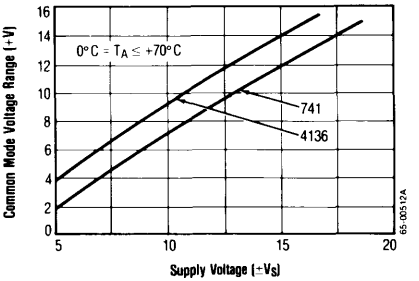
Open Loop Voltage Gain as a Function of Frequency



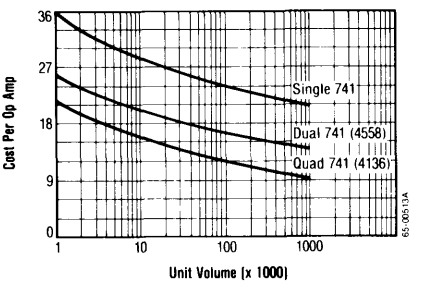
Voltage Follower Large Signal Pulse Response



Input Common Mode Voltage Range as a Function of Supply Voltage

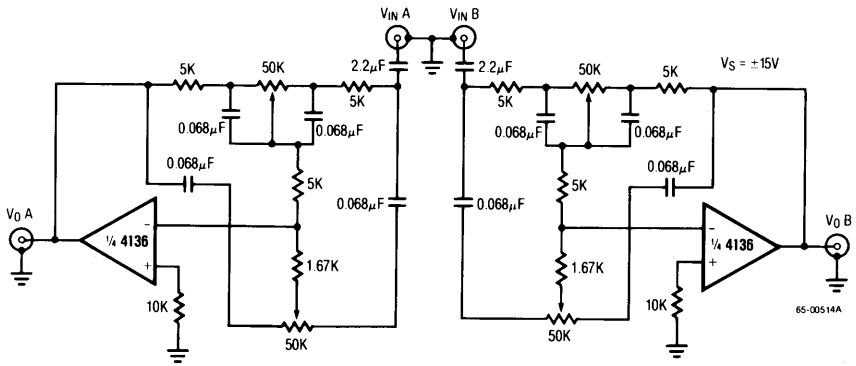


Unit Cost Comparisons

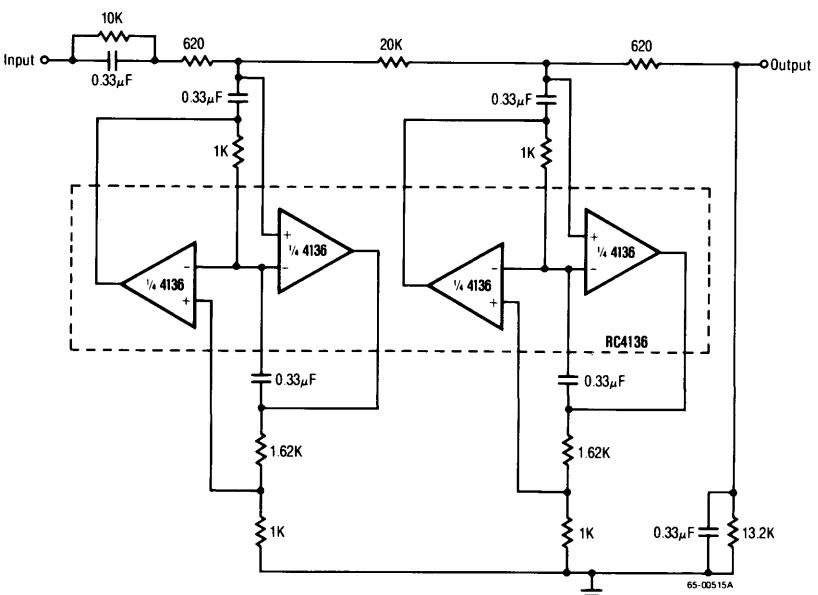


4136 Typical Applications

Stereo Tone Control

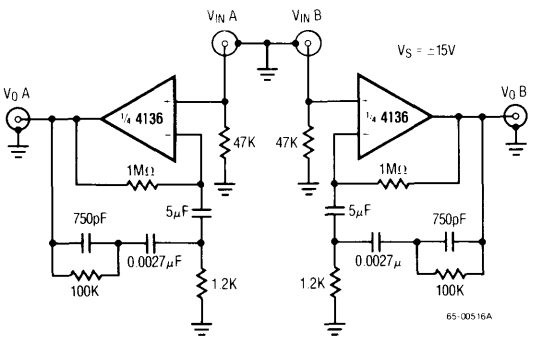


400Hz Lowpass Butterworth Active Filter

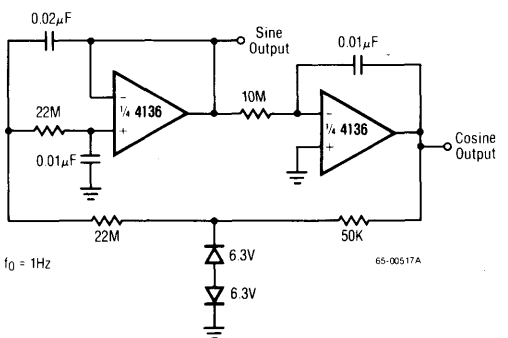


4136 Typical Applications (Continued)

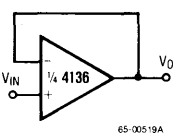
RIAA Preamplifier



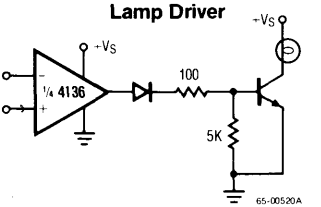
Low Frequency Sine Wave Generator With Quadrature Output



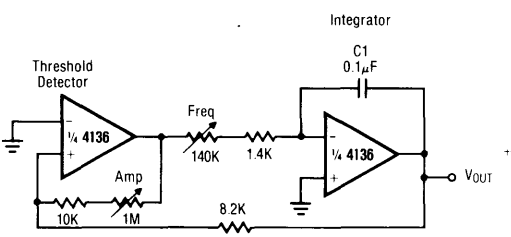
Voltage Follower



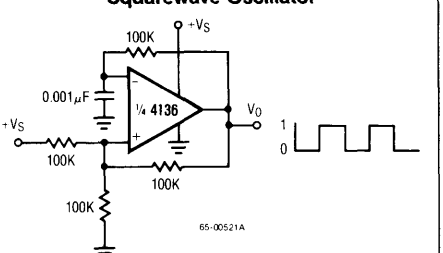
Lamp Driver



Triangular-Wave Generator

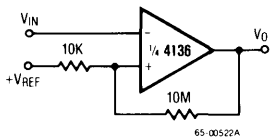


Squarewave Oscillator

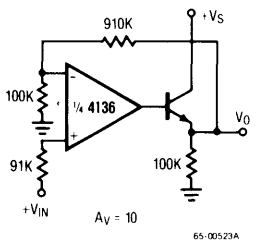


4136 Typical Applications (Continued)

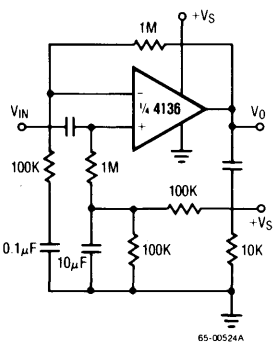
Comparator With Hysteresis



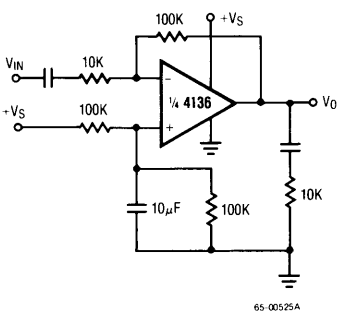
Power Amplifier



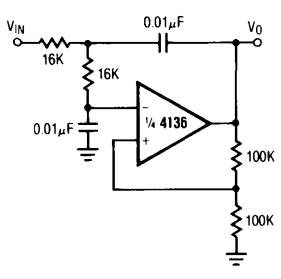
AC Coupled Non-Inverting Amplifier



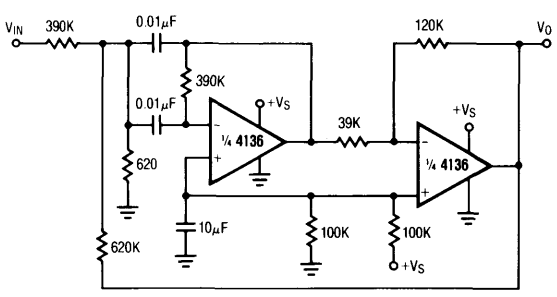
AC Coupled Inverting Amplifier



DC Coupled 1kHz Lowpass Active Filter

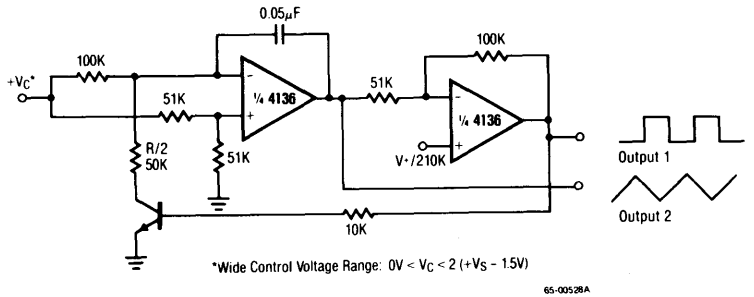


1kHz Bandpass Active Filter



4136 Typical Applications (Continued)

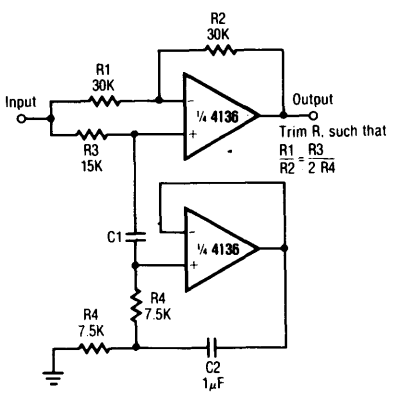
Voltage Controlled Oscillator (VCO)



*Wide Control Voltage Range: $0V < V_C < 2(+V_S - 1.5V)$

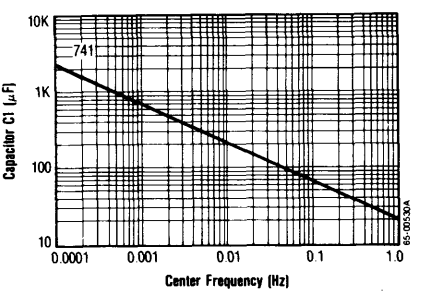
65-00528A

Notch Filter Using the 4136 as a Gyrator

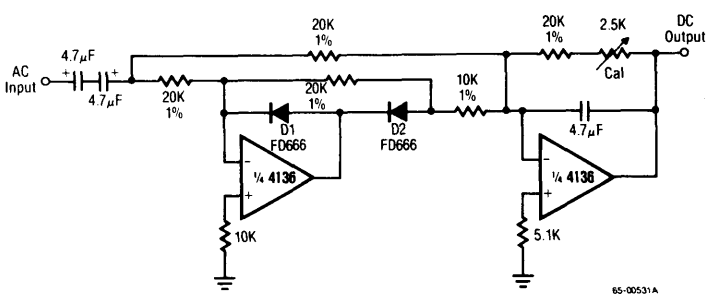


65-00529A

Notch Frequency as a Function of C1



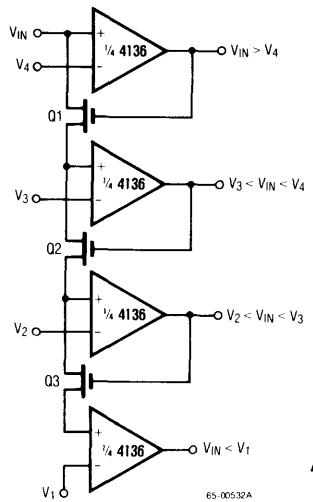
Full-Wave Rectifier and Averaging Filter



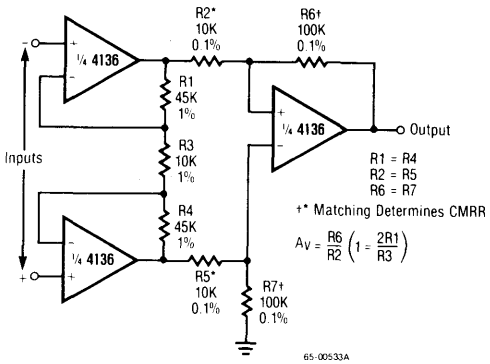
65-00531A

4136 Typical Applications (Continued)

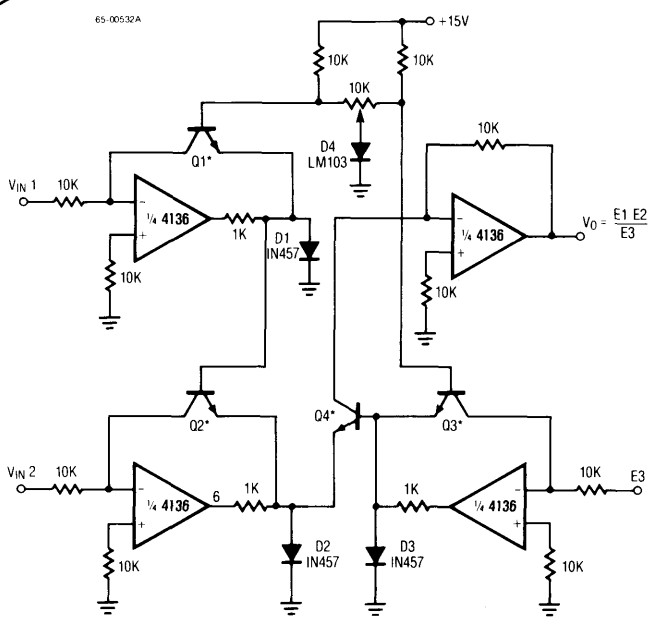
Multiple Aperture Window Discriminator



Differential Input Instrumentation Amplifier With High Common Mode Rejection



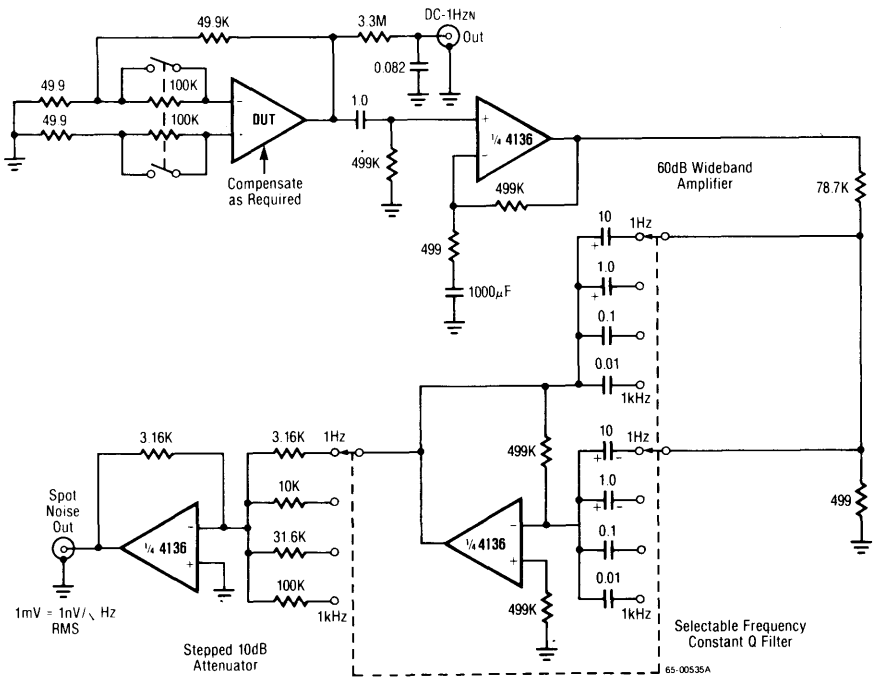
Analog Multiplier/Divider



*Matched Transistors

4136 Typical Applications (Continued)

Spot Noise Measurement Test Circuit



Raytheon

High Performance Quad Operational Amplifier

RC4156

Features

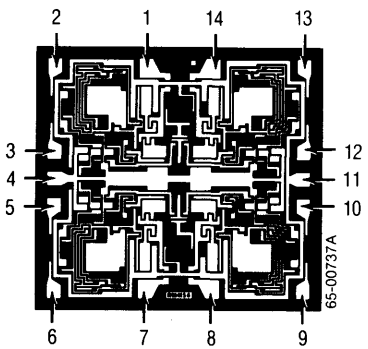
- Unity gain bandwidth — 3.5MHz typical; 2.8MHz guaranteed
- High slew rate — 1.6V/μS typical; 1.3V/μS guaranteed
- Low noise voltage — 1.4μV typical; 2.0μV_{RMS} guaranteed
- Indefinite short circuit protection
- No crossover distortion
- Low input offset and bias parameters
- Internal compensation

Description

The 4156 is a monolithic integrated circuit, consisting of four independent high performance operational amplifiers constructed with an advanced epitaxial process.

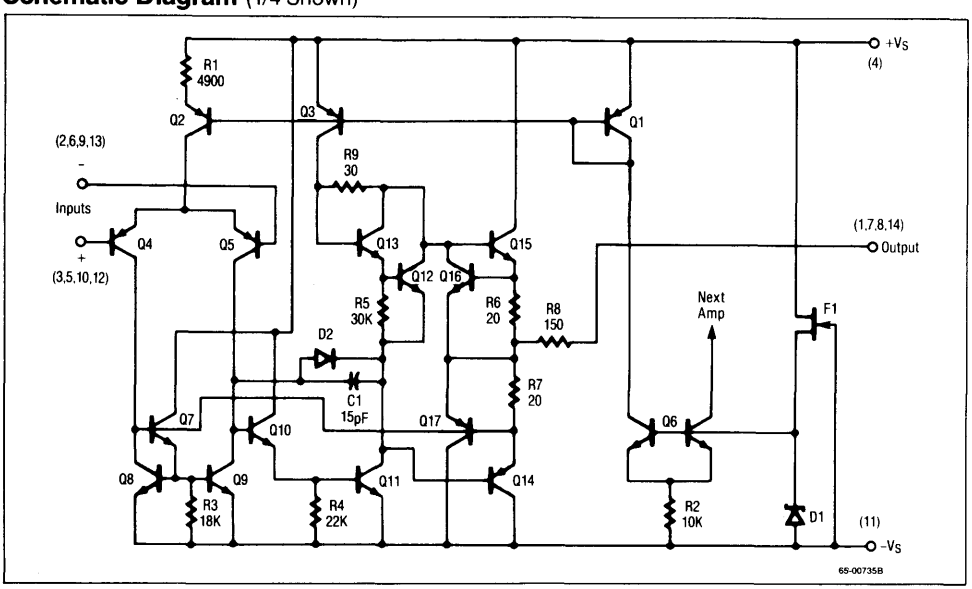
These amplifiers feature guaranteed AC performance which far exceeds that of the 741 type amplifiers. Also featured are excellent input characteristics and guaranteed low noise, making this device the optimum choice for audio, active filter and instrumentation applications.

Mask Pattern



Die Size: 80 x 84 mils
Min. Pad Dimension: 4 x 4 mils

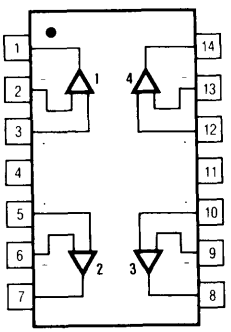
Schematic Diagram (1/4 Shown)



RC4156 High Performance Quad Operational Amplifier

Connection Information

14-Lead
Dual In-Line Packages
(Top View)



65-0078-A

Pin	Function
1	Output A
2	$-V_{IN}$ A
3	$+V_{IN}$ A
4	$+V_S$
5	$+V_{IN}$ B
6	$-V_{IN}$ B
7	Output B
8	Output C
9	$-V_{IN}$ C
10	$+V_{IN}$ C
11	$-V_S$
12	$+V_{IN}$ D
13	$-V_{IN}$ D
14	Output D

Thermal Characteristics

	14-Lead Plastic DIP	14-Lead Ceramic DIP
Max. Junction Temp.	125°C	175°C
Max. P_D $T_A < 50°C$	468mW	1042mW
Therm. Res. θ_{JC}	—	50°C/W
Therm. Res. θ_{JA}	160°C/W	120°C/W
For $T_A > 50°C$ Derate at	6.25mW per °C	8.33mW per °C

Absolute Maximum Ratings

Supply Voltage ..... ±20V
Differential Input Voltage 15V
Input Voltage[1] ..... ±15V
Output Short Circuit Duration[2] ..... Indefinite
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
RM4156 ..... -55°C to +125°C
RV4156 ..... -40°C to +85°C
RC4156 ..... 0°C to +70°C
Lead Soldering Temperature
(60 Sec) ..... +300°C

Notes: 1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Short circuit to ground on one amplifier only.

Ordering Information

Part Number	Package	Operating Temperature Range
RC4156DB	Plastic	0°C to +70°C
RC4156DC	Ceramic	0°C to +70°C
RM4156DC	Ceramic	-55°C to +125°C
RM4156DC/883B*	Ceramic	-55°C to +125°C

*MIL-STD-883, Level B Processing

Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise specified)

Parameters	Test Conditions	RM4156			RC/RV4156			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 10k\Omega$		0.5	3.0		1.0	5.0	mV
Input Offset Current			15	30		30	50	nA
Input Bias Current			60	200		60	300	nA
Input Resistance			0.5			0.5		MΩ
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} ±10V	50	100		25	100		V/mV
Output Voltage Swing	$R_L \geq 10k\Omega$	±12	±14		±12	±14		V
	$R_L \geq 2k\Omega$	±10	±13		±10	±13		V
Input Voltage Range		±12	±14		±12	±14		V
Output Resistance			230			230		Ω
Short Circuit Current			25			25		mA
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	80			80			dB
Power Supply Rejection Ratio	$R_S \leq 10k\Omega$	80			80			dB
Supply Current (All Amplifiers)	$R_L = \infty$		4.5	5.0		5.0	7.0	mA
Transient Response								
Rise Time			50			75		nS
Overshoot			25			25		%
Slew Rate		1.3	1.6		1.3	1.6		V/μS
Unity Gain Bandwidth		2.8	3.5		2.8	3.5		MHz
Phase Margin	R_L = 2kΩ, C_L = 50pF		50			50		Deg.
Power Bandwidth	$V_O = 20V_{p-p}$	20	25		20	25		kHz
Input Noise Voltage	f = 20Hz to 20kHz		1.4	2.0		1.4	2.0	μV_{RMS}
Input Noise Current	f = 20Hz to 20kHz		15			15		pA_{RMS}
Channel Separation			108			108		dB

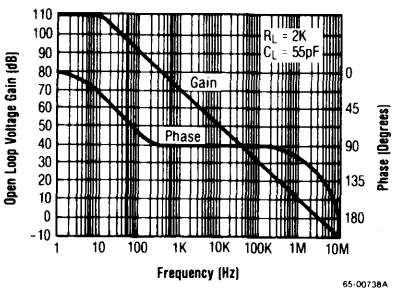
Electrical Characteristics (Continued)

($-55°C \leq T_A \leq +125°C$ for RM4156, $-40°C \leq T_A \leq +85°C$ for RV4156, $0°C \leq T_A \leq +70°C$ for RC4156, $V_S = \pm 15V$)

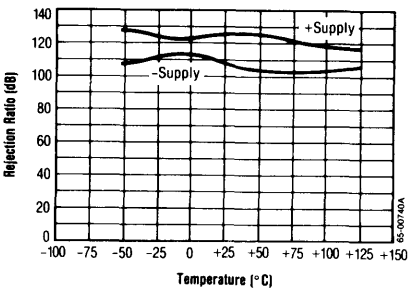
Parameters	Test Conditions	RM4156			RC/RV4156			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 10k\Omega$			5.0			6.5	mV
Input Offset Current				75			100	nA
Input Bias Current				320			400	nA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_{OUT} \pm 10V$	25			15			V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	±10			±10			V
Supply Current			10			10		mA
Average Input Offset Voltage Drift			5.0			5.0		μV/°C

Typical Performance Characteristics

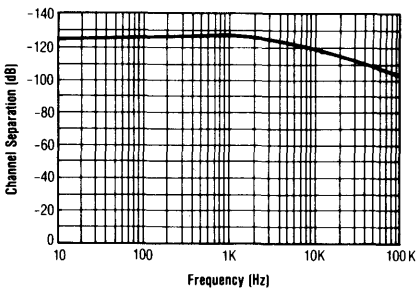
Open Loop Frequency Response

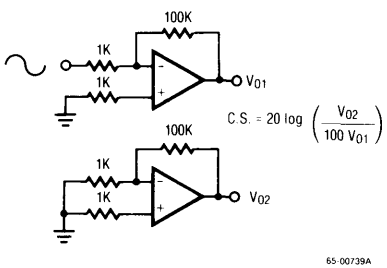


Power Supply Rejection Ratio vs. Temperature

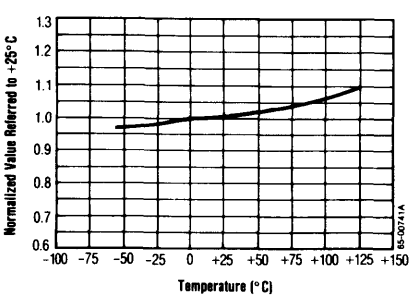


Channel Separation vs. Frequency

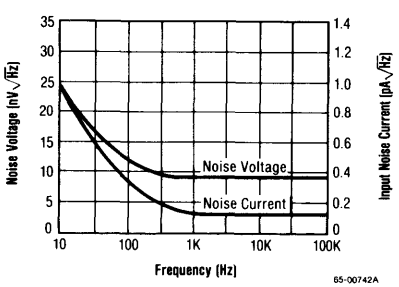




Transient Response vs. Temperature

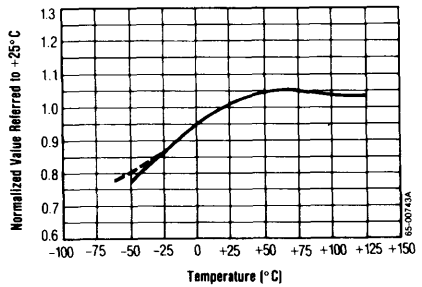


Input Noise vs. Frequency

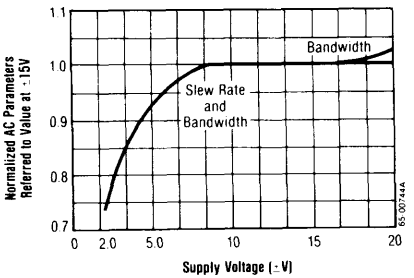


Typical Performance Characteristics (Continued)

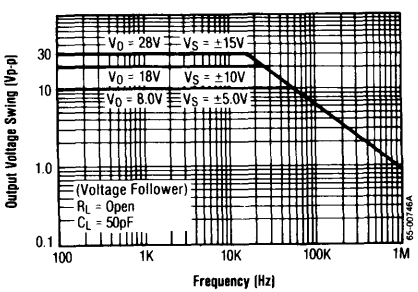
Normalized AC Parameters vs. Temperature



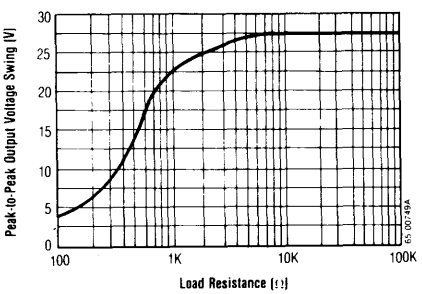
Slew Rate vs. Supply Voltage



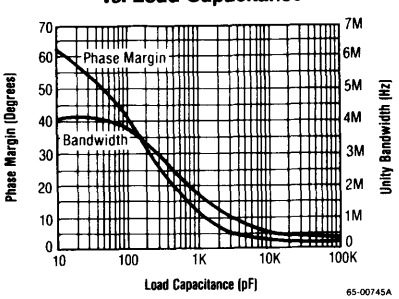
Output Voltage Swing vs. Frequency



Output Voltage Swing vs. Load Resistance

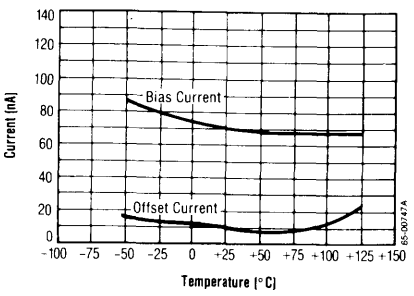


Small Signal Bandwidth and Phase Margin vs. Load Capacitance

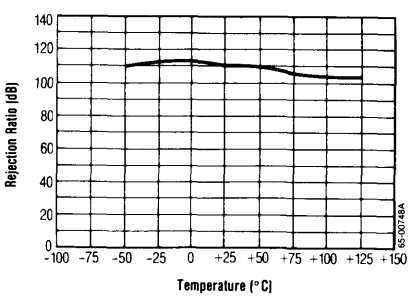


Typical Performance Characteristics (Continued)

Input Current vs. Temperature



Common Mode Rejection Ratio vs. Temperature



Applications

The 4156 quad operational amplifier can be used in almost any 741 application and will provide superior performance. The higher unity gain bandwidth and slew rate make it ideal for applications requiring good frequency response, such as active filter circuits, oscillators and audio amplifiers.

The following applications have been selected to illustrate the advantages of using the Raytheon 4156 quad operational amplifier.

Triangle and Square Wave Generator

The circuit of Figure 1 uses a positive feedback loop closed around a combined comparator and integrator. When power is applied the output of the comparator will switch to one of two states, to the maximum positive or maximum negative voltage. This applies a peak input signal to the integrator, and the integrator output will ramp either down or up, opposite of the input signal. When the integrator output (which is connected to the comparator input) reaches a threshold set by R1 and R2, the comparator will switch to the opposite polarity. This cycle will repeat endlessly, the integrator charging positive then negative, and the comparator switching in a square wave fashion.

Amplitude of V_2 is adjusted by varying R1. For best operation, it is recommended that R1 and

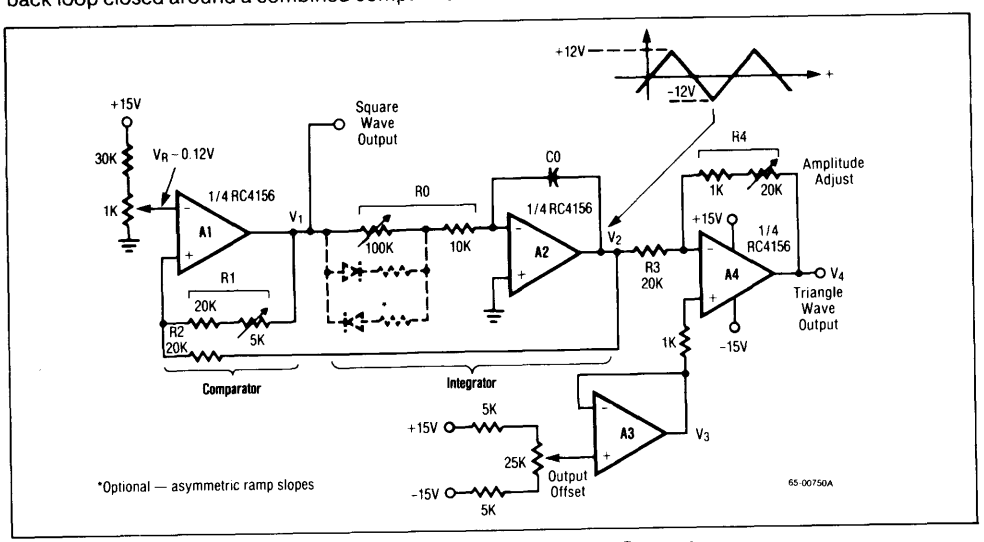


Figure 1. Triangle and Square Wave Generator

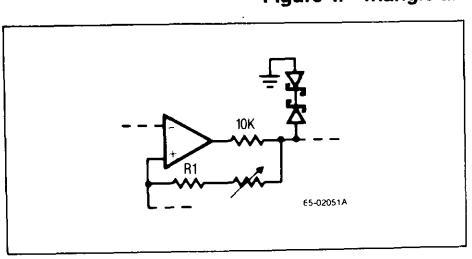


Figure 2. Triangle Generator — Symmetrical Output Option

V_R be set to obtain a triangle wave at V_2 with ±12V amplitude. This will then allow A3 and A4 to be used for independent adjustment of output-offset and amplitude over a wide range.

The triangle wave frequency is set by C0, R0, and the maximum output voltages of the comparator. A more symmetrical waveform can be generated by adding a back-to-back zener diode pair as shown in Figure 2.

An asymmetric triangle wave is needed in some applications. Adding diodes as shown by the dashed lines is a way to vary the positive and negative slopes independently.

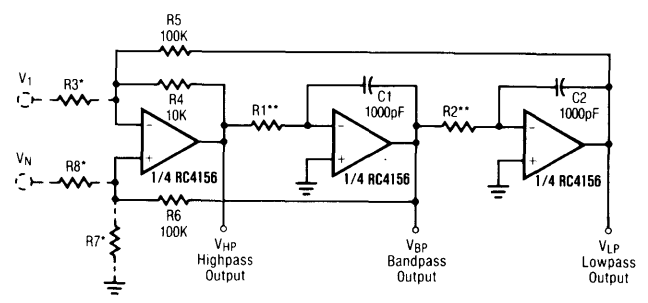
Frequency range can be very wide and the circuit will function very well up to about 10kHz. Transition time for the square wave at V_1 is less than 21μS when using the 4156.

Active Filters

The introduction of low-cost quad op amps has had a strong impact on active filter design. The complex multiple-feedback, single op amp filter circuits have been rendered obsolete for most applications. State-variable active-filter circuits using three to four op amps per section offer many advantages over the single op amp circuits. They are relatively insensitive to the passive-component tolerances and variations. The Q, gain, and natural frequency can be independently adjusted. Hybrid construction is very practical because resistor and capacitor values are relatively low and the filter parameters are determined by resistance ratios rather than by single resistors. A generalized circuit diagram of the 2-pole state-variable active filter is shown in Figure 3. The particular input connections and component-values can be calculated for specific applications. An important feature of the state-variable filter is that it can be inverting or non-inverting and can simultaneously provide three outputs: lowpass, bandpass, and highpass. A notch filter can be realized by adding one summing op amp.

The Raytheon 4156 was designed and characterized for use in active filter circuits. Frequency response is fully specified with minimum values for unity-gain bandwidth, slew-rate, and full-power response. Maximum noise is specified. Output swing is excellent with no distortion or clipping. The Raytheon 4156 provides full, undistorted response up to 20kHz and is ideal for use in high-performance audio and telecommunication equipment.

In the state-variable filter circuit, one amplifier performs a summing function and the other two act as integrators. The choice of passive component values is arbitrary, but must be consistent with the amplifier operating range and input signal characteristics. The values shown for C1, C2, R4, R5 and R6 are arbitrary. Pre-selecting their values will simplify the filter tuning procedures, but other values can be used if necessary.



*Input connections are chosen for inverting or non-inverting response. Values of R3, R7, R8 determine gain and Q.
**Values of R1 and R2 determine natural frequency.

Figure 3. Generalized State-Variable Configuration for Active Filter

The generalized transfer function for the state-variable active filter is:

$$T(s) = \frac{a_2 s^2 + a_1 s + a_0}{s^2 + b_1 s + b_0}$$

Filter response is conventionally described in terms of a natural frequency ω_0 in radians/sec, and Q, the quality of the complex pole pair. The filter parameters ω_0 and Q relate to the coefficients in T(s) as:

$$\omega_0 = \sqrt{b_0} \text{ and } Q = \frac{\omega_0}{b_0}$$

The input configuration determines the polarity (inverting or non-inverting), and the output selection determines the type of filter response (lowpass, bandpass, or highpass).

Notch and all-pass configurations can be implemented by adding another summing amplifier.

Bandpass filters are of particular importance in audio and telecommunication equipment. A design approach to bandpass filters will be shown as an example of the state-variable configuration.

Design Example — Bandpass Filter

In this example, the input signal is applied through R3 to the inverting input of the summing amplifier and the output is taken from the first integrator (V_{BP}). The summing amplifier will maintain equal voltage at the inverting and non-inverting inputs (see equation below).

$$\frac{\frac{R3R5}{R3+R5}}{R4+\frac{R3R5}{R3+R5}} V_{HP}(s) + \frac{\frac{R3R4}{R3+R4}}{R5+\frac{R3R4}{R3+R4}} V_{LP}(s) + \frac{\frac{R4R5}{R4+R5}}{R3+\frac{R4R5}{R4+R5}} V_{IN}(s) = \frac{R7}{R6+R7} V_{BP}(s)$$

These equations can be combined to obtain the transfer function:

$$V_{BP}(s) = -\frac{1}{R1C1S} V_{HP}(s) \text{ and } V_{LP}(s) = -\frac{1}{R2C2S} V_{BP}(s)$$

$$\frac{V_{BP}(s)}{V_{IN}(s)} = \frac{\frac{R4}{R3}\frac{1}{R1C1}s}{s^2 + \frac{R7}{R6+R7}\left(1+\frac{R4}{R5}+\frac{R4}{R3}\right)\left(\frac{1}{R1C1}\right)s + \frac{R4}{R5}\frac{1}{R1C1R2C2}}$$

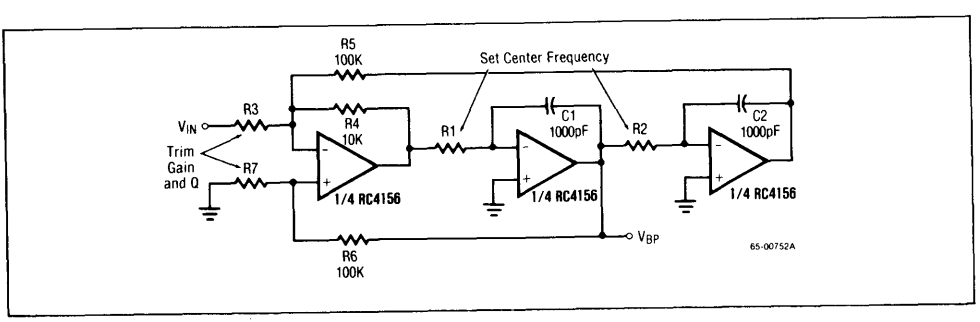


Figure 4. Bandpass Active Filter

Defining 1/R1C1 as ω_1, 1/R2C2 as ω_2, and substituting in the assigned values for R4, R5, and R6, then the transfer function simplifies to:

$$\frac{V_{BP}(s)}{V_{IN}(s)} = \frac{\frac{10^4}{R3}\omega_1 s}{s^2 + \left[\frac{1.1 + \frac{10^4}{R3}}{1 + \frac{10^5}{R7}}\right]\omega_1 s + \frac{0.1}{\omega_1\omega_2}}$$

This is now in a convenient form to look at the center-frequency ω_0 and filter Q.

$$\omega_0 = \sqrt{0.1\omega_1\omega_2} = 10^{-9}\sqrt{0.1R1R2}$$

$$\text{and } Q = \left[\frac{1 + \frac{10^5}{R7}}{1.1 + \frac{10^4}{R3}}\right]\omega_0$$

The frequency response for various values of Q are shown in Figure 5.

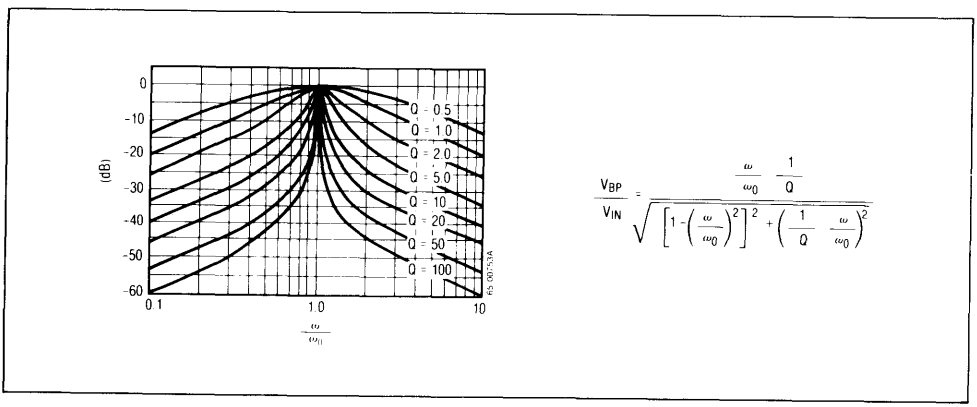


Figure 5. Bandpass Transfer Characteristics Normalized for Unity Gain and Frequency

These equations suggest a tuning sequence where ω is first trimmed via R1 or R2, then Q is trimmed by varying R7 and/or R3. An important advantage of the state-variable bandpass filter is that Q can be varied without affecting center frequency ω_0.

This analysis has assumed ideal op amps operating within their linear range, which is a valid design approach for a reasonable range of ω_0 and Q. At extremes of ω_0 and at high values of Q, the op amp parameters become significant. A rigorous analysis is very complex, but some factors are particularly important in designing active filters.

1. The passive component values should be chosen such that all op amps are operating within their linear region for the anticipated range of input signals. Slew rate, output current rating, and common-mode input range must be considered. For the integrators, the current through the feedback capacitor (I = C dV/dt) should be included in the output current computations.

2. From the equation for Q, it would seem that infinite Q could be obtained by making R7 zero. But as R7 is made small, the Q becomes limited by the op amp gain at the frequency of interest. The effective closed-loop gain is being increased directly as R7 is made smaller, and the ratio of open-loop gain to closed-loop gain is becoming less. The gain and phase error of the filter at high Q is very dependent on the op amp open-loop gain at ω_0.

3. The attenuation at extremes of frequency is limited by the op amp gain and unity-gain bandwidth. For integrators, the finite open-loop op amp gain limits the accuracy at the low-end. The open-loop roll-off of gain limits the filter attenuation at high frequency.

RC4156 High Performance Quad Operational Amplifier

The Raytheon 4156 quad operational amplifier has much better frequency response than a conventional 741 circuit and is ideal for active filter use. Natural frequencies of up to 10kHz are readily achieved and up to 20kHz is practical for some configurations. Q can range up to 50 with very good accuracy and up to 500 with reasonable response. The extra gain of the 4156 at high frequencies gives the Raytheon quad op amp an extra margin of performance in active-filter circuits.

Raytheon

High Output Current Dual Operational Amplifier

RC4556

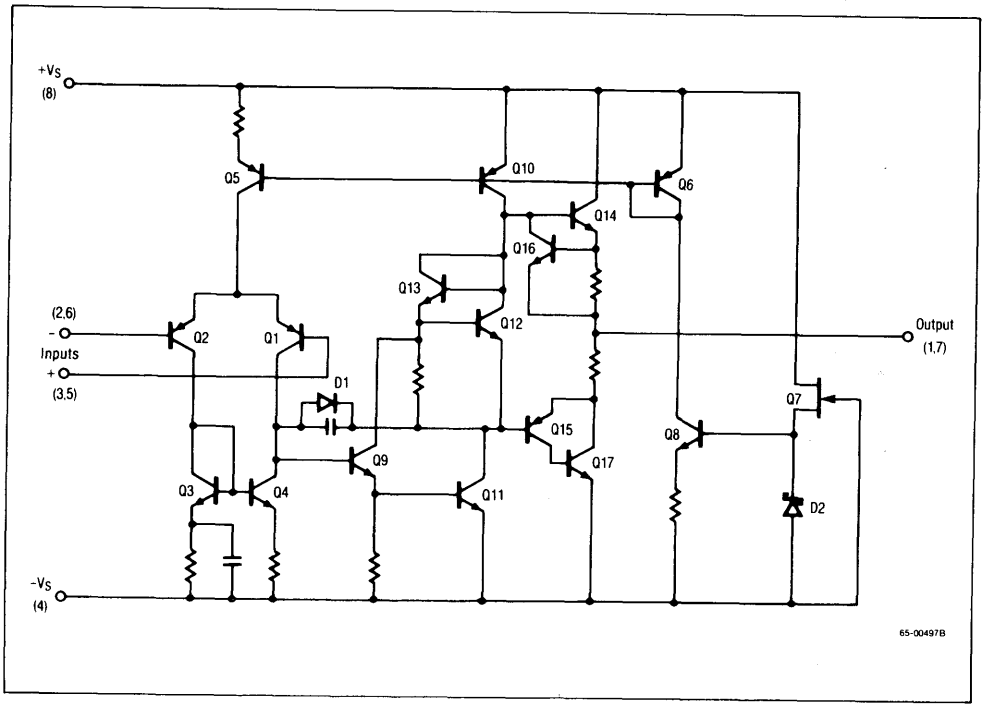
Features

- Unity gain bandwidth — 8.0MHz
- Drives ±10.5V min into 150Ω (±10mA)
- Slew rate — 3.0V/μS
- Current drain per amplifier — 4.5mA
- Input offset voltage — 0.5mV
- Input offset current — 5.0nA
- Input bias current — 180nA
- 10nV/√Hz noise at 1kHz
- Unity gain frequency compensated

Description

The 4556 integrated circuit is a high-gain, high output current dual operational amplifier capable of driving ±70mA into 150Ω loads (±10.5V output voltage). The 4556 combines many of the features of the popular 4558 as well as having the capability of driving 150Ω loads. In addition, the wide bandwidth, low noise, high slew rate and low distortion of the 4556 make it ideal for many audio, telecommunications and instrumentation applications.

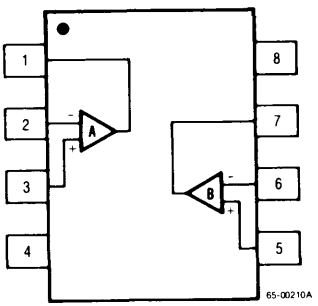
Schematic Diagram (1/2 Shown)



RC4556 High Output Current Dual Operational Amplifier

Connection Information

8-Lead
Dual In-Line Package
(Top View)



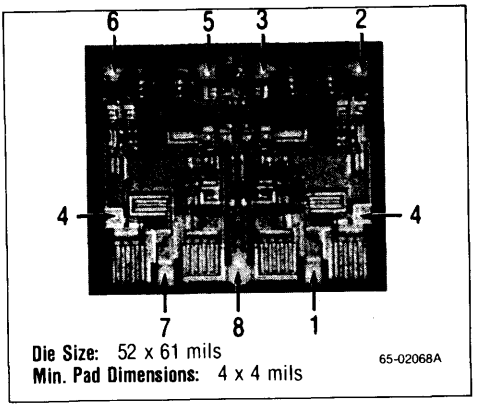
Pin	Function
1	A Output
2	A -Input
3	A +Input
4	$-V_S$
5	B +Input
6	B -Input
7	B Output
8	$+V_S$

Absolute Maximum Ratings

Supply Voltage ..... ±18V
Input Voltage[1] ..... ±15V
Differential Input Voltage 30V
Output Short Circuit Duration[2] ..... Indefinite
Operating Temperature
Range ..... -20°C to +75°C
Lead Soldering Temperature (10 Sec)
RC4556NB ..... +300°C
RC4556M ..... +260°C

Notes: 1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Short circuit may be to ground on one amp only. Rating applies to +75°C ambient temperature.

Mask Pattern



Die Size: 52 x 61 mils
Min. Pad Dimensions: 4 x 4 mils

Thermal Characteristics

	8-Lead Micro-Pak Plastic DIP	8-Lead Plastic DIP
Max. Junction Temp.	125°C	125°C
Max. P_D $T_A < 50°C$	300mW	468mW
Therm. Res. θ_{JC}	—	—
Therm. Res. θ_{JA}	240°C/W	160°C/W
For $T_A > 50°C$ Derate at	4.17mW per °C	6.25mW per °C

Ordering Information

Part Number	Package	Operating Temperature Range
RC4556M	Micro-Plastic	-20°C to +75°C
RC4556NB	Plastic	-20°C to +75°C

Matching Characteristics

($V_S = \pm15V$, $T_A = +25°C$)

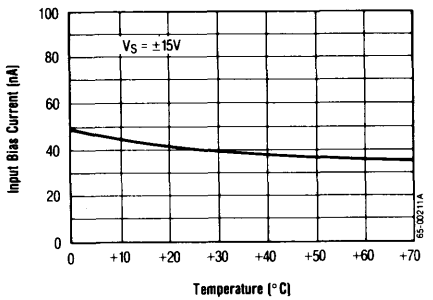
Parameter	Conditions	Typ	Units
Voltage Gain	$R_L \geq 20k\Omega$	±1.0	dB
Input Bias Current		±15	nA
Input Offset Current		±7.5	nA
Input Offset Voltage	$R_S \geq 10k\Omega$	±0.2	mV

Electrical Characteristics ($V_S = \pm15V$ and $T_A = +25°C$ unless otherwise specified)

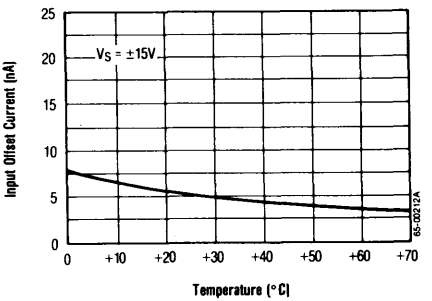
Parameters	Test Conditions	Min	Typ	Max	Units
Input Offset Voltage	$R_S \leq 10k\Omega$		2.0	6.0	mV
Input Offset Current			5.0	200	nA
Input Bias Current			40	500	nA
Input Resistance		0.3	1.0		MΩ
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_{OUT} = \pm10V$	20	100		V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	±12	±13.5		V
	$R_L = 150\Omega$	±10.5	±11		
Input Voltage Range		±12	±14		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	90		dB
Power Supply Rejection Ratio	$R_S \leq 10k\Omega$	76	90		dB
Power Consumption	$R_L = \infty$		270	360	mW
Transient Response Rise Time	$V_{IN} = 20mV$, $R_L = 2k\Omega$		0.03		μS
Overshoot	$C_L \leq 100pF$		40		%
Slew Rate	$R_L \geq 2k\Omega$		3.0		V/μS
Channel Separation	f = 10kHz, R_S = 1kΩ, Gain = 100		90		dB
Unity Gain Bandwidth		5.0	8.0		MHz
The following specifications apply for $-20°C \leq T_A \leq +75°C$					
Input Offset Voltage	$R_S \leq 10k\Omega$			7.5	mV
Input Offset Current				300	nA
Input Bias Current				800	nA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_{OUT} = \pm10V$	15			V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	±10			V
Power Consumption	$T_A = +75°C$		260	340	mW
	$T_A = -20°C$		290	380	

Typical Performance Characteristics

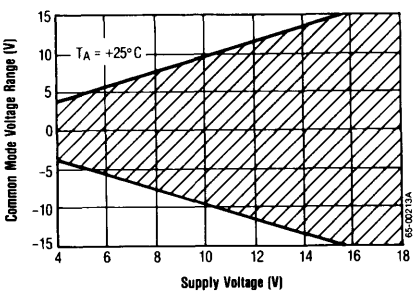
Input Bias Current as a Function of Ambient Temperature



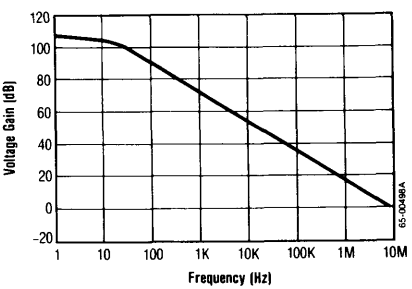
Input Offset Current as a Function of Ambient Temperature



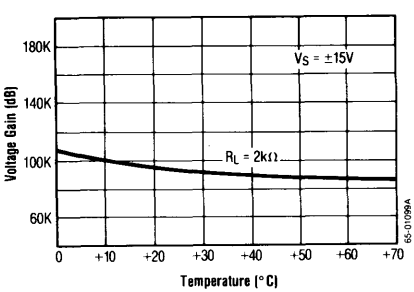
Common Mode Range as a Function of Supply Voltage



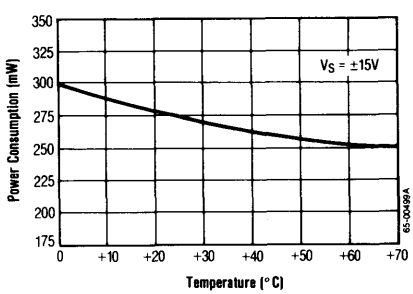
Open Loop Gain as a Function of Temperature



Open Loop Voltage Gain as a Function of Frequency

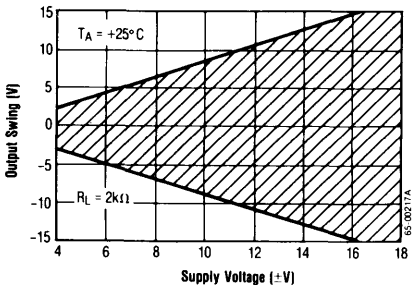


Power Consumption as a Function of Ambient Temperature

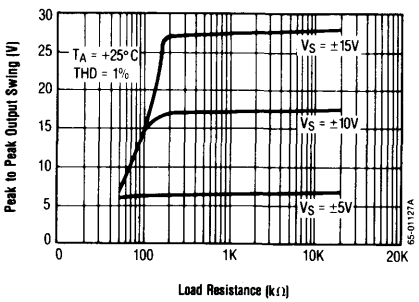


Typical Performance Characteristics (Continued)

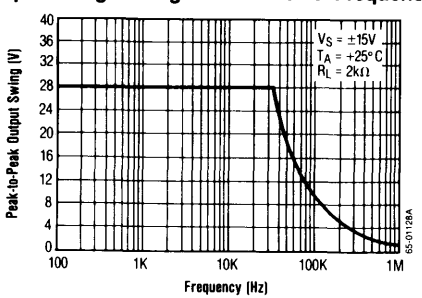
Typical Output Voltage as a Function of Supply Voltage



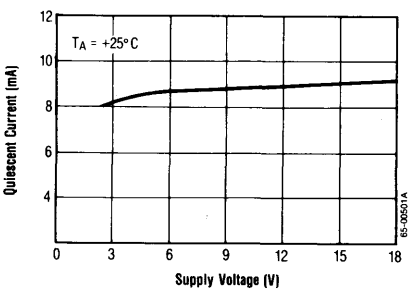
Output Voltage Swing as a Function of Load Resistance



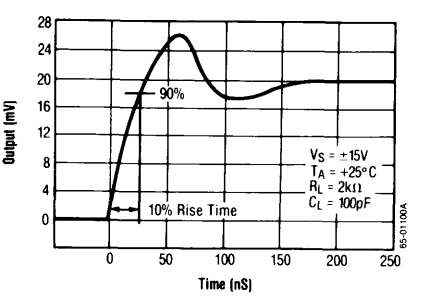
Output Voltage Swing as a Function of Frequency



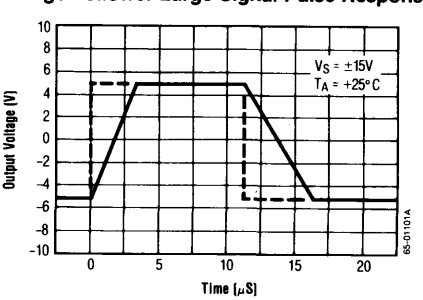
Quiescent Current as a Function of Supply Voltage



Transient Response

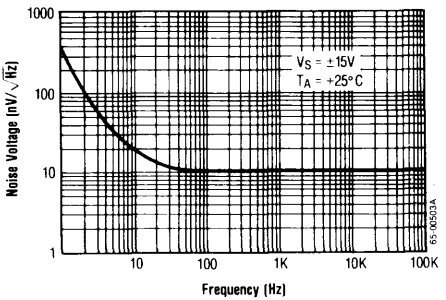


Voltage Follower Large Signal Pulse Response

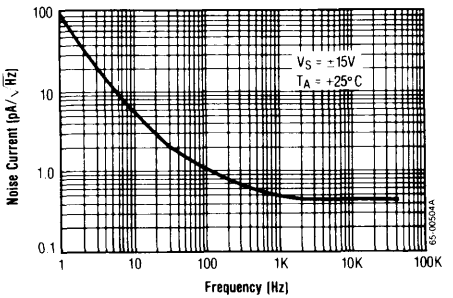


Typical Performance Characteristics (Continued)

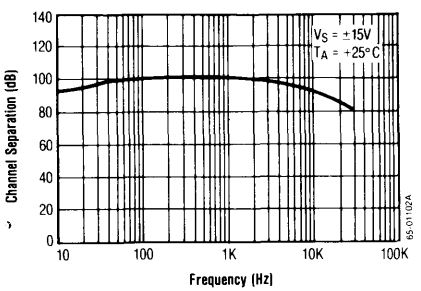
Input Noise Voltage as a Function of Frequency



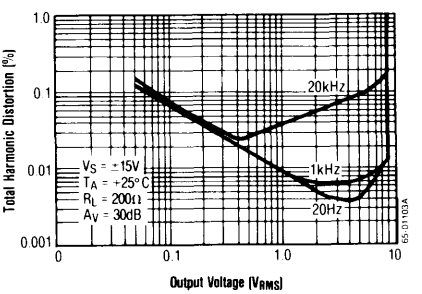
Input Noise Current as a Function of Frequency



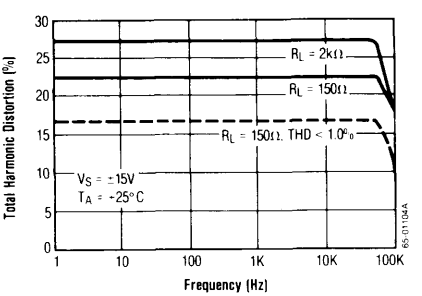
Channel Separation



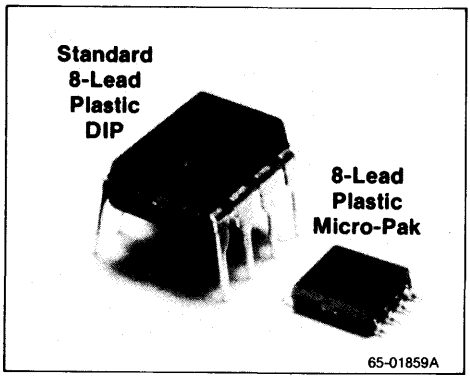
Total Harmonic Distortion vs. Output Voltage



Distortion vs. Frequency



Comparison of Standard vs. Micro-Package



Raytheon

High-Gain Dual Operational Amplifier

RC4558

Features

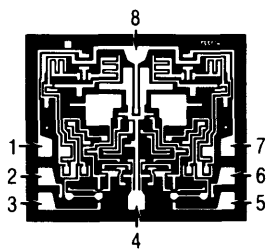
- 2.5MHz unity gain bandwidth guaranteed
- Supply voltage ±22V for RM4558 and ±15V for RC4558
- Short-circuit protection
- No frequency compensation required
- No latch-up
- Large common-mode and differential voltage ranges
- Low power consumption
- Parameter tracking over temperature range
- Gain and phase match between amplifiers

Description

The 4558 integrated circuit is a dual high-gain operational amplifier internally compensated and constructed on a single silicon chip using an advanced epitaxial process.

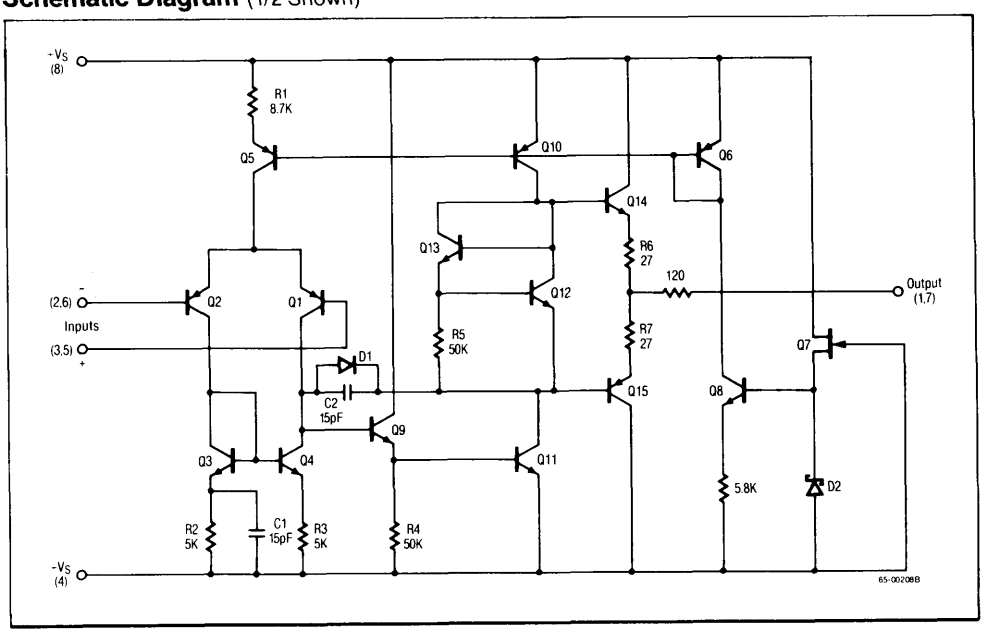
Combining the features of the 741 with the close parameter matching and tracking of a dual device on a monolithic chip results in unique performance characteristics. Excellent channel separation allows the use of the dual device in single 741 operational amplifier applications providing density. It is especially well suited for applications in differential-in, differential-out as well as in potentiometric amplifiers and where gain and phase matched channels are mandatory.

Mask Pattern



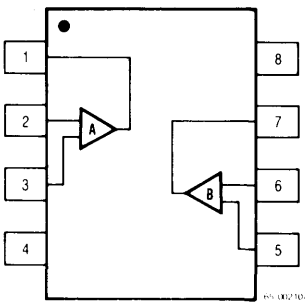
Die Size: 52 x 61 mils
Min. Pad Dimensions: 4 x 4 mils

Schematic Diagram (1/2 Shown)

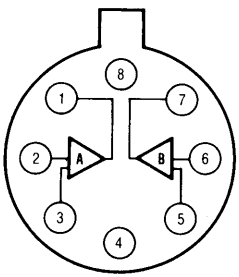


Connection Information

8-Lead
Dual In-Line Package
(Top View)



8-Lead
Metal Can TO-99
(Top View)



Pin	Function
1	A Output
2	A -Input
3	A +Input
4	$-V_S$
5	B +Input
6	B -Input
7	B Output
8	$+V_S$

Absolute Maximum Ratings

Supply Voltage
- RM4558 ..... ±22V
- RC4558 ..... ±18V

Differential Input Voltage 30V
Input Voltage[1] ..... ±15V
Operating Temperature Range
- RM4558 ..... -55°C to +125°C
- RV4558 ..... -40°C to +85°C
- RC4558 ..... 0°C to +70°C

Output Short Circuit Duration[2] ..... Indefinite

Notes: 1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Short circuit may be to ground on one amp only. Rating applies to +75°C ambient temperature.

Ordering Information

Part Number	Package	Operating Temperature Range
RC4558DE	Ceramic	0°C to +70°C
RC4558M	Micro Plastic	0°C to +70°C
RC4558NB	Plastic	0°C to +70°C
RC4558T	TO-99	0°C to +70°C
RV4558DE	Ceramic	-40°C to +85°C
RV4558NB	Plastic	-40°C to +85°C
RM4558DE	Ceramic	-55°C to +125°C
RM4558DE/883B*	Ceramic	-55°C to +125°C
RM4558T	TO-99	-55°C to +125°C
RM4558T/883B*	TO-99	-55°C to +125°C

*MIL-STD-883, Level B Processing

Thermal Characteristics

	8-Lead Micro-Pak	8-Lead Plastic DIP	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can
Max. Junction Temp.	125°C	125°C	175°C	175°C
Max. P_D $T_A \leq 50°C$	300mW	468mW	833mW	658mW
Therm. Res. θ_{JC}	—	—	45°C/W	50°C/W
Therm. Res. θ_{JA}	240°C/W	160°C/W	150°C/W	190°C/W
For $T_A > 50°C$ Derate at	4.1mW per °C	6.25mW per °C	8.33mW per °C	5.26mW per °C

Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise specified)

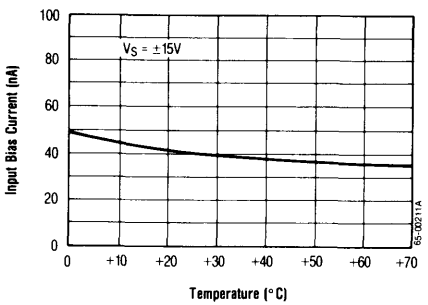
Parameters	Test Conditions	RM4558			RV/RC4558			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 10k\Omega$		1.0	5.0		2.0	6.0	mV
Input Offset Current			5.0	200		5.0	200	nA
Input Bias Current			40	500		40	500	nA
Input Resistance		0.3	1.0		0.3	1.0		MΩ
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	50	300		20	300		V/mV
Output Voltage Swing	$R_L \geq 10k\Omega$	±12	±14		±12	±14		V
	$R_L \geq 2k\Omega$	±10	±13		±10	±13		V
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	100		70	100		dB
Power Supply Rejection Ratio	$R_S \leq 10k\Omega$	76	100		76	100		dB
Power Consumption	$R_L = \infty$		100	170		100	170	mW
Transient Response Rise Time	V_{IN} = 20mV R_L = 2kΩ		0.3			0.3		μS
Overshoot	$C_L \leq 100pF$		35			35		%
Slew Rate	$R_L \geq 2k\Omega$		0.8			0.8		V/μS
Channel Separation	f = 10kHz, R_S = 1kΩ		90			90		dB
Unity Gain Bandwidth (Gain = 1)		2.5	3.0		2.0	3.0		MHz
The following specifications apply for $-55°C \leq T_A \leq +125°C$ for RM4558; $0°C \leq T_A \leq +70°C$ for RC4558; $-40°C \leq T_A \leq +85°C$ for RV4558								
Input Offset Voltage	$R_S \leq 10k\Omega$			6.0			7.5	mV
Input Offset Current RC4558 RV4558				 500 500			 300 500	 nA nA
Input Bias Current RC4558 RV4558				 1500 1500			 800 1500	 nA nA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	25			15			V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	±10			±10			V
Power Consumption	$R_L = \infty$		120	200		120	200	mW

Matching Characteristics (V_S = ±15V and T_A = +25°C unless otherwise specified)

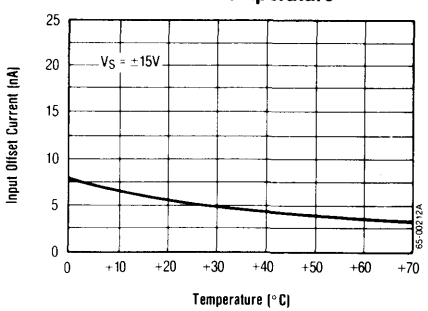
Parameters	Test Conditions	RM4558 Typ	RC4558 Typ	Units
Voltage Gain	$R_L \geq 2k\Omega$	±1.0	±1.0	dB
Input Bias Current	$R_L \geq 2k\Omega$	±15	±15	nA
Input Offset Current	$R_L \geq 2k\Omega$	±7.5	±7.5	nA

Typical Performance Characteristics

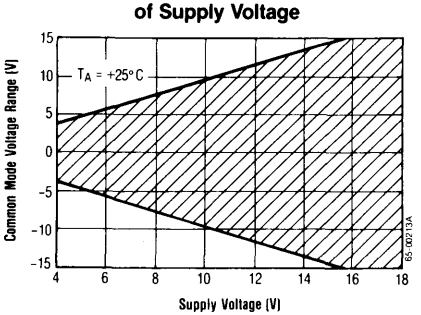
Input Bias Current as a Function of Ambient Temperature



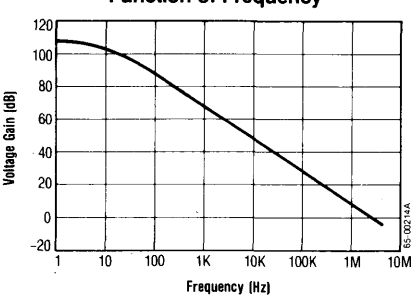
Input Offset Current as a Function of Ambient Temperature



Common Mode Range as a Function of Supply Voltage

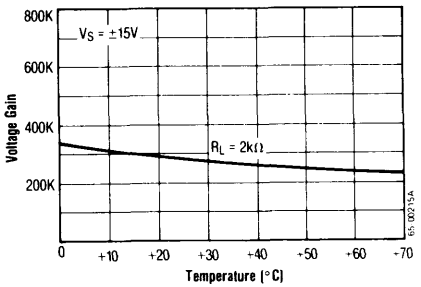


Open Loop Voltage Gain as a Function of Frequency

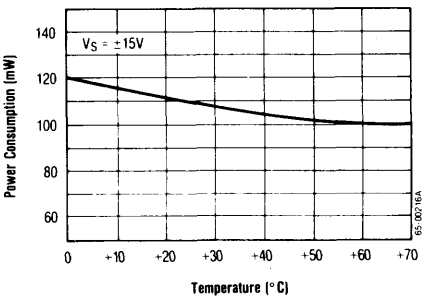


Typical Performance Characteristics (Continued)

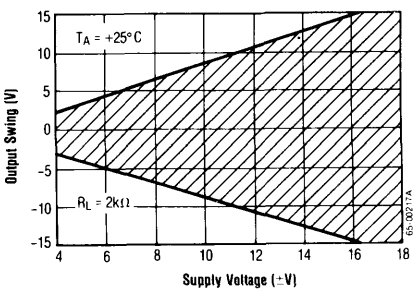
Open Loop Gain as a Function of Temperature



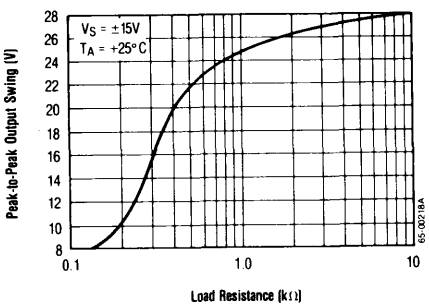
Power Consumption as a Function of Ambient Temperature



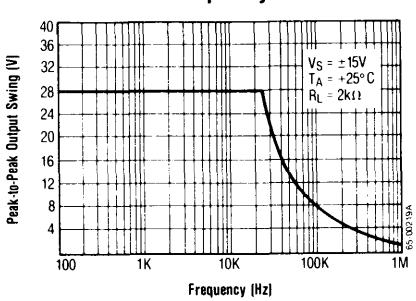
Typical Output Voltage as a Function of Supply Voltage



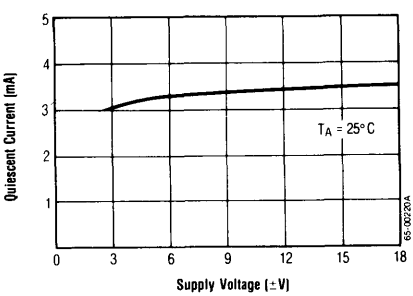
Output Voltage Swing as a Function of Load Resistance



Output Voltage Swing as a Function of Frequency

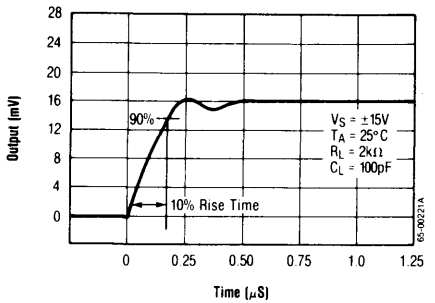


Quiescent Current as a Function of Supply Voltage

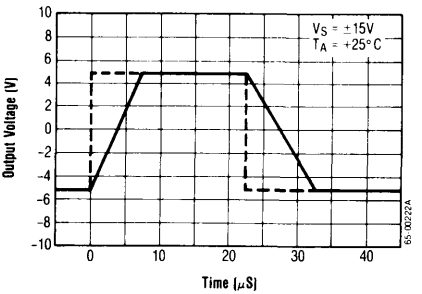


Typical Performance Characteristics (Continued)

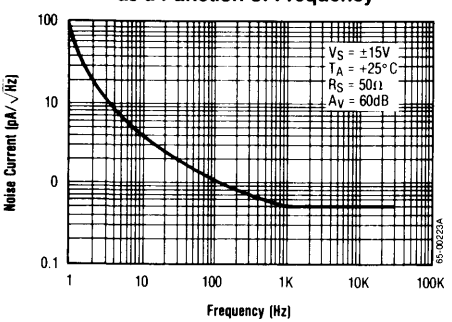
Transient Response



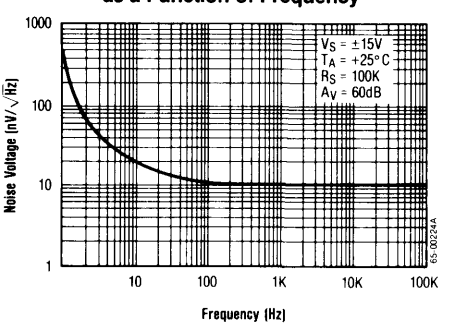
Voltage Follower Large Signal Pulse Response



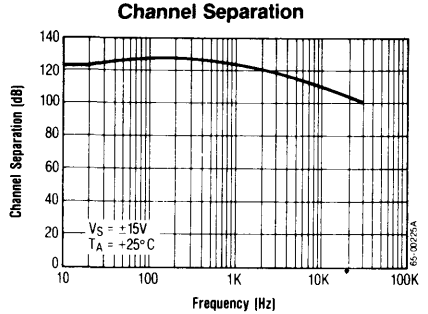
Input Noise Current as a Function of Frequency



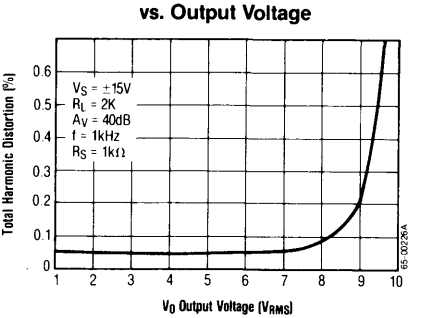
Input Noise Voltage as a Function of Frequency



Channel Separation

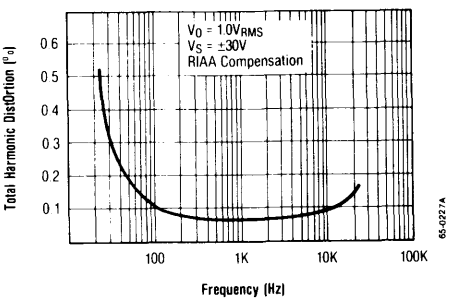


Total Harmonic Distortion vs. Output Voltage



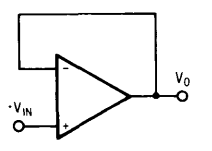
Typical Performance Characteristics (Continued)

Distortion vs. Frequency

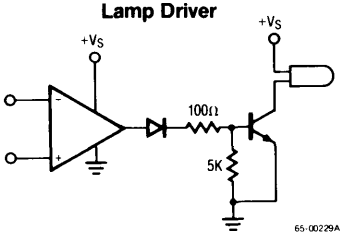


Typical Applications

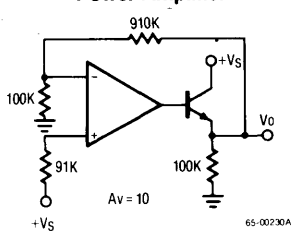
Voltage Follower



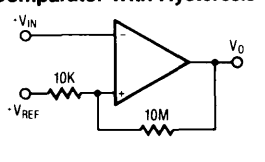
Lamp Driver



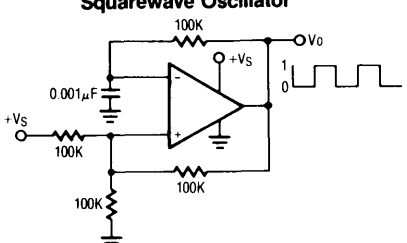
Power Amplifier



Comparator With Hysteresis

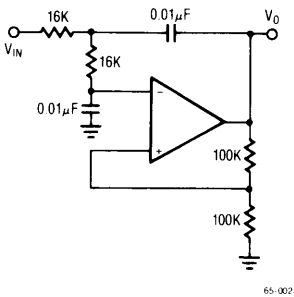


Squarewave Oscillator

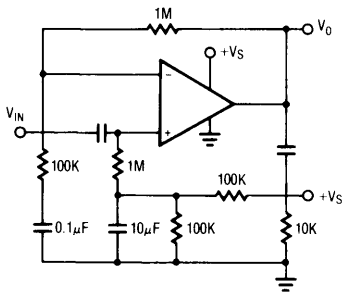


Typical Applications (Continued)

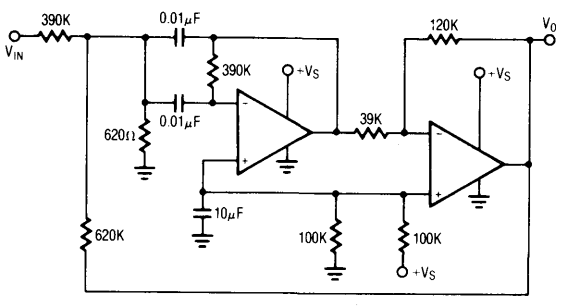
DC Coupled 1kHz Low-Pass Active Filter



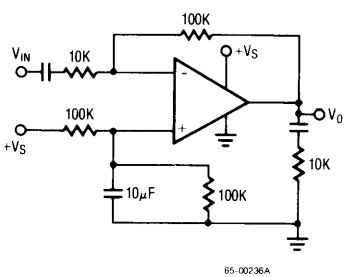
AC Coupled Non-Inverting Amplifier



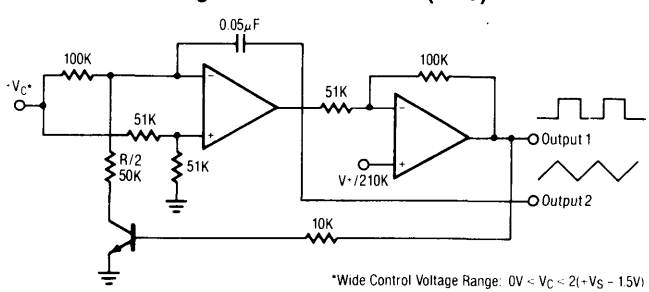
1kHz Bandpass Active Filter



AC Coupled Inverting Amplifier



Voltage Controlled Oscillator (VCO)



*Wide Control Voltage Range: $0V < V_C < 2(+V_S - 1.5V)$

65-00237A

Raytheon

High Performance Dual Operational Amplifier

RC4559

Features

- Unity gain bandwidth — 4.0MHz typical — 3.0MHz guaranteed
- Slew rate — 2.0V/μS typical — 1.5V/μS guaranteed
- Low noise voltage — 1.4μV_{RMS} typical — 2.0μV_{RMS} guaranteed
- Supply voltage — ±22V for RM4559 and ±18V for RC4559
- No frequency compensation required
- No latch up
- Large common mode and differential voltage ranges
- Low power consumption
- Parametric tracking over temperature range
- Gain and phase match between amplifiers

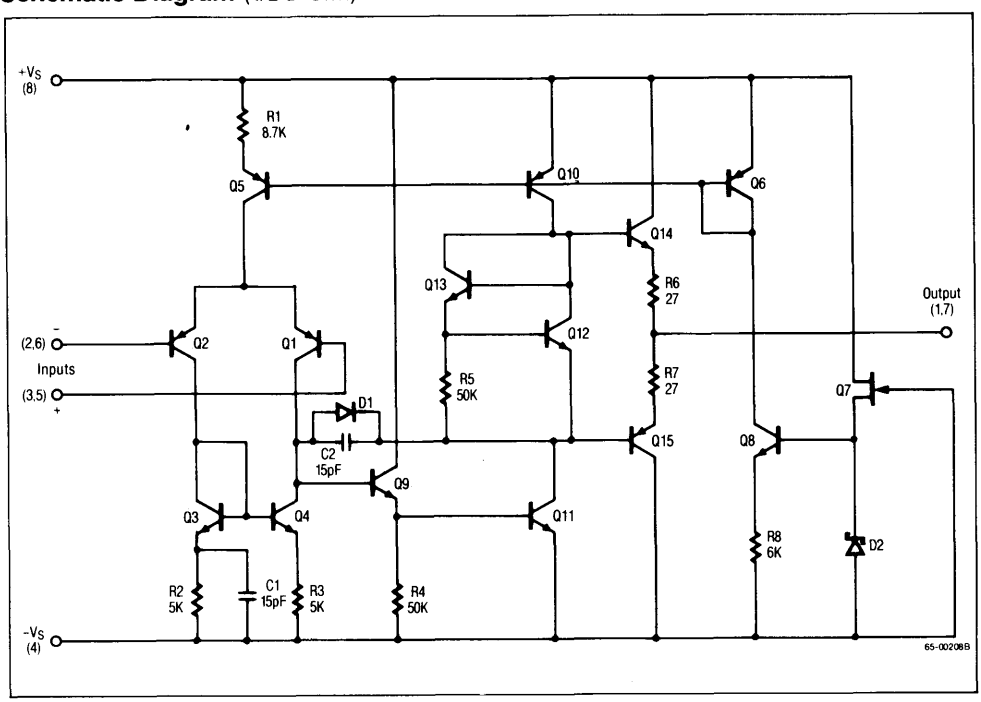
Description

The 4559 integrated circuit is a high performance dual operational amplifier internally compensated and constructed on a single silicon chip using an advanced epitaxial process.

These amplifiers feature guaranteed AC performance which far exceeds that of the 741-type amplifiers. The specially designed low-noise input transistors allow the 4559 to be used in low-noise signal processing applications such as audio preamplifiers and signal conditioners.

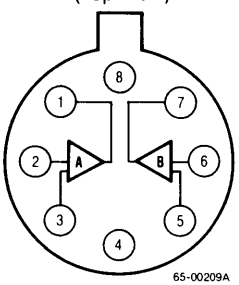
The 4559 also has more output drive capability that 741-type amplifiers and can be used to drive a 600Ω load.

Schematic Diagram (1/2 Shown)



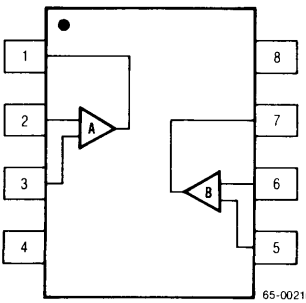
Connection Information

8-Lead
Metal Can TO-99
(Top View)



65-00209A

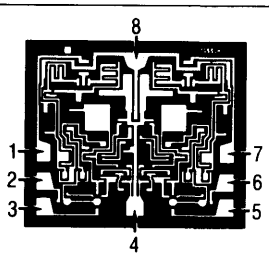
8-Lead
Dual In-Line Package
(Top View)



65-00210A

Pin	Function
1	A Output
2	A -Input
3	A +Input
4	$-V_S$
5	B +Input
6	B -Input
7	B Output
8	$+V_S$

Mask Pattern



65-01537A

Die Size: 52 x 61 mils
Min. Pad Dimensions: 4 x 4 mils

Absolute Maximum Ratings

Supply Voltage
- RM4559 ..... ±22V
- RC4559 ..... ±18V

Input Voltage[1] ..... ±15V
Differential Input Voltage 30V
Output Short Circuit Duration[2] ..... Indefinite
Operating Temperature Range
- RM4559 ..... -55°C to +125°C
- RV4559 ..... -40°C to +85°C
- RC4559 ..... 0°C to +70°C

Lead Soldering Temperature
- RV4559, RC4559 ..... +300°C
- RM4559 ..... +260°C

Notes: 1. For supply voltages less than -15V, the absolute maximum input voltage is equal to the supply voltage.
2. Short circuit may be to ground on one amp only. Rating applies to +75°C ambient temperature.

Thermal Characteristics

	8-Lead Micro-Pak	8-Lead Plastic DIP	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can
Max. Junction Temp.	125°C	125°C	175°C	175°C
Max. P_D $T_A < 50°C$	300mW	468mW	833mW	658mW
Therm. Res. θ_{JC}	—	—	45°C/W	50°C/W
Therm. Res. θ_{JA}	240°C/W	160°C/W	150°C/W	190°C/W
For $T_A > 50°C$ Derate at	4.1mW per °C	6.25mW per °C	8.33mW per °C	5.26mW per °C

Ordering Information

Part Number	Package	Operating Temperature Range
RC4559DE	Ceramic	0°C to +70°C
RC4559M	Micro-Plastic	0°C to +70°C
RC4559NB	Plastic	0°C to +70°C
RC4559T	TO-99	0°C to +70°C
RV4559DE	Ceramic	-40°C to +85°C
RV4559NB	Plastic	-40°C to +85°C
RM4559DE	Ceramic	-55°C to +125°C
RM4559DE/883B*	Ceramic	-55°C to +125°C
RM4559T	TO-99	-55°C to +125°C
RM4559T/883B*	TO-99	-55°C to +125°C

*MIL-STD-883, Level B Processing

Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise specified)

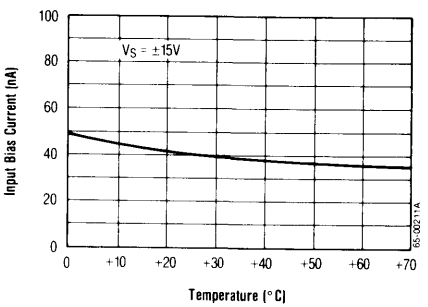
Parameters	Test Conditions	RM4559			RV/RC4559			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 10k\Omega$		1.0	5.0		2.0	6.0	mV
Input Offest Current			5.0	100		5.0	100	nA
Input Bias Current			40	250		40	250	nA
Input Resistance (Differential Mode)		0.3	1.0		0.3	1.0		MΩ
Large Signal Voltage Gain	$R_L \geq 2k\Omega$ V_{OUT} = ±10V	50	300		20	300		V/mV
Output Voltage Swing	$R_L \geq 10k\Omega$	±12	±14		±12	±14		V
	$R_L \geq 2k\Omega$	±10	±13		±10	±13		V
	$R_L \geq 600\Omega$	±9.5	±10		±9.5	±10		V
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	80	100		80	100		dB
Power Supply Rejection Ratio	$R_S \leq 10k\Omega$	82	100		82	100		dB
Supply Current	$R_L = \infty$		3.3	5.6		3.3	5.6	mA
Transient Response Rise Time	V_{IN} = 20mV R_L = 2kΩ		80			80		nS
Overshoot	$C_L \leq 100pF$		35			35		%
Slew Rate		1.5	2.0		1.5	2.0		V/μS
Unity Gain Bandwidth		3.0	4.0		3.0	4.0		MHz
Power Bandwidth	$V_O = 20V_{p-p}$	24	32		24	32		kHz
Input Noise Voltage	f = 20Hz to 20kHz		1.4	2.0		1.4	2.0	μV_{RMS}
Input Noise Current	f = 20Hz to 20kHz		25			25		pA_{RMS}
Channel Separation	Gain = 100, f = 10kHz R_S = 1kΩ		90			90		dB
The following specifications apply for $-55°C \leq T_A \leq +125°C$ for RM4559; $-40°C \leq T_A \leq +85°C$ for RV4559; and $0°C \leq T_A \leq +70°C$ for RC4559								
Input Offset Voltage	$R_S \leq 10k\Omega$			6.0			7.5	mV
Input Offset Current				300			200	nA
Input Bias Current				500			500	nA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$ V_{OUT} = ±10V	25			15			V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	±10			±10			V
Supply Current	$R_L = \infty$		4.0	6.6		4.0	6.6	mA

Matching Characteristics (V_S = ±15V, T_A = +25°C unless otherwise specified)

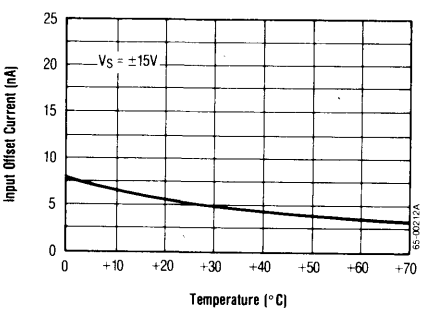
Parameter	Conditions	RM4559 Typ	RC4559 Typ	Units
Voltage Gain	$R_L \geq 2k\Omega$	±1.0	±1.0	dB
Input Bias Current		±15	±15	nA
Input Offset Current		±7.5	±7.5	nA

Typical Performance Characteristics

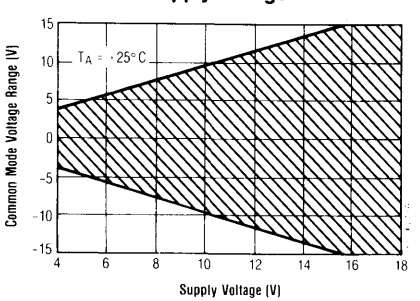
Input Bias Current as a Function of Ambient Temperature



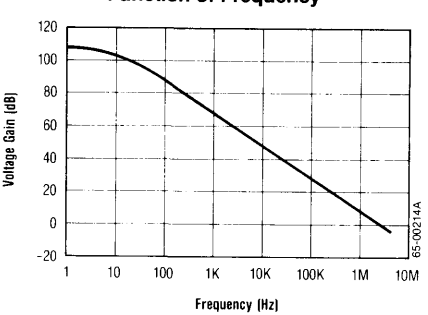
Input Offset Current as a Function of Ambient Temperature



Common Mode Range as a Function of Supply Voltage

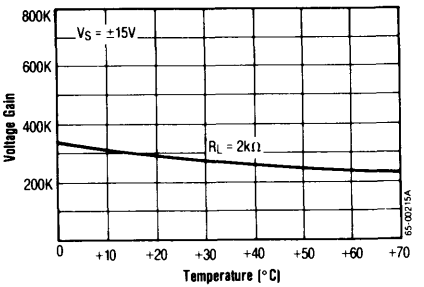


Open Loop Voltage Gain as a Function of Frequency

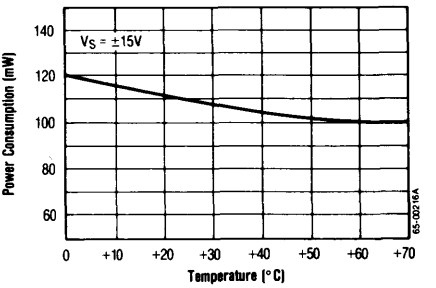


Typical Performance Characteristics (Continued)

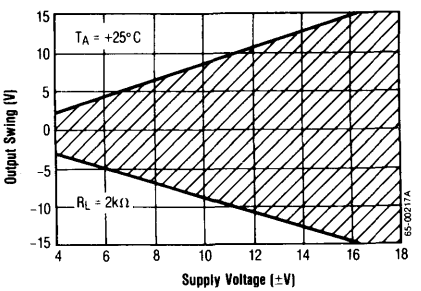
Open Loop Gain as a Function of Temperature



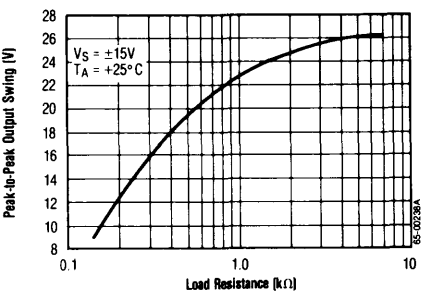
Power Consumption as a Function of Ambient Temperature



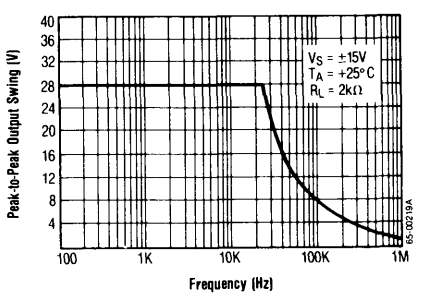
Typical Output Voltage as a Function of Supply Voltage



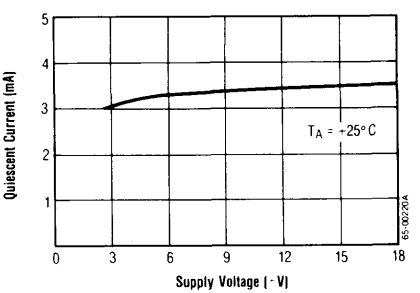
Output Voltage Swing as a Function of Load Resistance



Output Voltage Swing as a Function of Frequency

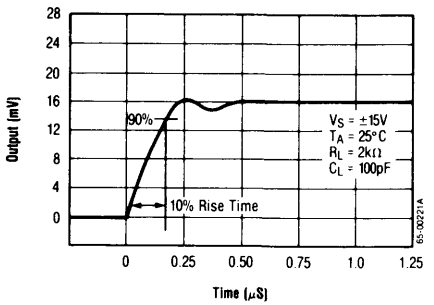


Quiescent Current as a Function of Supply Voltage

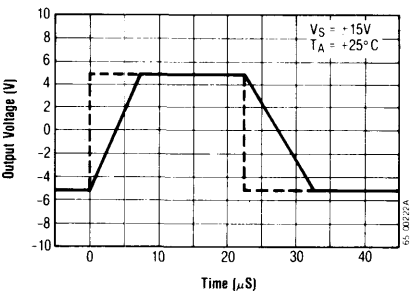


Typical Performance Characteristics (Continued)

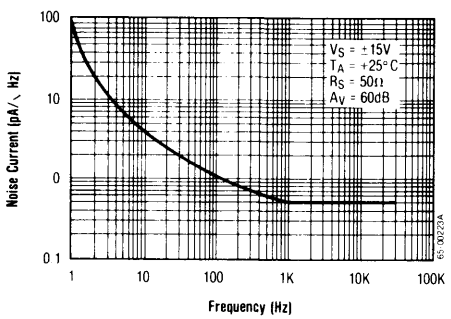
Transient Response



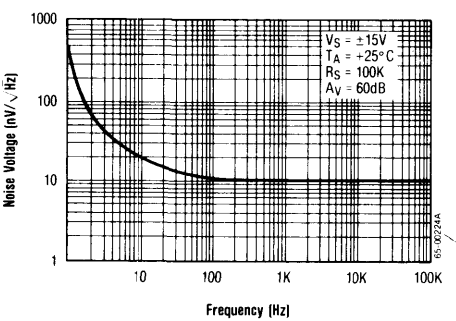
Voltage Follower Large Signal Pulse Response



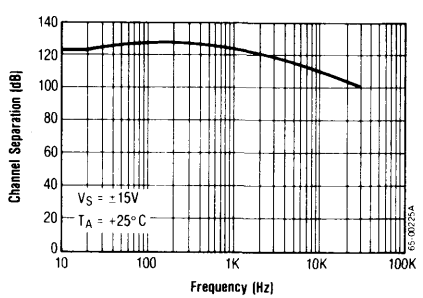
Input Noise Current as a Function of Frequency



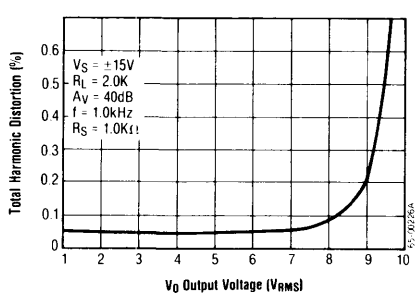
Input Noise Voltage as a Function of Frequency



Channel Separation

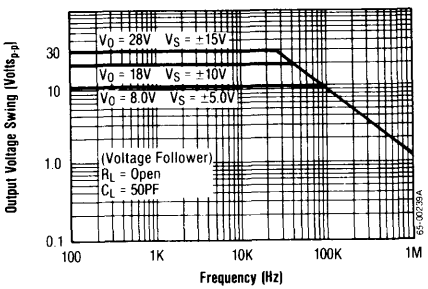


Total Harmonic Distortion vs. Output Voltage

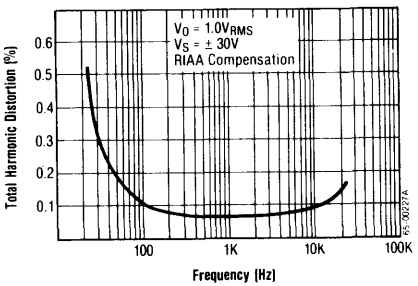


Typical Performance Characteristics (Continued)

Output Voltage Swing vs. Frequency

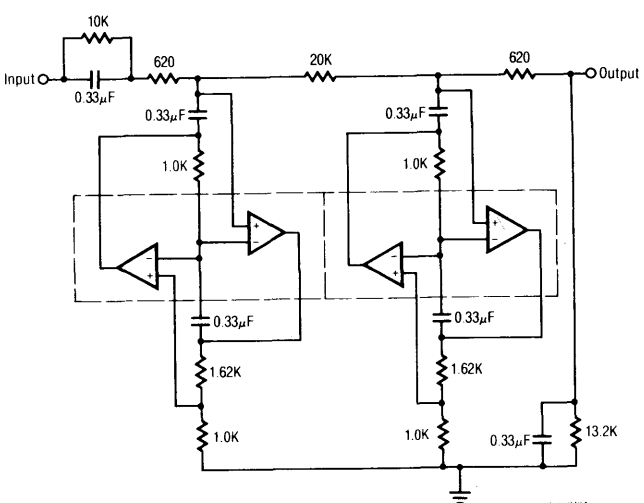


Distortion vs. Frequency



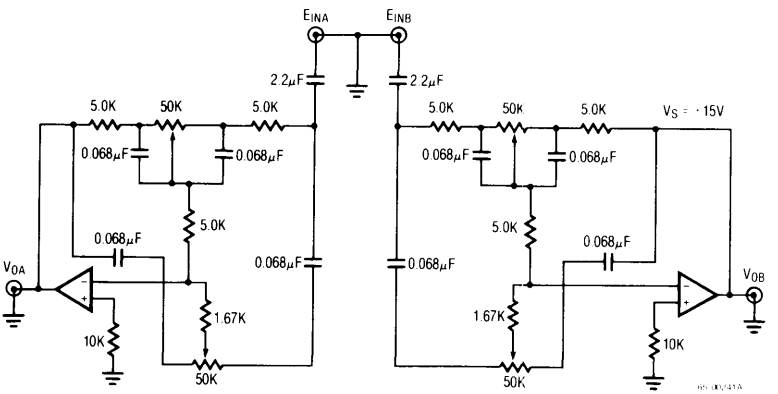
Typical Applications

400Hz Lowpass Butterworth Active Filter

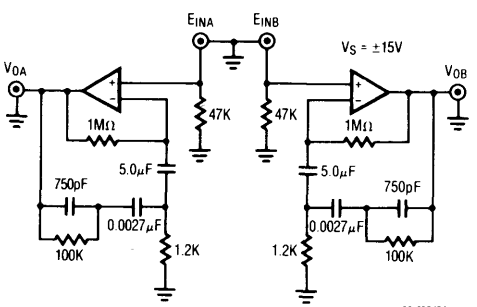


Typical Applications (Continued)

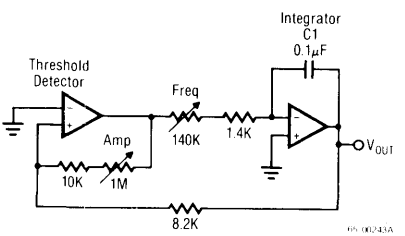
Stereo Tone Control



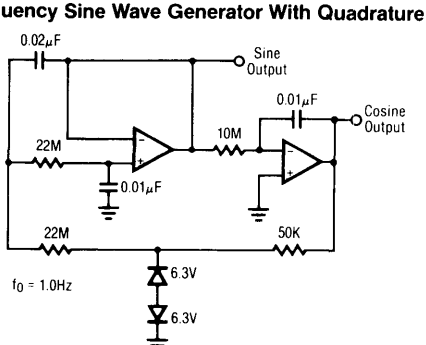
RIAA Preamplifier



Triangular-Wave Generator



Low Frequency Sine Wave Generator With Quadrature Output



Raytheon

Wide-Bandwidth Dual Operational Amplifier

RC4560

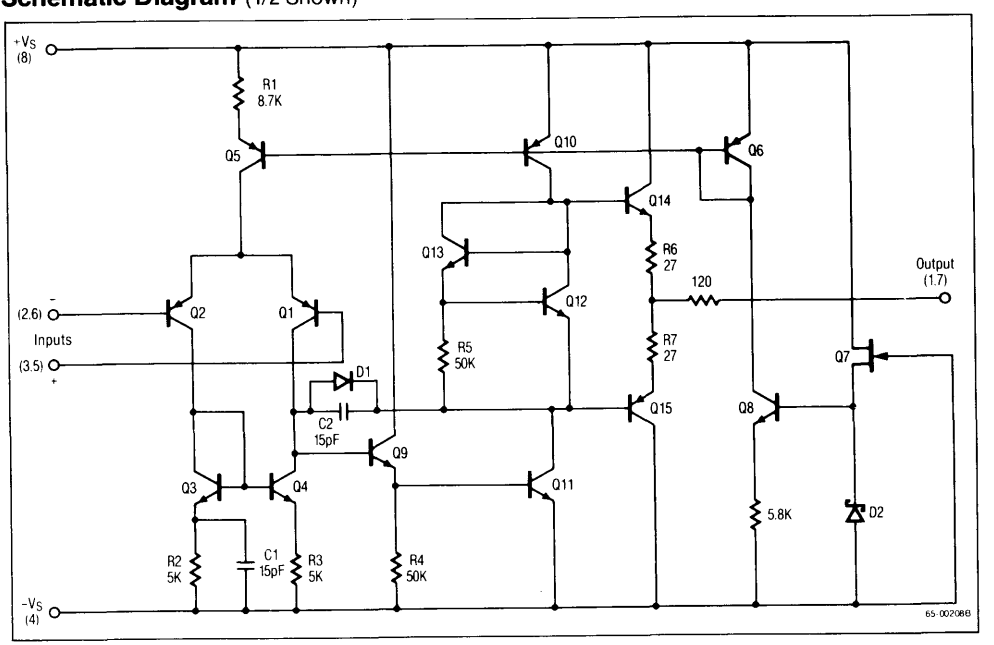
Features

- Unity gain bandwidth (A_V = 1) — 10MHz
- Slew rate — 4.0V/μS
- Noise voltage at 1kHz — 7.0nV/$\sqrt{Hz}$
- Noise voltage current at 1kHz — 0.4pA/$\sqrt{Hz}$
- ±10V Output into 400Ω loads (±25mA)
- Supply current per amplifier — 1.8mA
- Input offset voltage — 2.0mV
- Input offset current — 5.0nA
- Unity gain frequency compensated
- Output short circuit protected

Description

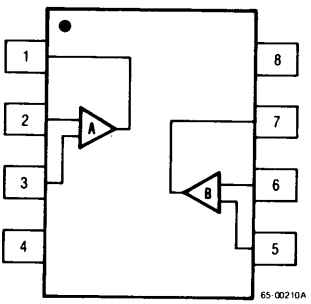
The 4560 integrated circuit is a high-gain, wide-bandwidth, dual operational amplifier capable of driving 20V peak-to-peak into 400Ω loads. The 4560 combines many of the features of the 4558 as well as providing the capability of wider bandwidth, and higher slew rate make the 4560 ideal for active filters, data and telecommunications, and many instrumentation applications. The availability of the 4560 in the surface mounted micro-package allows the 4560 to be used in critical applications requiring very high packing densities.

Schematic Diagram (1/2 Shown)



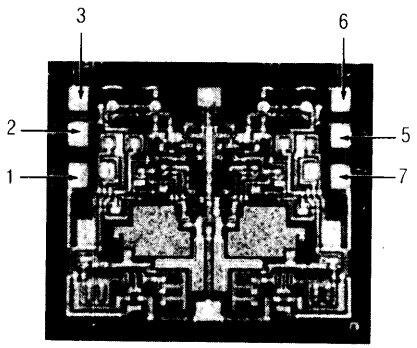
Connection Information

8-Lead
Dual In-Line Package
(Top View)



Pin	Function
1	A Output
2	A -Input
3	A +Input
4	$+V_S$
5	B +Input
6	B -Input
7	B Output
8	$-V_S$

Mask Pattern



Die Size: 52 x 61 mils
Min. Pad Dimensions: 4 x 4 mils

Thermal Characteristics

	8-Lead Micro-Pak Plastic DIP	8-Lead Plastic DIP
Max. Junction Temp.	125°C	125°C
Max. P_D T_A < 50°C	300mW	468mW
Therm. Res. θ_{JC}	—	—
Therm. Res. θ_{JA}	240°C/W	160°C/W
For T_A > 50°C Derate at	4.17mW per °C	6.25mW per °C

Ordering Information

Part Number	Package	Operating Temperature Range
RC4560M	Micro-Plastic	-20°C to +75°C
RC4560NB	Plastic	-20°C to +75°C

Absolute Maximum Ratings

Supply Voltage ..... ±18V
Input Voltage[1] ..... ±15V
Differential Input Voltage 30V
Output Short Circuit Duration[2] ..... Indefinite
Operating Temperature
Range ..... -20°C to +75°C
Lead Soldering Temperature (10 Sec)
RC4560NB ..... +300°C
RC4560M ..... +260°C

Notes: 1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Short circuit may be to ground on one amp only. Rating applies to +75°C ambient temperature.

Matching Characteristics

(V_S = ±15V, T_A = +25°C)

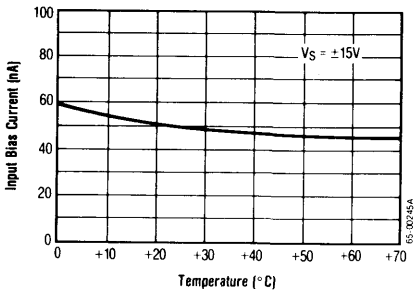
Parameter	Conditions	Typ	Units
Voltage Gain	$R_L \geq 2k\Omega$	±1.0	dB
Input Bias Current		±15	nA
Input Offset Current		±7.5	nA
Input Offset Voltage	$R_S \geq 10k\Omega$	±0.2	mV

Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise specified)

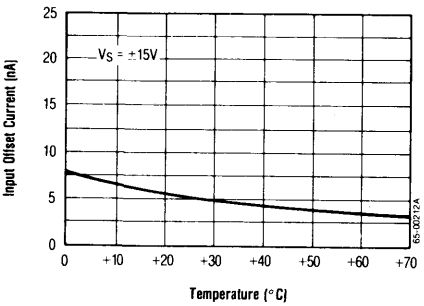
Parameters	Test Conditions	Min	Typ	Max	Units
Input Offset Voltage	$R_S \leq 10k\Omega$		2.0	6.0	mV
Input Offset Current			5.0	200	nA
Input Bias Current			50	500	nA
Input Resistance (Differential Mode)		0.3	0.1		MΩ
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	20	300		V/mV
Output Voltage Swing	$R_L \geq 10k\Omega$	±12	±14		V
	I_O = 25mA	±10	±11.5		
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	90		dB
Power Supply Rejection Ratio	$R_S \leq 10k\Omega$	76	90		dB
Power Consumption	$R_L = \infty$		135	200	mW
Transient Response Rise Time	V_{IN} = 20mV, R_L = 2kΩ		0.05		μS
Overshoot	$C_L \leq 100pF$, Gain = 1		35		%
Slew Rate	$R_L \leq 2k\Omega$, Gain = 1		4.0		V/μS
Channel Separation	f = 10kHz R_S = 1kΩ, Gain = 100		100		dB
Unity Gain Bandwidth	A_V = +1, V_O = -3dB		10		MHz
The following specifications apply for $-20°C \leq T_A \leq +75°C$					
Input Offset Voltage	$R_S \leq 10k\Omega$			7.0	mV
Input Offset Current				300	nA
Input Bias Current				800	nA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	15			V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	±10			V
Power Consumption	T_A = +75°C		135	200	mW
	T_A = -20°C		165	230	

Typical Performance Characteristics

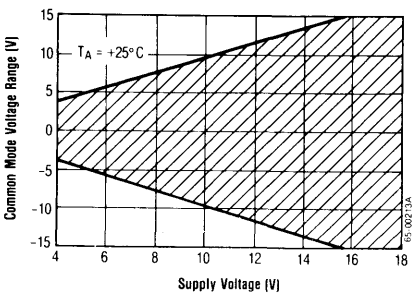
Input Bias Current as a Function of Ambient Temperature



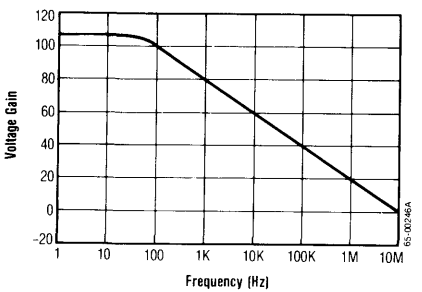
Input Offset Current as a Function of Ambient Temperature



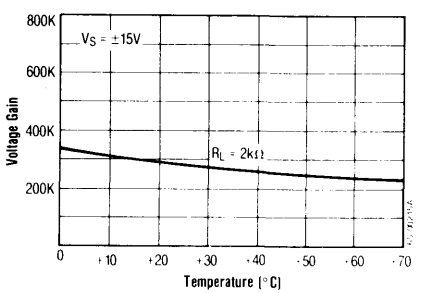
Common Mode Range as a Function of Supply Voltage



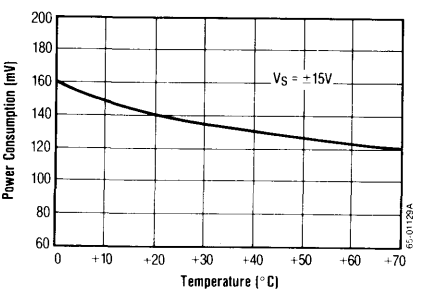
Open Loop Voltage Gain as a Function of Frequency



Open Loop Gain as a Function of Temperature

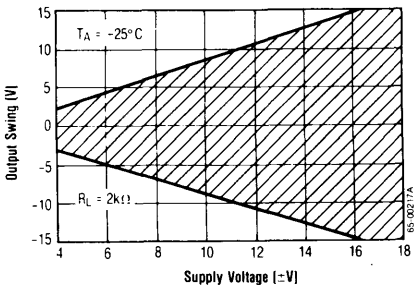


Power Consumption as a Function of Ambient Temperature

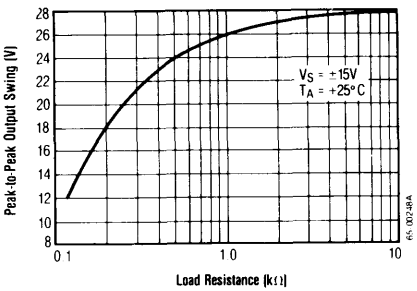


Typical Performance Characteristics (Continued)

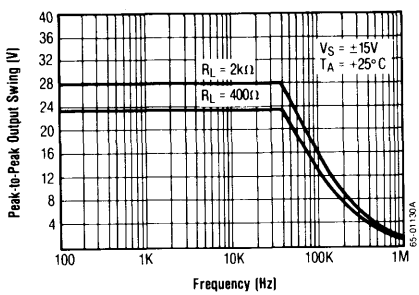
Typical Output Voltage as a Function of Supply Voltage



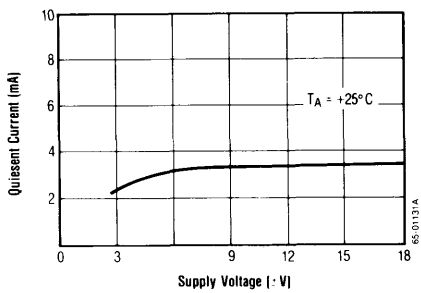
Output Voltage Swing as a Function of Load Resistance



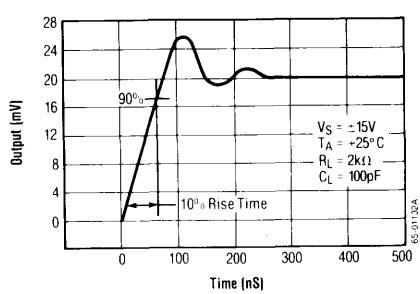
Output Voltage Swing as a Function of Frequency



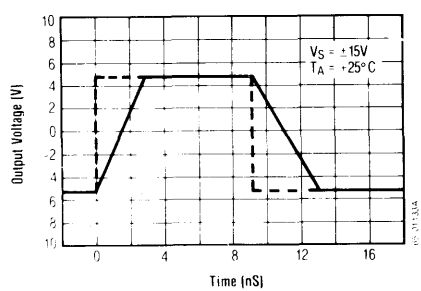
Quiescent Current as a Function of Supply Voltage



Transient Response

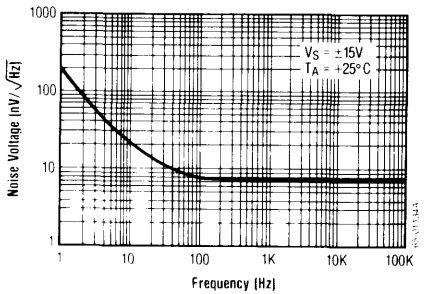


Voltage Follower Large Signal Pulse Response

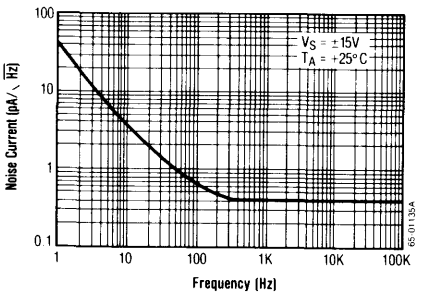


Typical Performance Characteristics (Continued)

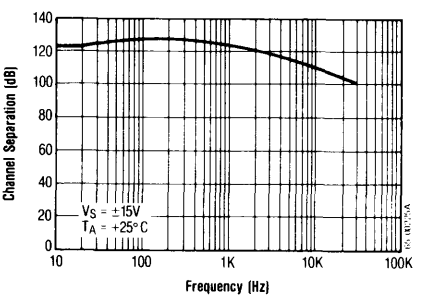
Input Noise Voltage as a Function of Frequency



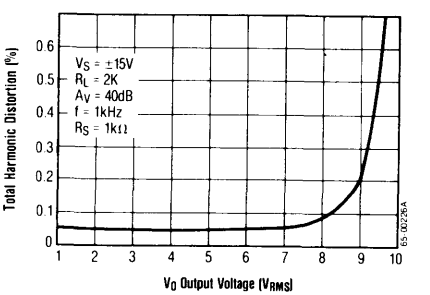
Input Noise Current as a Function of Frequency



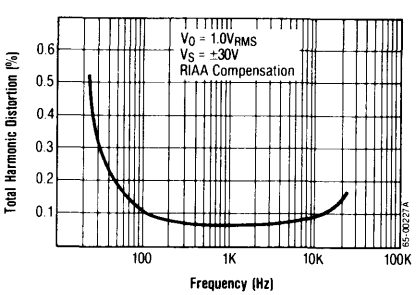
Channel Separation



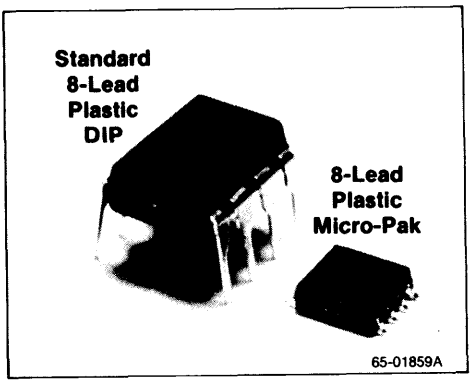
Total Harmonic Distortion vs. Output Voltage



Distortion vs. Frequency



Comparison of Standard vs. Micro-Package



Raytheon

Decompensated Wide-Bandwidth Dual Operational Amplifier

RC4562

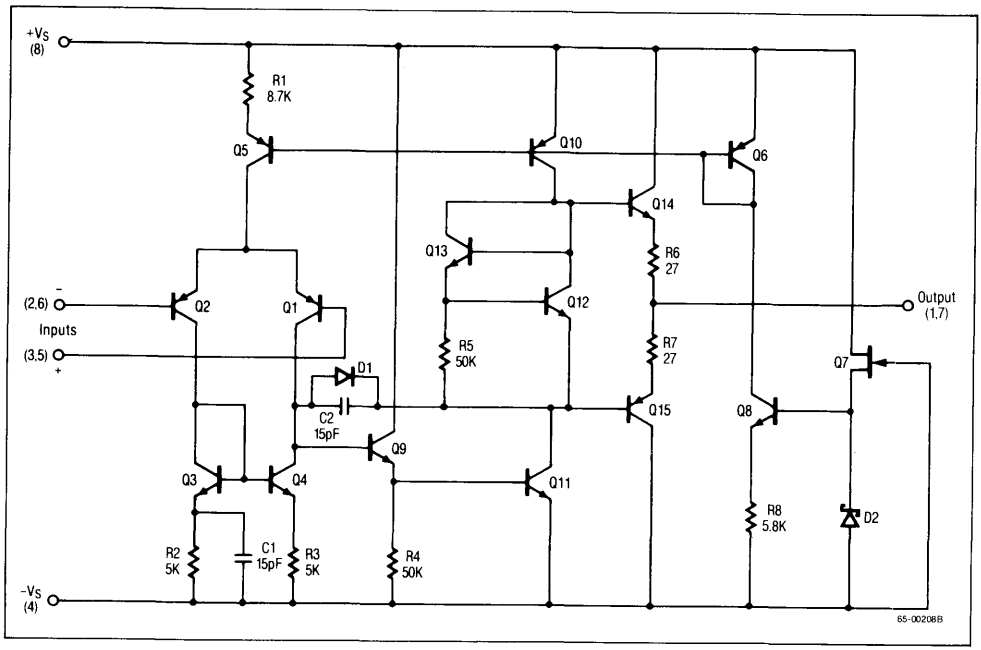
Features

- Frequency compensated for gains >10
- Unity gain bandwidth — 15MHz
- Slew rate — 7.0V/μS
- Noise voltage at 1kHz — 5.5nV/$\sqrt{Hz}$
- Noise current at 1kHz — 0.2pA/$\sqrt{Hz}$
- ±10V Output into 600Ω loads
- 0.005% distortion at $9.0V_{RMS}$
- Supply current per amplifier — 1.8mA
- Output short circuit protected

Description

The 4562 integrated circuit is a high gain, wide-bandwidth, low noise, dual operational amplifier capable of driving 20V peak-to-peak into 600Ω loads. The 4562 is frequency compensated for closed loop gains greater than 10. The 4562 combines many of the features of the popular 4558 as well as providing the capability of wider bandwidth, and higher slew rate and less noise make the 4562 ideal for audio preamplifiers, active filters, telecommunications, and many instrumentation applications. The availability of the 4562 in the surface mounted micro-package allows the 4562 to be used in critical applications requiring very high packing densities.

Schematic Diagram (1/2 Shown)

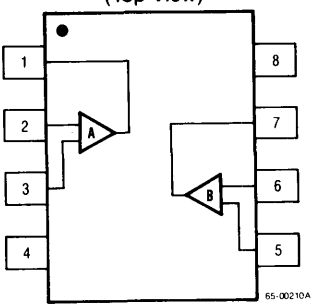


RC4562

Decompensated Wide-Bandwidth Dual Operational Amplifier

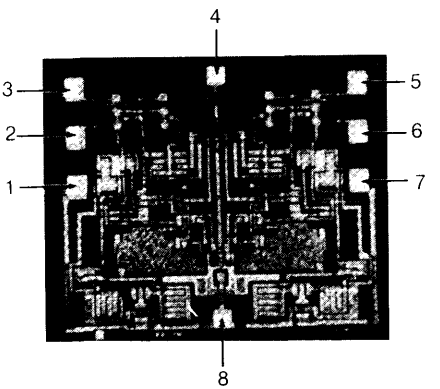
Connection Information

8-Lead
Dual In-Line Package
(Top View)



Pin	Function
1	A Output
2	A -Input
3	A +Input
4	$-V_S$
5	B +Input
6	B -Input
7	B Output
8	$+V_S$

Mask Pattern



Die Size: 52 x 61 mils
Min. Pad Dimensions: 4 x 4 mils

Thermal Characteristics

	8-Lead Micro-Pak Plastic DIP	8-Lead Plastic DIP
Max. Junction Temp.	125°C	125°C
Max. P_D T_A < 50°C	300mW	468mW
Therm. Res. θ_{JC}	—	—
Therm. Res. θ_{JA}	240°C/W	160°C/W
For T_A > 50°C Derate at	4.17mW per °C	6.25mW per °C

Ordering Information

Part Number	Package	Operating Temperature Range
RC4562M	Micro-Plastic	-20°C to +75°C
RC4562NB	Plastic	-20°C to +75°C

Absolute Maximum Ratings

Supply Voltage ..... ±18V
Input Voltage[1] ..... ±15V
Differential Input Voltage 30V
Output Short Circuit Duration[2] ..... Indefinite
Operating Temperature Range ..... -20°C to +75°C
Lead Soldering Temperature (10 Sec)
RC4562NB ..... +300°C
RC4562M ..... +260°C

Notes: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Short circuit may be to ground on one amp only. Rating applies to +75°C ambient temperature.

Matching Characteristics

(V_S = ±15V, T_A = +25°C)

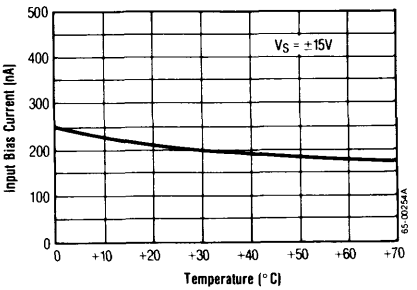
Parameter	Conditions	Typ	Units
Voltage Gain	$R_L \geq 2k\Omega$	±1.0	dB
Input Bias Current		±15	nA
Input Offset Current		±7.5	nA
Input Offset Voltage	$R_S \leq 10k\Omega$	±0.2	mV

Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise specified)

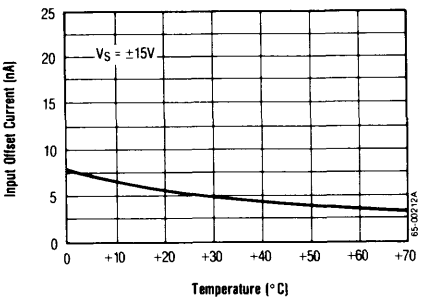
Parameters	Test Conditions	Min	Typ	Max	Units
Input Offset Voltage	$R_S \leq 10k\Omega$		1.0	6.0	mV
Input Offset Current			5.0	200	nA
Input Bias Current			200	500	nA
Input Resistance		0.3	1.0		MΩ
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	20	300		V/mV
Output Voltage Swing	$R_L \geq 10k\Omega$	±12	±14		V
	$R_L \geq 2k\Omega$	±10	±13		
Input Voltage Range		±12	±14		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	90		dB
Power Supply Rejection Ratio	$R_S \leq 10k\Omega$	76	90		dB
Power Consumption (All Amplifiers)	$R_L = \infty$		100	170	mW
Transient Response Rise Time	V_{IN} = 20mV, R_L = 2kΩ		0.06		μS
Overshoot	$C_L \leq 100pF$, Gain = 10		60		%
Slew Rate	$R_L \leq 2k\Omega$, Gain = 10		7.0		V/μS
Channel Separation	f = 10kHz R_S = 1kΩ, Gain = 100		90		dB
Unity Gain Bandwidth	Gain = 10	8.5	15		MHz
The following specifications apply for $-20°C \leq T_A \leq +75°C$					
Input Offset Voltage	$R_S \leq 10k\Omega$			7.5	mV
Input Offset Current				300	nA
Input Bias Current				800	nA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	15			V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	±10			V
Power Consumption	T_A = +75°C		90	150	mW
	T_A = -20°C		120	200	

Typical Performance Characteristics

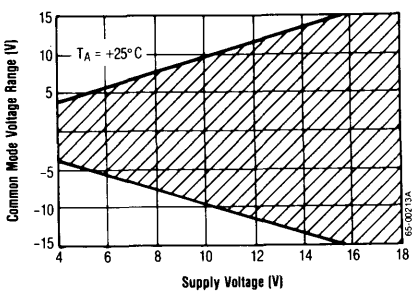
Input Bias Current as a Function of Ambient Temperature



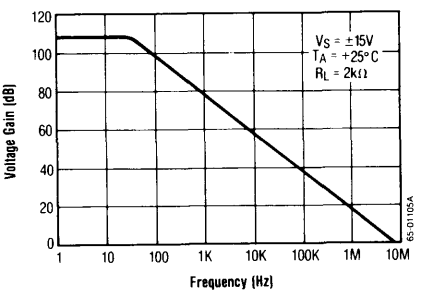
Input Offset Current as a Function of Ambient Temperature



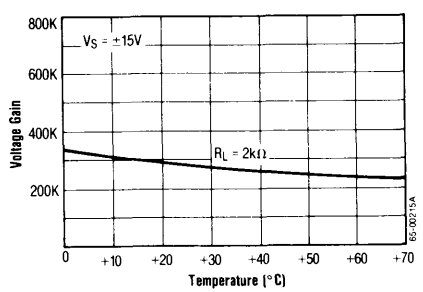
Common Mode Range as a Function of Supply Voltage



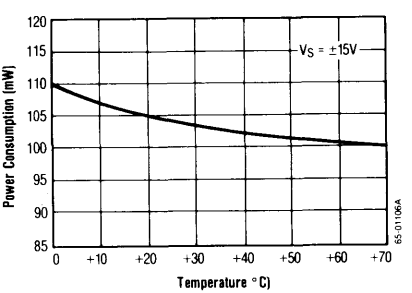
Open Loop Voltage Gain as a Function of Frequency



Open Loop Gain as a Function of Temperature

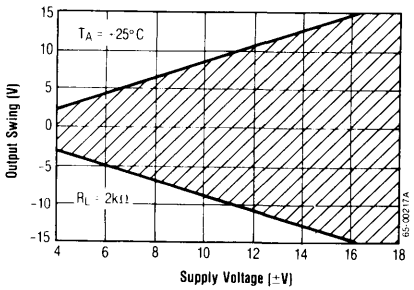


Power Consumption as a Function of Ambient Temperature

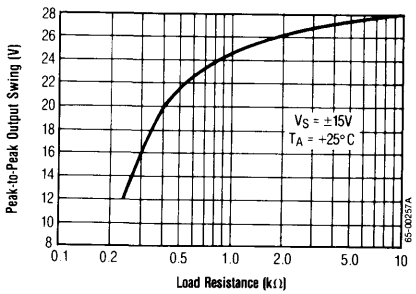


Typical Performance Characteristics (Continued)

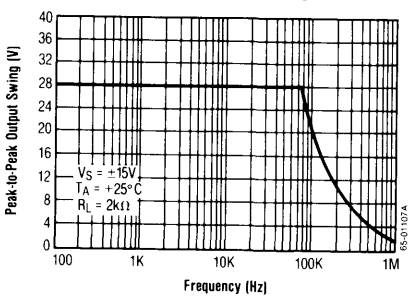
Typical Output Voltage as a Function of Supply Voltage



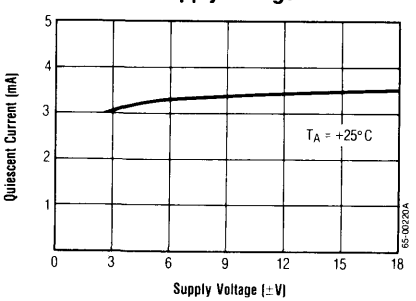
Output Voltage Swing as a Function of Load Resistance



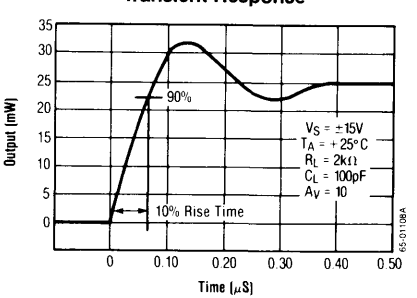
Output Voltage Swing as a Function of Frequency



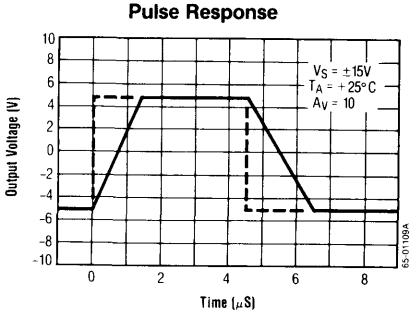
Quiescent Current as a Function of Supply Voltage



Transient Response

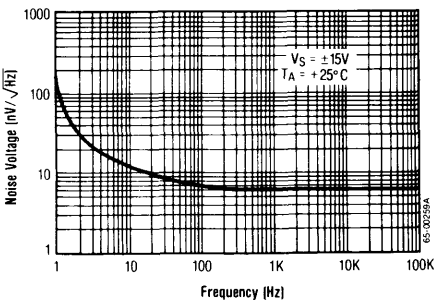


Voltage Follower Large Signal Pulse Response

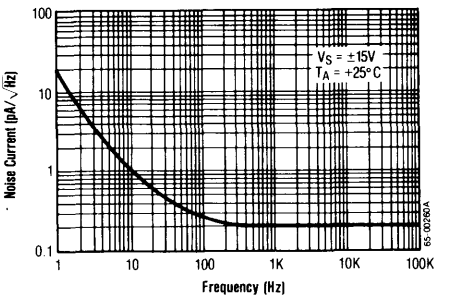


Typical Performance Characteristics (Continued)

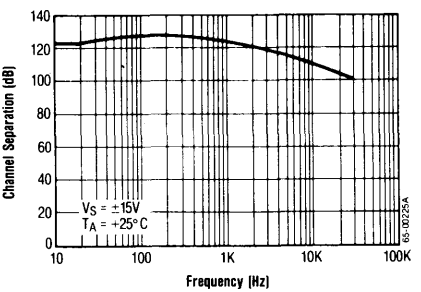
Input Noise Voltage as a Function of Frequency



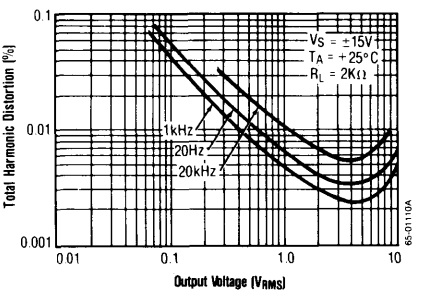
Input Noise Current as a Function of Frequency



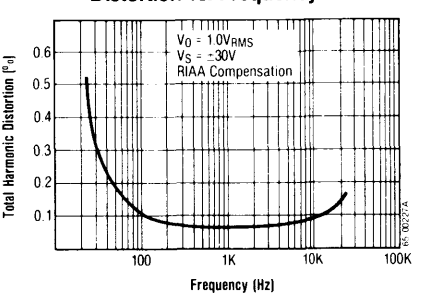
Channel Separation



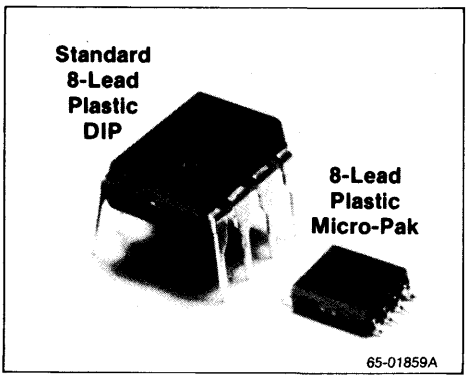
Total Harmonic Distortion vs. Output Voltage



Distortion vs. Frequency



Comparison of Standard vs Micro-Pak



Raytheon

Low Noise Dual Operational Amplifier

RC4739

Features

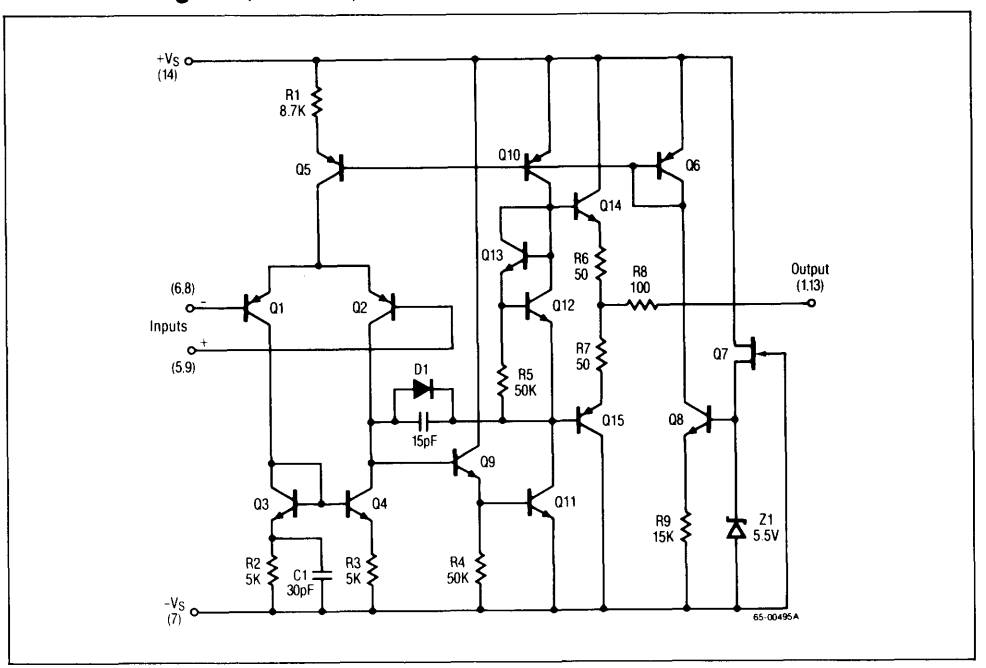
- Internally compensated replacement for μA739 and MC1303
- Signal-to-noise ratio — 76dB (RIAA 10mV ref.)
- Channel separation — 125dB
- Unity gain bandwidth — 3MHz
- Output short-circuit protected
- <0.05% distortion into 2kΩ load
- 10nV/$\sqrt{Hz}$ noise at 100Hz

Description

The RC4739 low noise dual operational amplifier is fabricated on a single silicon chip using the planar epitaxial process. It was designed primarily for preamplifiers in consumer and industrial signal processing equipment. The device is pin compatible with the μA739 and MC1303, however, compensation is internal. This permits a lowered external parts count and simplified application.

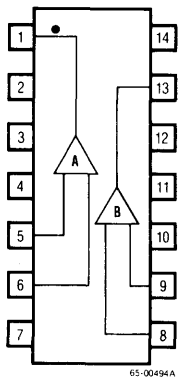
The RC4739 is available in molded dual in-line 14-pin package and operates over the commercial temperature range from 0° C to +70° C.

Schematic Diagram (1/2 Shown)



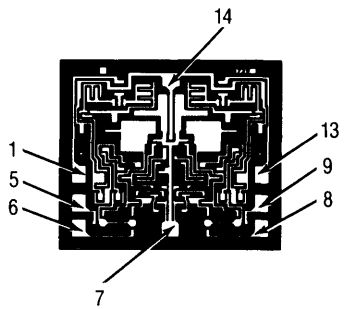
Connection Information

14-Lead
Dual In-Line Package
(Top View)



Pin	Function
1	A Output
2	NC
3	NC
4	NC
5	+A Input
6	-A Input
7	$-V_S$
8	-B Input
9	+B Input
10	NC
11	NC
12	NC
13	B Output
14	$+V_S$

Mask Pattern



Die Size: 52 x 61 mils
Min. Pad Dimensions: 4 x 4 mils

Absolute Maximum Ratings

Supply Voltage ..... ±18V
Input Voltage[1] ..... ±15V
Differential Input Voltage 30V
Output Short Circuit Duration[2] ..... Indefinite
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature
Range ..... 0°C to +70°C
Lead Soldering Temperature
(60 Sec) ..... +300°C

Notes: 1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Short circuit may be to ground, typically 45mA.

Thermal Characteristics

	14-Lead Plastic DIP
Max. Junction Temp.	125°C
Max. P_D T_A < 50°C	468mW
Therm. Res. θ_{JC}	—
Therm. Res. θ_{JA}	160°C/W
For T_A > 50°C Derate at	6.25mW per °C

Ordering Information

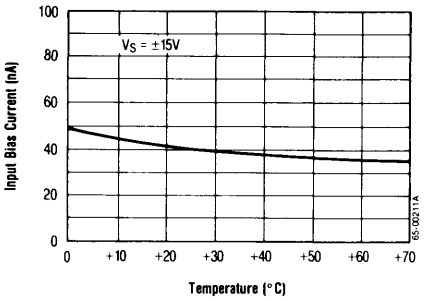
Part Number	Package	Operating Temperature Range
RC4739DB	Plastic	0°C to +70°C

Electrical Characteristics (V_S = +15V and T_A = +25°C)

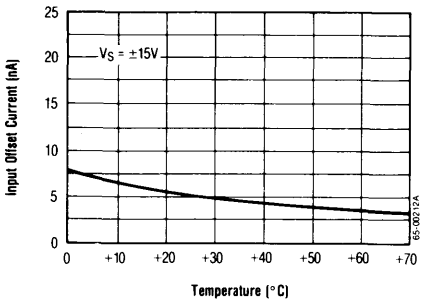
Parameters	Test Conditions	Min	Typ	Max	Units
Input Offset Voltage	$R_S \leq 10k\Omega$		2.0	6.0	mV
Input Offset Current			5.0	200	nA
Input Bias Current			40	500	nA
Input Resistance (Differential Mode)		0.3	5.0		MΩ
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$	20	300		V/mV
Output Voltage Swing	$R_L \geq 10k\Omega$	±12	±14		V
	$R_L \geq 2k\Omega$	±10	±13		
Input Voltage Range		±12	±14		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	100		dB
Power Supply Rejection Ratio	$R_S \leq 10k\Omega$	76	100		dB
Power Consumption			105	170	mW
Transient Response Rise Time	V_{IN} = 20mV, R_L = 2kΩ		0.15		μS
Overshoot	$C_L \leq 100pF$		10		%
Slew Rate	$R_L \geq 2k\Omega$		1.0		V/μS
Input Voltage Noise	B_W = 10-30kHz, R_S = 1kΩ		2.5		μV_{RMS}
Channel Separation	f = 1.0kHz, A_V = 40dB, R_S = 1kΩ		125		dB
The following specification applies for 0°C ≤ T_A ≤ +70°C unless otherwise specified. V_S = ±15V					
Input Offset Voltage	$R_S \leq 10k\Omega$		3.0	7.5	mV
Input Offset Current			7.0	300	nA
Input Bias Current			50	800	nA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$	15	200		V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$, $V_S = \pm 15V$	±10	±13		V
Power Consumption	T_S = +70°C		100	150	mW
	T_A = 0°C		110	220	mW

Typical Performance Characteristics

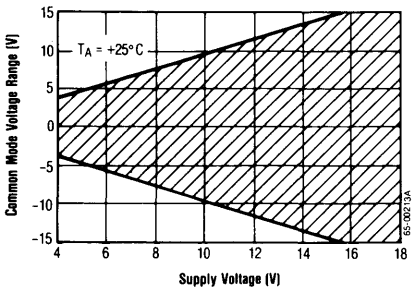
Input Bias Current as a Function of Ambient Temperature



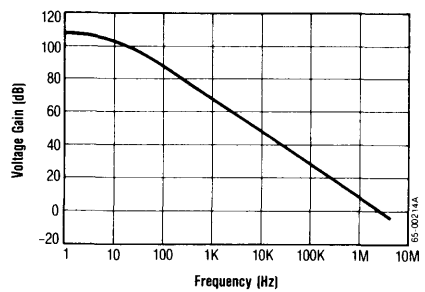
Input Offset Current as a Function of Ambient Temperature



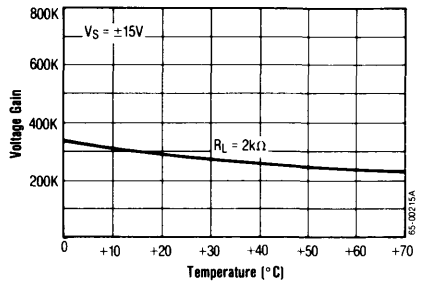
Common Mode Range as a Function of Supply Voltage



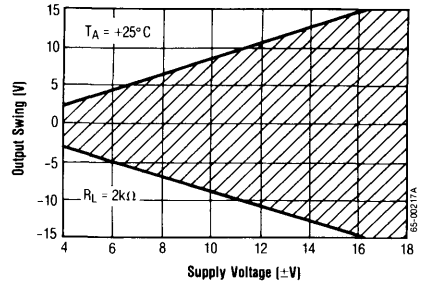
Open Loop Voltage Gain as a Function of Frequency



Open Loop Gain as a Function of Temperature

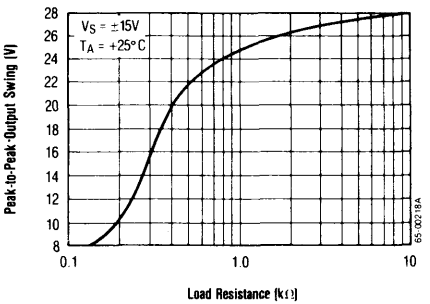


Typical Output Voltage as a Function of Supply Voltage

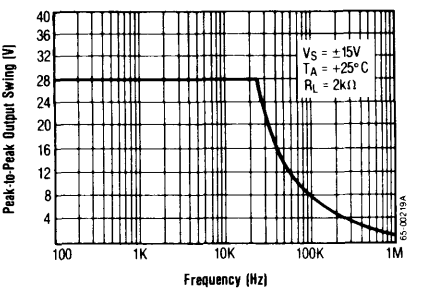


Typical Performance Characteristics (Continued)

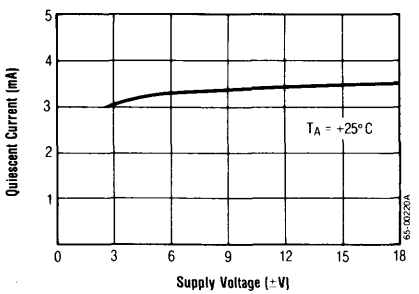
Output Voltage Swing as a Function of Load Resistance



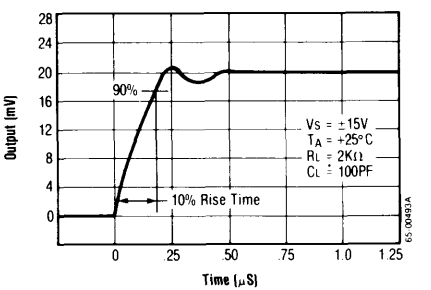
Output Voltage Swing as a Function of Frequency



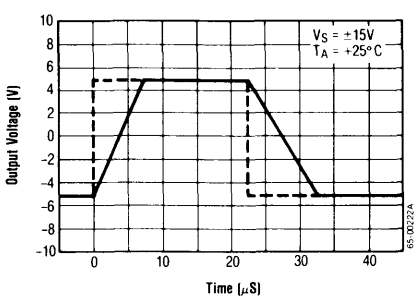
Quiescent Current as a Function of Supply Voltage



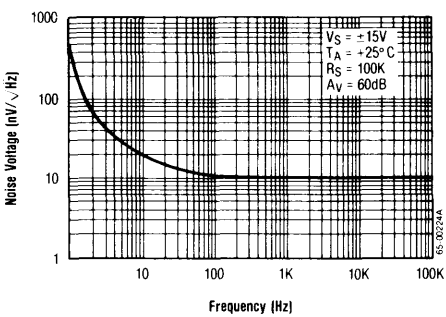
Transient Response



Voltage Follower Large Signal Pulse Response

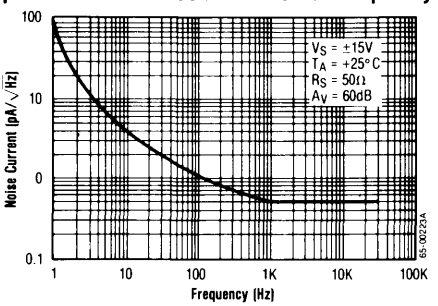


Input Noise Voltage as a Function of Frequency

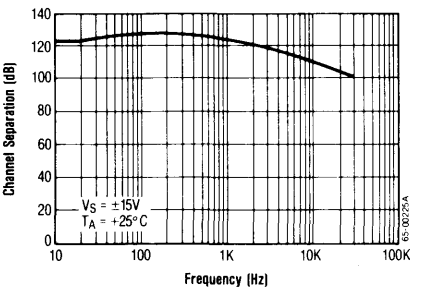


Typical Performance Characteristics (Continued)

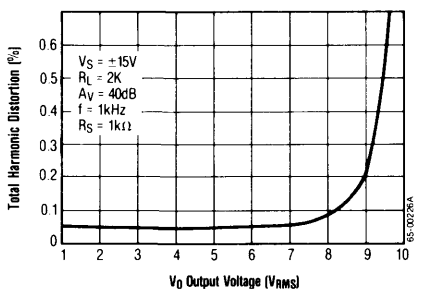
Input Noise Current as a Function of Frequency



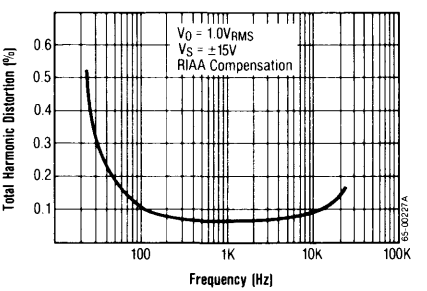
Channel Separation



Total Harmonic Distortion vs. Output Voltage

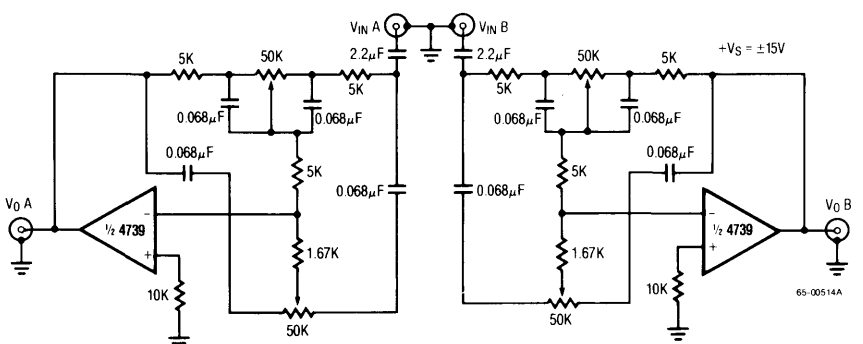


Distortion vs. Frequency



Typical Applications

Stereo Tone Control



High Performance Dual Low Noise Operational Amplifier

Raytheon

RC5532, 5532A

Features

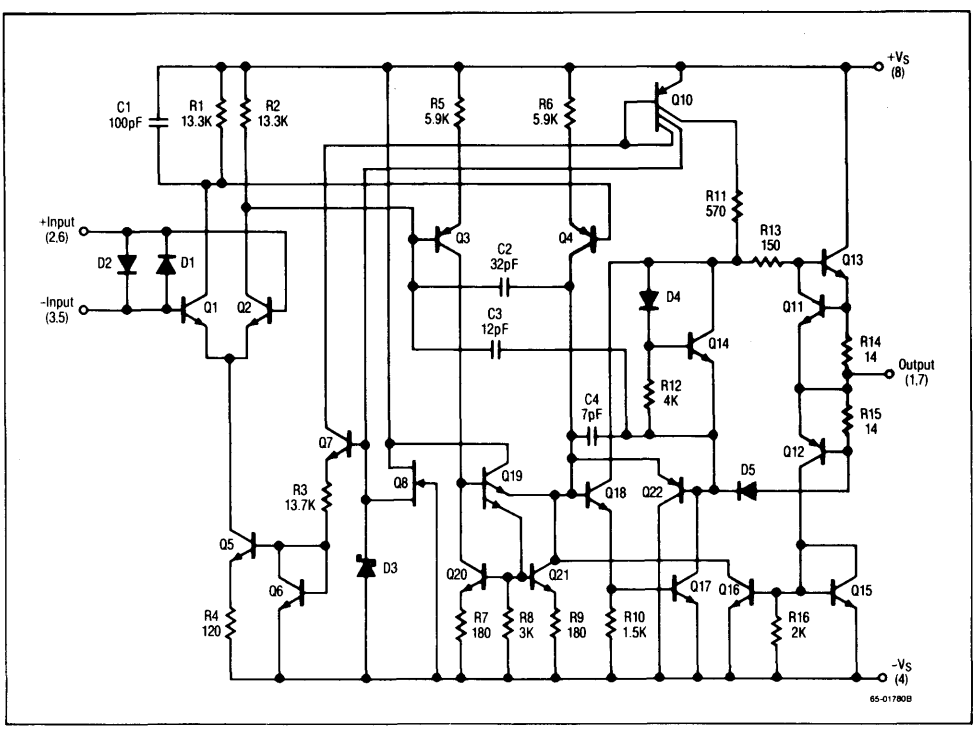
- Small signal bandwidth — 10MHz
- Output drive capability — 600Ω, 10V (rms)
- Input noise voltage — 5nV/√Hz
- DC voltage gain — 50,000
- AC voltage gain — 2200 at 10kHz
- Power bandwidth — 140kHz
- Slew rate — 8V/μS
- Large supply voltage range — ±3 to ±20V

Description

The 5532 is a high performance dual low noise operational amplifier. Compared to the standard dual operational amplifiers, such as the 1458, it shows better noise performance, improved output drive capability, and considerably higher small-signal and power bandwidths.

This makes the device especially suitable for application in high quality and professional audio equipment, instrumentation, and control circuits, and telephone channel amplifiers. The op amp is internally compensated for gains equal to one. If very low noise is of prime importance, it is recommended that the 5532A version be used which has guaranteed noise specifications.

Schematic Diagram (1/2 Shown for 5532)

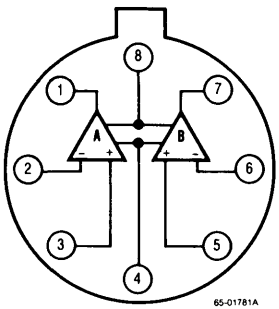


RC5532, 5532A

High Performance Dual Low Noise Operational Amplifier

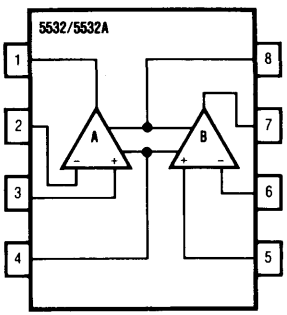
Connection Information

8-Lead TO-99 Package (Top View)



65-01781A

8-Lead DE/NB Package (Top View)



65-01782A

Pin	Function
1	Output A
2	Inverting Input A
3	Non-Inverting Input A
4	$-V_S$
5	Non-Inverting Input B
6	Inverting Input B
7	Output B
8	$+V_S$

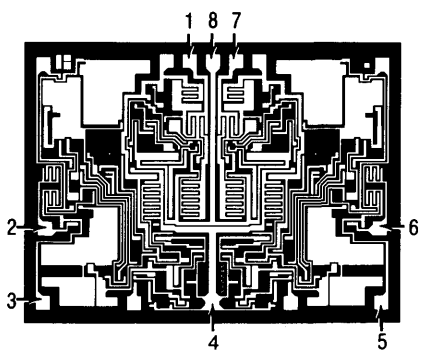
Absolute Maximum Ratings

Supply Voltage ..... ±22V
Input Voltage ..... ±V Supply
Differential Input Voltage[1] 0.5V
Operating Temperature Range
RM5532 ..... -55°C to +125°C
RV5532 ..... 0°C to +70°C
Storage Temperature
Range ..... -65°C to +150°C
Lead Soldering Temperature
(10 Sec) ..... +300°C

Thermal Characteristics

	8-Lead Plastic DIP	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can
Max. Junction Temp.	125°C	175°C	175°C
Max. P_D $T_A < 50°C$	468mW	833mW	658mW
Therm. Res. θ_{JC}	—	45°C/W	50°C/W
Therm. Res. θ_{JA}	160°C/W	150°C/W	190°C/W
For $T_A > 50°C$ Derate at	6.25mW per °C	8.33mW per °C	5.26mW per °C

Mask Pattern



Die Size: 78 x 104 mils
Min. Pad Dimensions: 4 x 4 mils

DC Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise noted)[2,3]

Parameters	Test Conditions	RM5532/5532A			RC5532/5532A			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage			0.5	2.0		0.5	4.0	mV
	Over Temperature			3.0			5.0	mV
Input Offset Current				100		10	150	nA
	Over Temperature			200			200	nA
Input Bias Current			200	400		200	800	nA
	Over Temperature			700			1000	nA
Supply Current			6.0	11		6.0	16	mA
	Over Temperature			13			22	mA
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio		80	100		70	100		dB
Power Supply Rejection Ratio		86	100		80	100		dB
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_O = ±10V	50			25	100		V/mV
	Over Temperature	25			15	50		V/mV
	$R_L \geq 600\Omega$, V_O = ±10V	40			15	50		V/mV
	Over Temperature	20			10			V/mV
Output Voltage Swing	$R_L \geq 600\Omega$	±12	±13		±12	±13		V
	$R_L \geq 600\Omega$, V_S = ±18V	±15	±16		±15	±16		V
	$R_L \geq 2k\Omega$	±12	±13					V
Input Resistance (Differential Mode)		30	300		30	300		kΩ
Short Circuit Current			38			38		mA

Notes: 1. Diodes protect the inputs against over-voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to ±10mA.
2. For RC5532/RC5532A: T_{MIN} = 0°C, T_{MAX} = +70°C
3. For RM5532/RM5532A: T_{MIN} = -55°C, T_{MAX} = +125°C

AC Electrical Characteristics (V_S = +15V and T_A = +25°C)

Parameters	Test Conditions	RC/RM5532/5532A Min	Typ	Max	Units
Output Resistance	A_V = 30dB Closed Loop f = 10kHz, R_L = 600Ω		0.3		Ω
Overshoot	Unity Gain V_{IN} = 100mV_{p-p} C_L = 10pF, R_L = 600Ω		10		%
Gain	f = 10kHz		2.2		V/mV
Gain Bandwidth Product	C_L = 100pF, R_L = 600Ω		10		MHz
Slew Rate			8.0		V/μS
Power Bandwidth	V_{OUT} = ±10V V_{OUT} = ±14V, R_L = 600Ω V_{CC} = ±18V		140 100		kHz kHz

Electrical Characteristics (V_S = +15V and T_A = +25°C)

Parameters	Test Conditions	RC/RM5532 Min	Typ	Max	RC/RM5532A Min	Typ	Max	Units
Input Noise Voltage Density	f_0 = 30Hz f_0 = 1kHz		8.0 5.0			8.0 5.0	12. 6.0	nV/$\sqrt{Hz}$
Input Noise Current Density	f_0 = 30Hz f_0 = 1kHz		2.7 0.7			2.7 0.7		pA/$\sqrt{Hz}$
Channel Separation	f = 1kHz, R_S = 5kΩ		110			110		dB

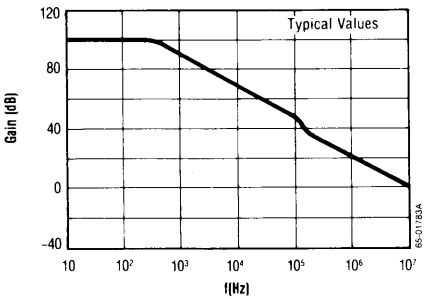
Ordering Information

Part Number	Package	Operating Temperature Range
RC5532NB	Plastic	0°C to +70°C
RC5532ANB	Plastic	0°C to +70°C
RC5532DE	Ceramic	0°C to +70°C
RC5532ADE	Ceramic	0°C to +70°C
RC5532T	TO-99	0°C to +70°C
RC5532AT	TO-99	0°C to +70°C
RM5532DE	Ceramic	-55°C to +125°C
RM5532DE/883B*	Ceramic	-55°C to +125°C
RM5532ADE	Ceramic	-55°C to +125°C
RM5532ADE/883B*	Ceramic	-55°C to +125°C
RM5532T	TO-99	-55°C to +125°C
RM5532T/883B*	TO-99	-55°C to +125°C
RM5532AT	TO-99	-55°C to +125°C
RM5532AT/883B*	TO-99	-55°C to +125°C

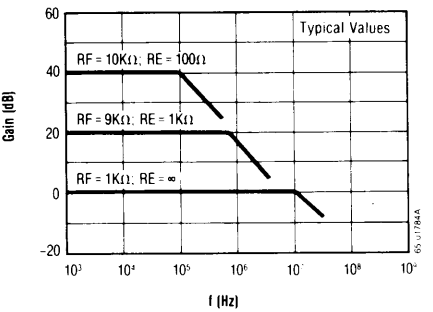
*MIL-STD-883, Level B Processing

Typical Performance Characteristics

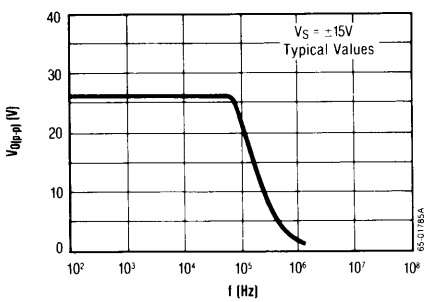
Open Loop Frequency Response



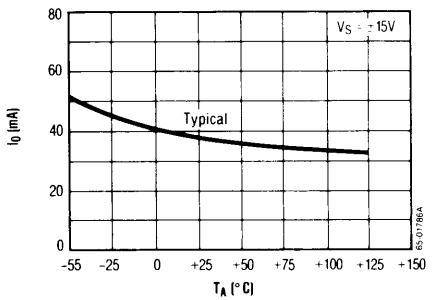
Closed Loop Frequency Response



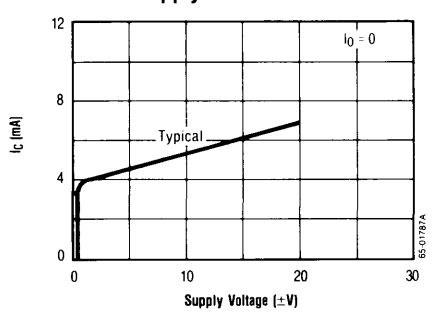
Large Signal Frequency Response



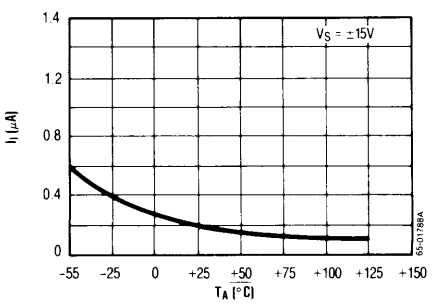
Output Short Circuit Current



Supply Current

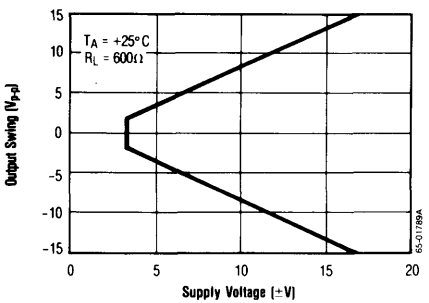


Input Bias Current

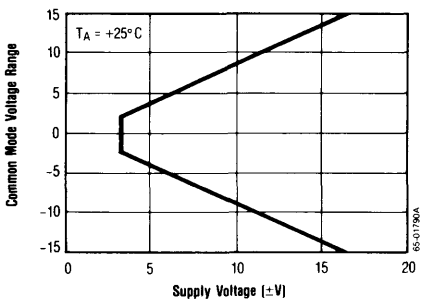


Typical Performance Characteristics (Continued)

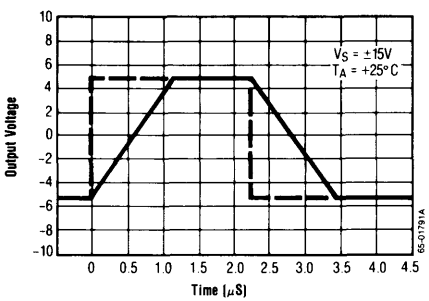
Typical Output Voltage as a Function of Supply Voltage



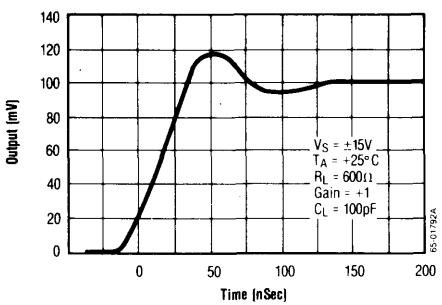
Common Mode Range as a Function of Supply Voltage



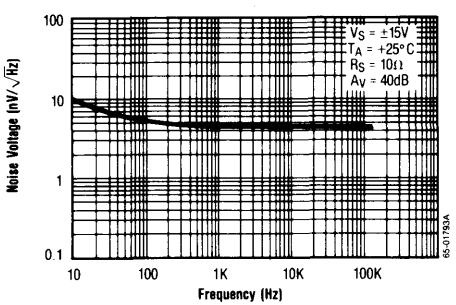
Voltage Follower Large Signal Pulse Response



Transient Response

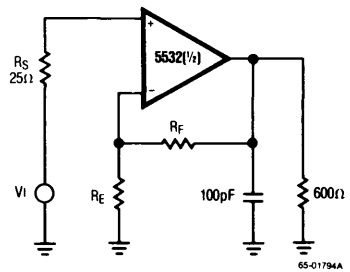


Input Noise Voltage Density

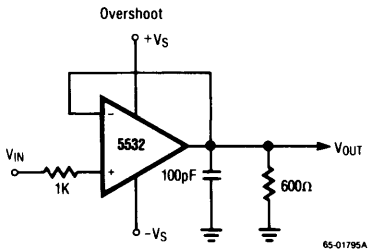


Test Circuits

Closed Loop Frequency Response



Voltage Follower



Raytheon

High Performance Low Noise Operational Amplifier

RC5534, 5534A

Features

- Small signal bandwidth — 10MHz
- Output drive capability — 600Ω, $10V_{RMS}$ at $V_S = \pm 18V$
- Input noise voltage — $4nV/\sqrt{Hz}$
- DC voltage gain — 100,000
- AC voltage gain — 6000 at 10kHz
- Power bandwidth — 200kHz
- Slew rate — $13V/\mu S$
- Large supply voltage range — ±3V to ±20V

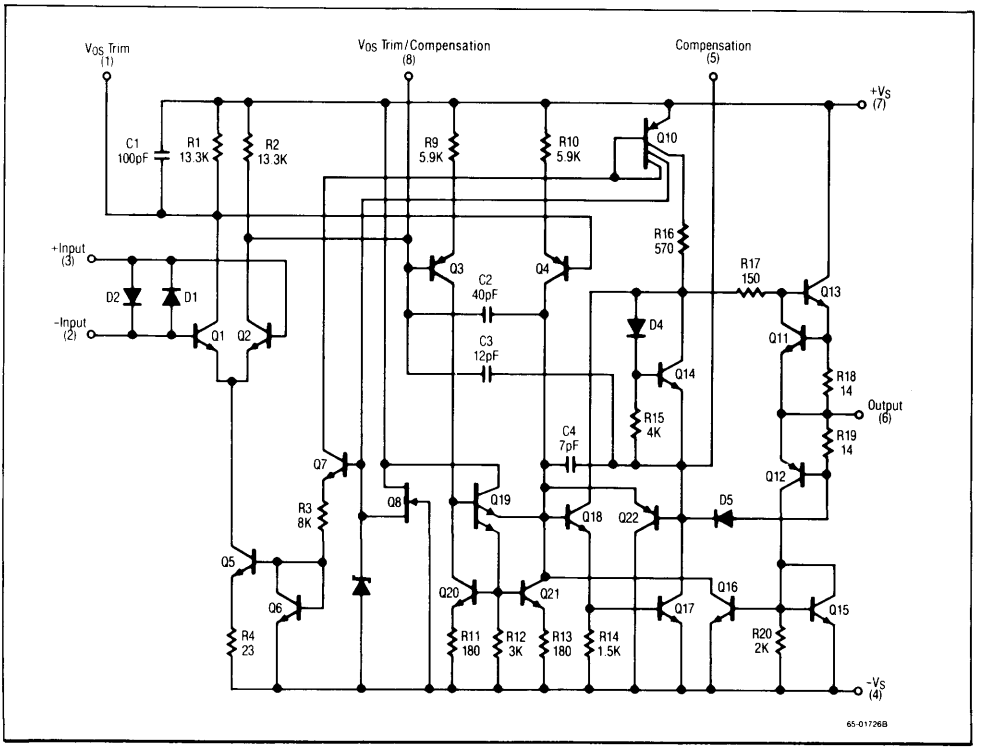
Description

The 5534 is a high performance, low noise operational amplifier. This amplifier features popular pin-out, superior noise performance, and high output drive capability.

This amplifier also features guaranteed noise performance with substantially higher gain-bandwidth product, power bandwidth, and slew rate which far exceeds that of the 741 type amplifiers. The 5534 is internally compensated for a gain of three or higher and may be externally compensated for optimizing specific performance requirements of various applications such as unity-gain voltage followers, drivers for capacitive loads or fast settling.

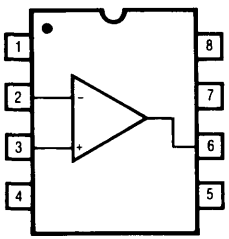
The specially designed low noise input transistors allow the 5534 to be used in very low noise signal processing applications such as audio preamplifiers and servo error amplifiers.

Schematic Diagram

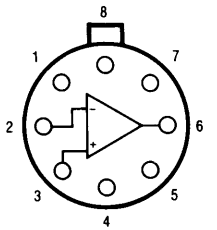


Connection Information

8-Lead
Ceramic DE and Plastic NB
Dual In-Line Package
(Top View)



8-Lead
TO-99
Metal Can
(Top View)



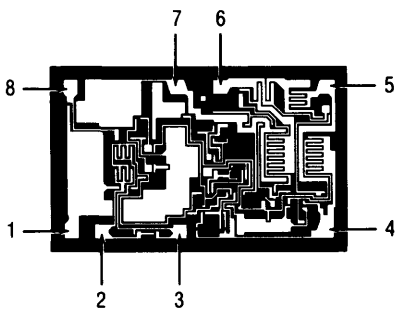
Pin	Function
1	V_{OS} Trim
2	-Input
3	+Input
4	$-V_S$
5	Compensation
6	Output
7	$+V_S$
8	V_{OS} Trim/Compensation

Absolute Maximum Ratings

Supply Voltage ..... ±22V
Differential Input Voltage 0.5V
Input Voltage ..... ±V Supply
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
RM5534/A ..... -55°C to ±125°C
RC5534/A ..... 0°C to +70°C
Lead Soldering Temperature
(10 Sec) ..... +300°C
Output Short Circuit Duration[1] ..... Indefinite

Notes: 1. Short circuit may be to ground only. Rating applies to +125°C case temperature or +75°C ambient temperature.

Mask Pattern



Die Size: 83 x 51 mils
Min. Pad Dimensions: 4 x 4 mils

Ordering Information

Part Number	Package	Operating Temperature Range
RC5534DE	Ceramic	0°C to +70°C
RC5534ADE	Ceramic	0°C to +70°C
RC5534NB	Plastic	0°C to +70°C
RC5534ANB	Plastic	0°C to +70°C
RC5534T	TO-99	0°C to +70°C
RC5534AT	TO-99	0°C to +70°C
RM5534DE	Ceramic	-55°C to +125°C
RM5534DE/883B*	Ceramic	-55°C to +125°C
RM5534ADE	Ceramic	-55°C to +125°C
RM5534ADE/883B*	Ceramic	-55°C to +125°C
RM5534T	TO-99	-55°C to +125°C
RM5534T/883B*	TO-99	-55°C to +125°C
RM5534AT	TO-99	-55°C to +125°C
RM5534AT/883B*	TO-99	-55°C to +125°C

*MIL-STD-883, Level B Processing

Thermal Characteristics

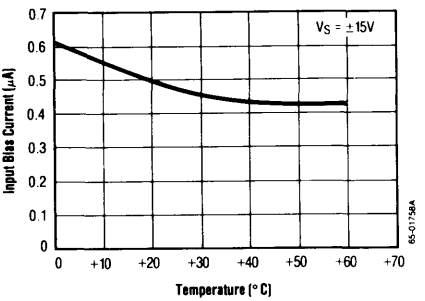
	8-Lead Plastic DIP	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can
Max. Junction Temp.	125°C	175°C	175°C
Max. P_D $T_A < 50°C$	468mW	833mW	658mW
Therm. Res. θ_{JC}	—	45°C/W	50°C/W
Therm. Res. θ_{JA}	160°C/W	150°C/W	190°C/W
For $T_A > 50°C$ Derate at	6.25mW per °C	8.33mW per °C	5.26mW per °C

Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise noted)

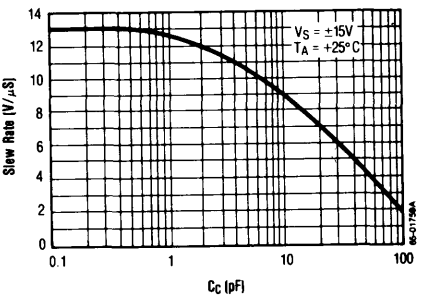
Parameters	Test Conditions	RM5534/A			RC5534/A			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 10k\Omega$		0.5	2.0		0.5	4.0	mV
Input Offset Current			10	200		20	300	nA
Input Bias Current			400	800		500	1500	nA
Input Resistance (Differential Mode)		50	100		30	100		kΩ
Large Signal Voltage Gain	$R_L \geq 600\Omega$, V_{OUT} = ±10V	50	100		25	100		V/mV
Output Voltage Swing	$R_L \geq 600\Omega$	±12	±13		±12	±13		V
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	80	100		70	100		dB
Power Supply Rejection Ratio	$R_S \leq 10k\Omega$	86	100		86	100		dB
Supply Current	$R_L = \infty$		4.0	6.5		4.0	8.0	mA
Transient Response Rise Time	V_{IN} = 50mV, R_L = 600Ω, C_L = 100pF, C_C = 22pF		35			35		nS
Overshoot			17			17		%
Slew Rate	$C_C = 0$		13			13		V/μS
Gain Bandwidth Product	C_C = 22pF, C_L = 100pF		10			10		MHz
Power Bandwidth	$V_O = 20V_{p-p}$, $C_C = 0$		200			200		kHz
Input Noise Voltage	f = 20Hz to 20kHz		1.0			1.0		μV_{RMS}
Input Noise Current	f = 20Hz to 20kHz		25			25		pA_{RMS}
Supply Current	V_S = ±15V, $R_L = \infty$			9.0			14	mA
Channel Separation	f = 1kHz, R_S = 5kΩ		110			110		dB
		5534A			5534			
Input Noise Voltage Density	f_O = 30Hz		5.5	7.0		7.0		nV/$\sqrt{Hz}$
	f_O = 1kHz		3.5	4.5		4.0		
Input Noise Current Density	f_O = 30Hz		1.5			2.5		pA/$\sqrt{Hz}$
	f_O = 1kHz		0.4			0.6		
Broadband Noise Figure	f = 10Hz – 20kHz, R_S = 5kΩ		0.9					dB
The following specifications apply for $-55°C \leq T_A \leq +125°C$ for RM; $0°C \leq T_A \leq +70°C$ for RC, V_S = ±15V								
		RM5534/A			RC5534/A			
Input Offset Voltage	$R_S \leq 10k\Omega$			3.0			5.0	mV
Input Offset Current				500			400	nA
Input Bias Current				1500			2000	nA
Large Signal Voltage Gain	$R_L \geq 600\Omega$, V_{OUT} = ±10V	25			15			V/mV
Output Voltage Swing	$R_L \geq 600\Omega$	±10			±10			V

Typical Performance Characteristics

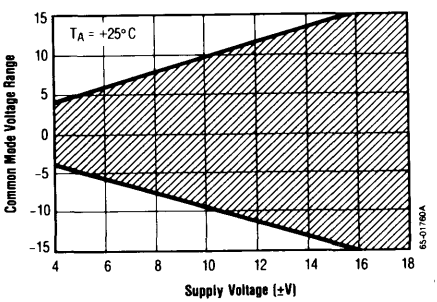
Input Bias Current vs. Temperature



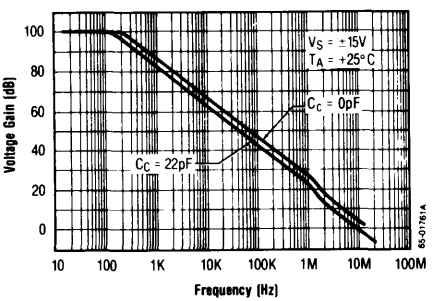
Slew Rate vs. Compensation Capacitor



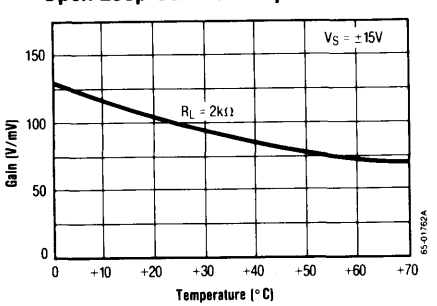
Common Mode Range as a Function of Supply Voltage



Open Loop Gain vs. Frequency

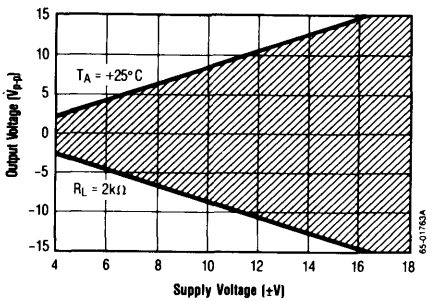


Open Loop Gain vs. Temperature

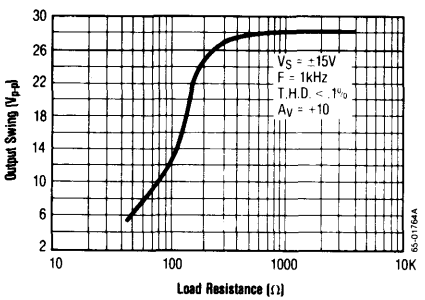


Typical Performance Characteristics (Continued)

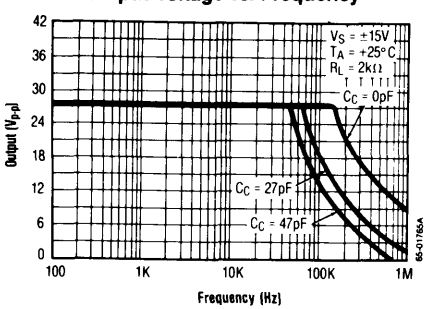
Typical Output Voltage as a Function of Supply Voltage



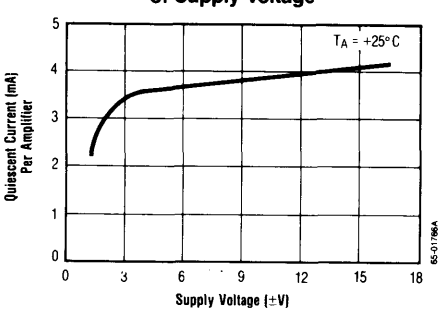
Output Voltage vs. Load Resistance



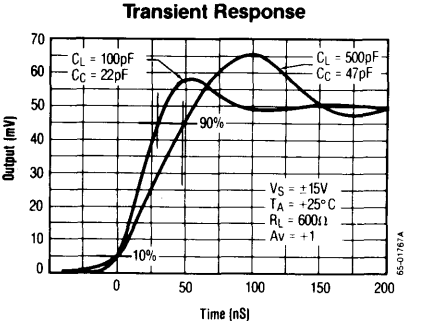
Output Voltage vs. Frequency



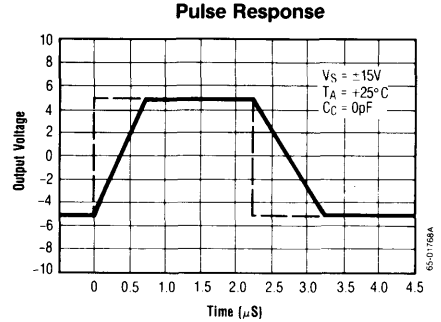
Quiescent Current as a Function of Supply Voltage



Transient Response

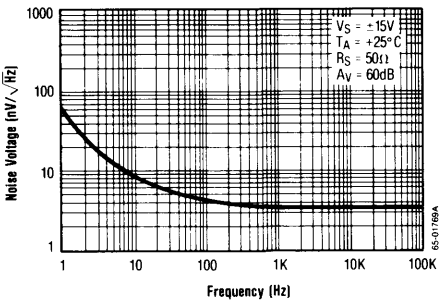


Voltage Follower Large Signal Pulse Response

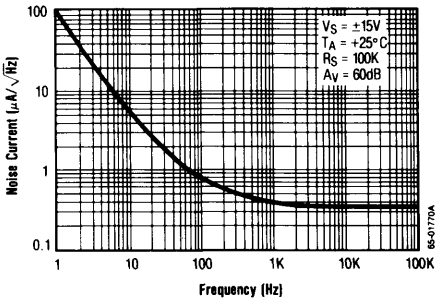


Typical Performance Characteristics (Continued)

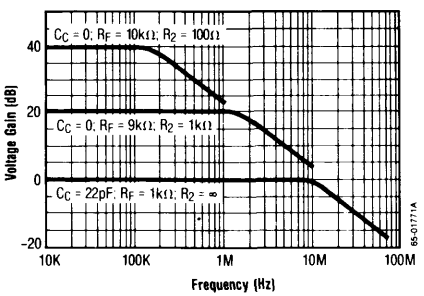
Input Noise Voltage as a Function of Frequency



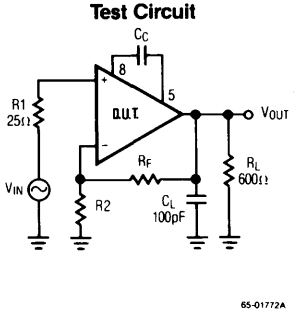
Input Noise Current as a Function of Frequency



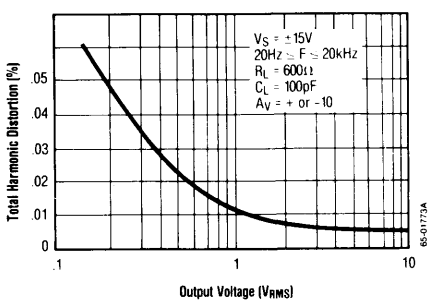
Closed Loop Frequency Response



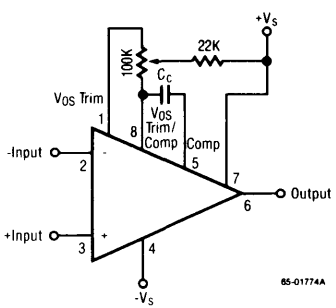
Test Circuit



Total Harmonic Distortion vs. Output Voltage



Offset Voltage Adjust Circuit



Section 7
Comparators

A voltage comparator is similar to an op amp in design, but lacks any AC compensation that would allow it to operate as a feedback amplifier. This lack of compensation capacitors gives a comparator the switching speed needed for fast comparisons of analog voltages. Another major difference is that most of Raytheon's comparators have an open collector output, which requires an external pull up resistor, while op amps have a push pull output stage. The exception is the RC4805 high speed precision comparator, which includes a push pull output stage.

Raytheon's part types include low input current single and dual comparators, dual and quad single supply types, and the RC4805 zener zap trimmed 22nS comparator. The LM111, LH2111, and LM139 are available in JAN 38510 grades.

DEFINITIONS

Average Input Offset Voltage Drift (TC_{VOS})
The ratio of change in input offset voltage to a change in ambient temperature, expressed in microvolts per degree C ($\mu V/^\circ C$).

$$TC_{VOS} = \frac{V_{OS} @ T_{(1)} - V_{OS} @ T_{(2)}}{T_{(1)} - T_{(2)}}$$

Where $T_{(1)}$ and $T_{(2)}$ are the upper and lower limits of the specified temperature range.

Common Mode Rejection Ratio (CMRR)
The ratio of change of input common mode voltage (both inputs swing together over a specified voltage range) to a change in input offset voltage, expressed in decibels (dB).

$$CMRR = 20LOG_{10}\left(\frac{V_{IN(1)} - V_{IN(2)}}{V_{OS} @ V_{IN(1)} - V_{OS} @ V_{IN(2)}}\right)$$

Where $V_{IN(1)}$ and $V_{IN(2)}$ are the upper and lower limits of the input common mode voltage range.

Input Bias Current (I_B)
The average of the two input currents with the output voltage at the center of its swing with no load, expressed in nanoamps (nA).

Input Offset Current (I_{OS})
The difference between the two input currents with the output voltage at the center of its swing with no load, expressed in nanoamps (nA).

Input Offset Voltage (V_{OS})
The voltage that must be applied between the two inputs to obtain an output voltage in the center of the output swing range, expressed in millivolts or microvolts (mV or μV).

Input Voltage Range
The range of voltages at the inputs over which the comparator operates within its common mode rejection ratio specification, expressed in volts (V).

Large Signal Voltage Gain (A_V)
The ratio of a specified output voltage change to the change in input offset voltage required to effect the change under open loop conditions, expressed in volts per millivolt (V/mV).

$$A_V = \frac{V_{O(1)} - V_{O(2)}}{V_{OS(1)} - V_{OS(2)}}$$

Where $V_{O(1)}$ and $V_{O(2)}$ are the specified upper and lower voltage limits for the change at the output.

Output Leakage Current
For open collector output types; the collector to emitter leakage current of the output transistor with the output in an off condition and a specified voltage applied, expressed in microamps (μA).

Output Sink Current
The current flowing into the output for a specified set of input and output conditions, measured in milliamps (mA).

Output Source Current
The current flowing out of the output for a specified set of input and output conditions, measured in milliamps (mA).

Output Voltage Swing
The peak output change, referred to ground, that can be obtained for a specified load resistance, expressed in volts (V).

Power Consumption
The DC power required to operate the comparator with the output at the center of its swing and zero load current, expressed in milliwatts (mW).

Power Supply Rejection Ratio (PSRR)
The ratio of change of supply voltage to a change in input offset voltage, expressed in decibels (dB).

$$PSRR = 20LOG_{10}\left(\frac{V_{S(1)} - V_{S(2)}}{V_{OS} @ V_{S(1)} - V_{OS} @ V_{S(2)}}\right)$$

Where $V_{S(10}$ and $V_{S(2)}$ are the upper and lower limits of the specified change of supply voltage.

Propagation Delay
The time delay between a step input to a resulting change at the output, from the 50% point of the input step to the 50% point of the output swing, measured in nanoseconds (nS).

DEFINITIONS (Continued)

Saturation Voltage (V_{SAT})
Voltage at the output when sinking a specified amount of current into the output, expressed in volts (V).

Supply Current (I_S)
The current required from the power supply to operate the comparator under quiescent no load conditions, expressed in milliamps (mA).

Supply Voltage (V_S)
The range of power supply voltages over which the comparator will operate, expressed in volts (V).

Raytheon

Single-Supply Quad Comparators

LM139/139A, 239/239A, 339/339A, 2901 RC3302

Features

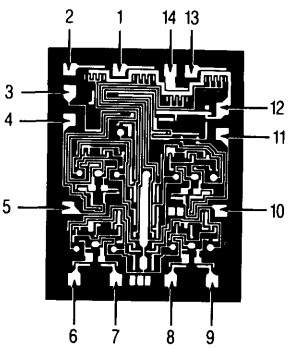
- Input common mode voltage range includes ground
- Wide single supply voltage range — 2V to 36V
- Output compatible with TTL, DTL, ECL, MOS and CMOS logic systems
- Very low supply current drain (0.8mA) independent of supply voltage

Description

These devices offer higher frequency operation and faster switching than can be had from internally compensated quad op amps. Intended for single-supply applications, the Darlington PNP input stage allows them to compare voltages that include ground. The two-stage common-emitter output circuit provides gain and output sink capacity of 3.2mA at an output level of 400mV. The output collector is left open, permitting the designer to drive devices in the range of 2V to 36V.

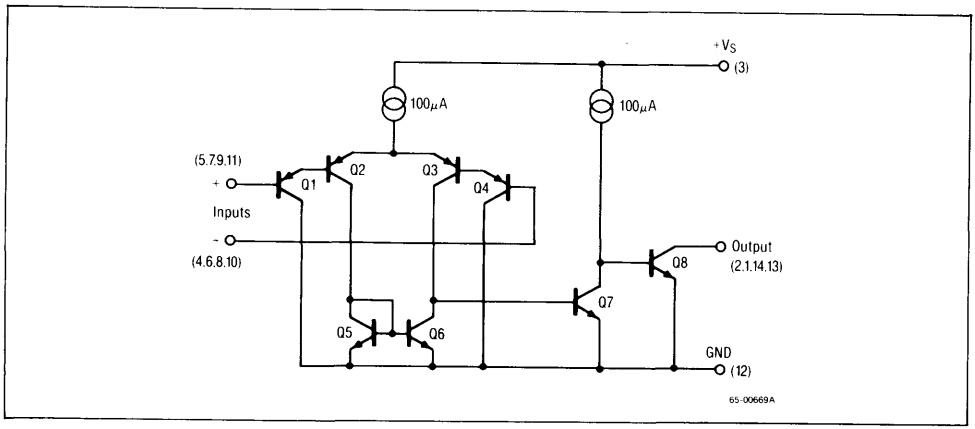
They are intended for applications not needing response time less than 1μS, but demanding excellent op amp input parameters of offset voltage, current, and bias current, to ensure accurate comparison with a reference voltage.

Mask Pattern



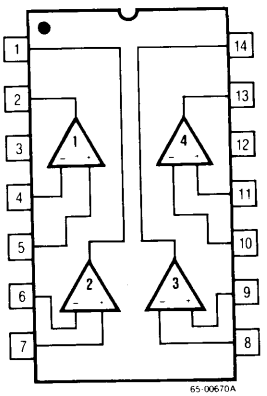
Die Size: 59 x 77 mils
Min. Pad Dimensions: 4 x 4 mils

Schematic Diagram (1/4 Shown)



Connection Information

14-Lead
Dual In-Line Package
(Top View)



Pin	Function
1	Output 2
2	Output 1
3	$+V_S$
4	-Input 1
5	+Input 1
6	-Input 2
7	+Input 2
8	-Input 3
9	+Input 3
10	-Input 4
11	+Input 4
12	Ground
13	Output 4
14	Output 3

Thermal Characteristics

	14-Lead Micro-Pak Plastic DIP	14-Lead Plastic DIP	14-Lead Ceramic DIP
Max. Junction Temp.	125°C	125°C	175°C
Max. P_D $T_A < 50°C$	300mW	468mW	1042mW
Therm. Res. θ_{JC}	—	—	60°C/W
Therm. Res. θ_{JA}	200°C/W	160°C/W	120°C/W
For $T_A > 50°C$ Derate at	5.0mW per °C	6.25mW per °C	8.38mW per °C

Absolute Maximum Ratings

Supply Voltage, $+V_S$ ..... +36 or ±18V
RC3302 ..... +28V or ±14V
Differential Input Voltage ..... +36V
RC3302 ..... +28V
Input Voltage ..... -0.3V to +36V
RC3302 ..... -0.3V to +28V
Output Short Circuit
to Ground[1] ..... Continuous
Input Current ($V_{IN} < -0.3V$)[2] 50mA
Operating Temperature Range
LM139 ..... -55°C to +125°C
LM239 ..... -25°C to +85°C
LM339 ..... 0°C to +70°C
LM2901/RC3302 ..... -40°C to +85°C
Storage Temperature Range
Standard Packages ..... -65°C to +150°C
Micro-Pak (LM only) ..... -40°C to +125°C
Lead Soldering Temperature (10 Sec)
Standard Packages ..... +300°C
Micro-Pak (LM only) ..... +260°C

Ordering Information

Part Number	Package	Operating Temperature Range
LM339J	Ceramic	0°C to +70°C
LM339M	Micro-Pak	0°C to +70°C
LM339N	Plastic	0°C to +70°C
LM339AJ	Ceramic	0°C to +70°C
LM339AM	Micro-Pak	0°C to +70°C
LM339AN	Plastic	0°C to +70°C
LM239J	Ceramic	-25°C to +85°C
LM239N	Plastic	-25°C to +85°C
LM239AJ	Ceramic	-25°C to +85°C
LM239AN	Plastic	-25°C to +85°C
LM2901N	Plastic	-40°C to +85°C
RC3302DB	Plastic	-40°C to +85°C
LM139J	Ceramic	-55°C to +125°C
LM139J/883B*	Ceramic	-55°C to +125°C
LM139AJ	Ceramic	-55°C to +125°C
LM139A/883B*	Ceramic	-55°C to +125°C

*MIL-STD-883, Level B Processing

Electrical Characteristics ($+V_S = +5V$[3])

Parameters	Test Conditions	LM139A			LM239A, 339A			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = +25°C$ [8]		±1.0	±2.0		±1.0	±2.0	mV
Input Bias Current	Output in Linear Range $T_A = +25°C$ [4]		25	100		25	250	nA
Input Offset Current	$T_A = +25°C$		±3.0	±25		±5.0	±50	nA
Input Voltage Range	$T_A = +25°C$ [5]	0		$+V_S$ −1.5	0		$+V_S$ −1.5	V
Supply Current	$R_L = \infty$ on all Comparators, $T_A = +25°C$		0.8	2.0		0.8	2.0	mA
Large Signal Voltage Gain	$R_L \geq 15k\Omega$, $+V_S = +15V$ (To Support Large V_O Swing), $T_A = +25°C$	50	200		50	200		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, $V_{REF} = 1.4V$, $V_{RL} = 5V$, $R_L = 5.1k\Omega$, $T_A = +25°C$		300			300		nS
Response Time	$V_{RL} = 5V$, $R_L = 5.1k\Omega$, $T_A = +25°C$ [6]		1.3			1.3		μS
Output Sink Current	$V_{IN-} \geq 1V$, $V_{IN+} = 0$, $V_O \leq 1.5V$, $T_A = +25°C$	6.0	16		6.0	16		mA
Saturation Voltage	$V_{IN-} \geq 1V$, $V_{IN+} = 0$, $I_{SINK} \leq 4mA$, $T_A = +25°C$		250	400		250	400	mV
Output Leakage Current	$V_{IN+} \geq 1V$, $V_{IN-} = 0$, $V_O = 5V$, $T_A = +25°C$		0.1			0.1		μA
Input Offset Voltage	Note 8			±4.0			±4.0	mV
Input Offset Current				±100			±150	nA
Input Bias Current	Output in Linear Range			300			400	nA
Input Voltage Range		0		$+V_S$ −2.0	0		$+V_S$ −2.0	V
Saturation Voltage	$V_{IN-} \geq 1V$, $V_{IN+} = 0$, $I_{SINK} \leq 4mA$			700			700	mV
Output Leakage Current	$V_{IN+} \geq 1V$, $V_{IN-} = 0$, $V_O = 30V$			1.0			1.0	μA
Differential Input Voltage	Keep all V_{IN}s $\geq 0V$ (or $-V_S$, if used)[7]			36			36	V

Electrical Characteristics (Continued)

Parameters	Test Conditions	LM139			LM239, 339			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	T_A = +25°C [8]		±2.0	±5.0		±2.0	±5.0	mV
Input Bias Current	Output in Linear Range, T_A = +25°C [4]		25	100		25	250	nA
Input Offset Current	T_A = +25°C		±3.0	±25		±5.0	±50	nA
Input Voltage Range	T_A = +25°C [5]	0		$+V_S$ −1.5	0		$+V_S$ −1.5	V
Supply Current	R_L = ∞ on all Comparators, T_A = +25°C		0.8	2.0		0.8	2.0	mA
Large Signal Voltage Gain	$R_L \geq 15k\Omega$, $+V_S$ = 15V (To Support Large V_O Swing), T_A = +25°C		200			200		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{REF} = +1.4V, V_{RL} = +5V, R_L = 5.1kΩ, T_A = +25°C		300			300		nS
Response Time	V_{RL} = 5V, R_L = 5.1kΩ, T_A = +25°C [6]		1.3			1.3		μS
Output Sink Current	$V_{IN-} \geq 1V$, V_{IN+} = 0, $V_O \leq 1.5V$, T_A = +25°C	6.0	16		6.0	16		mA
Output Voltage V_{OL}	$V_{IN-} \geq 1V$, V_{IN+} = 0, $I_{SINK} \leq 4mA$, T_A = +25°C		250	400		250	400	mV
Output Leakage Current	$V_{IN+} \geq 1V$, V_{IN-} = 0, V_O = +5V, T_A = +25°C		0.1			0.1		μA
Input Offset Voltage	Note 8			±9.0			±9.0	mV
Input Offset Current				±100			±150	nA
Input Bias Current	Output in Linear Range			300			400	nA
Input Voltage Range		0		$+V_S$ −2.0	0		$+V_S$ −2.0	V
Output Voltage V_{OL}	$V_{IN-} \geq 1V$, V_{IN+} = 0, $I_{SINK} \leq 4mA$			700			700	mV
Output Leakage Current	$V_{IN+} \geq 1V$, V_{IN-} = 0, V_O = 30V			1.0			1.0	μA
Differential Input Voltage	Keep all V_{IN}s ≥ 0V (or $-V_S$, if used)[7]			36			36	V

Electrical Characteristics (Continued)

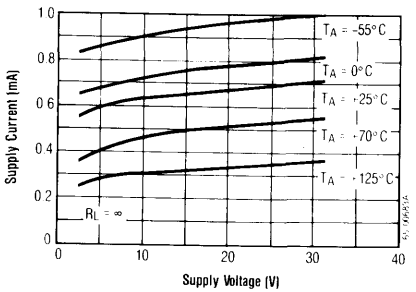
Parameters	Test Conditions	LM2901			RC3302			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	T_A = +25°C [8]		±2.0	±7.0		±3.0	±20	mV
Input Bias Current	Output in Linear Range, T_A = +25°C [4]		25	250		25	500	nA
Input Offset Current	T_A = +25°C		±5.0	±50		±3.0	±100	nA
Input Voltage Range	T_A = +25°C [5]	0		$+V_S$ −1.5	0		$+V_S$ −1.5	V
Supply Current	R_L = ∞ on all Comparators, T_A = +25°C		0.8	2.0		0.8	2.0	mA
	R_L = ∞, $+V_S$ = 30V, T_A = +25°C		1.0	2.5				mA
Large Signal Voltage Gain	$R_L \geq 15k\Omega$, $+V_S$ = 15V (To Support Large V_O Swing), T_A = +25°C	25	100		2.0	30		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{REF} = +1.4V, V_{RL} = +5V, R_L = 5.1kΩ, T_A = +25°C		300			300		nS
Response Time	V_{RL} = 5V, R_L = 5.1kΩ, T_A = +25°C [6]		1.3			1.3		μS
Output Sink Current	$V_{IN-} \geq 1V$, V_{IN+} = 0, $V_O \leq 1.5V$, T_A = +25°C	6.0	16		2.0	16		mA
Output Voltage V_{OL}	$V_{IN-} \geq 1V$, V_{IN+} = 0, $I_{SINK} \leq 4mA$, T_A = +25°C			400		250	500	mV
Output Leakage Current	$V_{IN+} \geq 1V$, V_{IN-} = 0, V_O = 5V, T_A = +25°C		0.1			0.1		μA
Input Offset Voltage	Note 8		±9.0	±15			±40	mV
Input Offset Current			50	200			300	nA
Input Bias Current	Output in Linear Range		200	500			1000	nA
Input Voltage Range		0		$+V_S$ −2.0	0		$+V_S$ −2.0	V
Output Voltage V_{OL}	$V_{IN-} \geq 1V$, V_{IN+} = 0, $I_{SINK} \leq 4mA$		400	700			700	mV
Output Leakage Current	$V_{IN+} \geq 1V$, V_{IN-} = 0, V_O = 30V			1.0			1.0	μA
Differential Input Voltage	Keep all V_{IN}s ≥ 0V (or $-V_S$, if used)[7]	0		$+V_S$			$+V_S$	V

Electrical Characteristics (Continued)

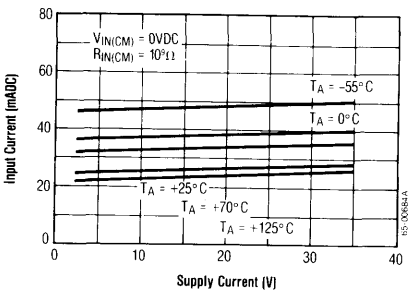
Notes:
1. Short circuits from the output to $+V_S$ can cause excessive heating and eventual destruction. The maximum output current is approximately 20mA independent of the magnitude of $+V_S$.
2. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltage of the comparators to go to the $+V_S$ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3V.
3. These specifications apply for $+V_S$ = 5V and $-55°C \leq T_A \leq +125°C$, unless otherwise stated. With the LM239 all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$, the LM339 temperature specifications are limited to $0°C \leq T_A \leq +70°C$, and the LM2901, RC3302 temperature range is $-40°C \leq T_A \leq +85°C$.
4. The direction of the input current is out of the IC due to the PNP input state. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
5. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common mode voltage range is $+V_S$ -1.5V, but either or both inputs can go to +30V without damage.
6. The response time specified is for a 100mV input step with 5mV overdrive. For larger overdrive signals 300nS can be obtained. See Typical Performance Characteristics section.
7. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common mode range, the comparator will provide a proper output state. The low input voltage state must not be less than -0.3V (or 0.3V below the magnitude of the negative power supply, if used).
8. At output switch point, $V_O \cong 1.4V$, $R_S = 0\Omega$ with $+V_S$ from 5V; and over the full input common mode range (0V to $+V_S$ -1.5V).
9. For input signals that exceed $+V_S$, only the overdriven comparator is affected. With a 5V supply, V_{IN} should be limited to 25V max, and a limiting resistor should be used on all inputs that might exceed the positive supply.

Typical Performance Characteristics LM139/139A, 239/239A, 339/339A, RC3302

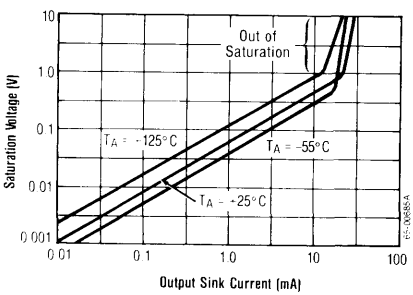
Supply Current



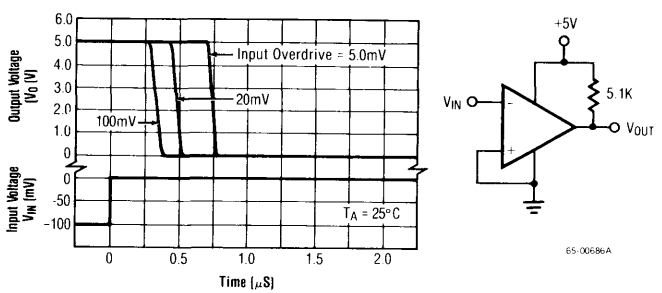
Input Current



Output Saturation Voltage

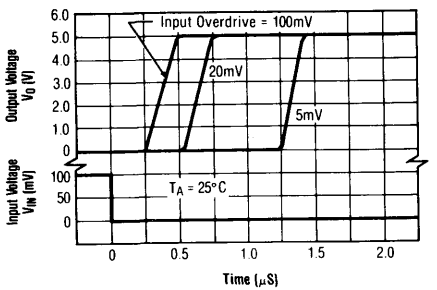


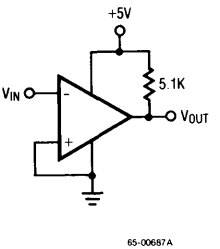
Response Time for Various Input Overdrives Negative Transition



Typical Performance Characteristics (Continued) LM139/139A, 239/239A, 339/339A, RC3302

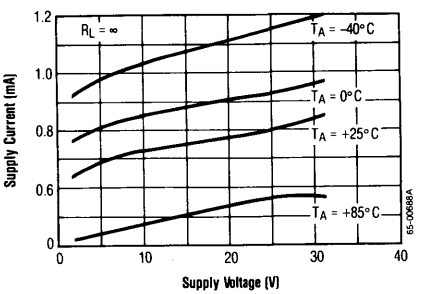
Response Time for Various Input Overdrive Positive Transition



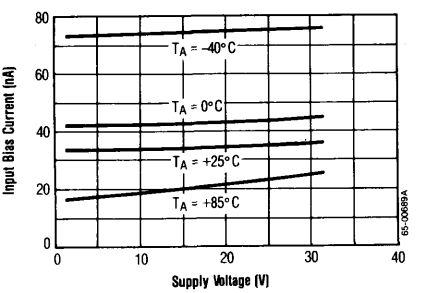


Typical Performance Characteristics LM2901

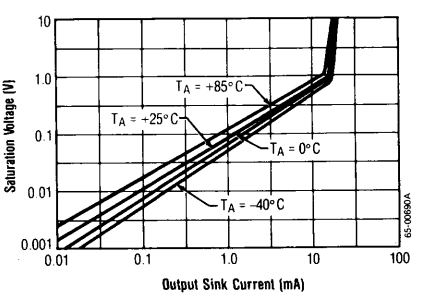
Supply Current



Input Current

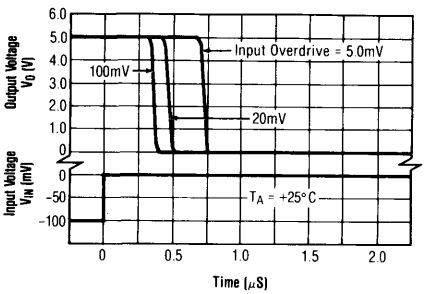


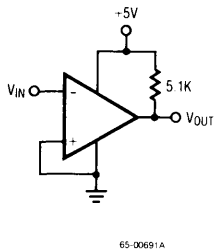
Output Saturation Voltage



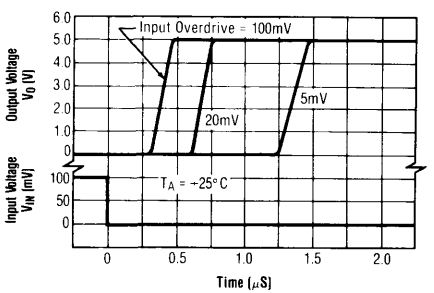
Typical Performance Characteristics (Continued) LM2901

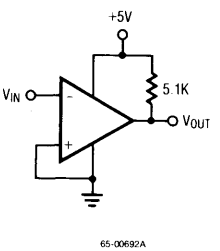
Response Time for Various Input Overdrives Negative Transition





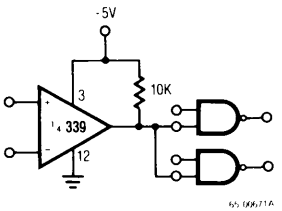
Response Time for Various Input Overdrives Positive Transition



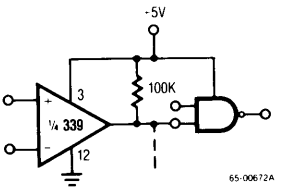


Typical Applications — Single Supply ($+V_S$ = +15V)

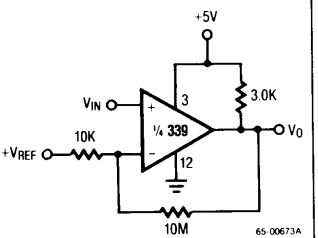
Driving TTL



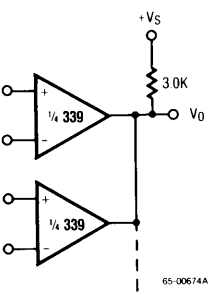
Driving CMOS



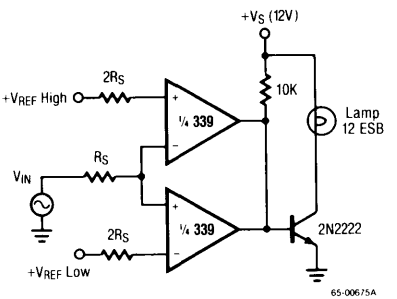
Comparator With Hysteresis



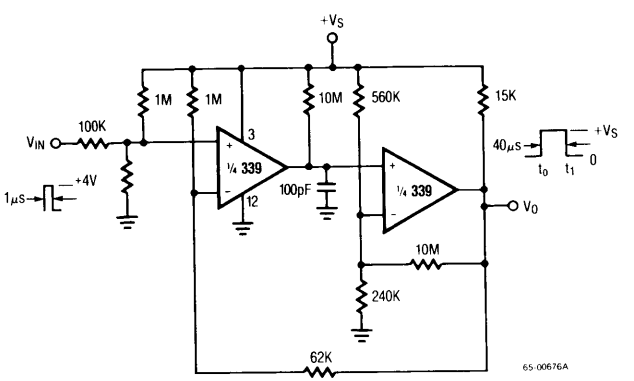
ORing the Output



Limit Comparator

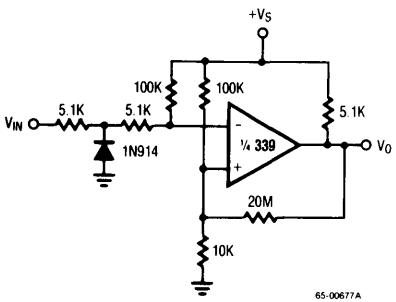


One-Shot Multivibrator With Input Lock Out

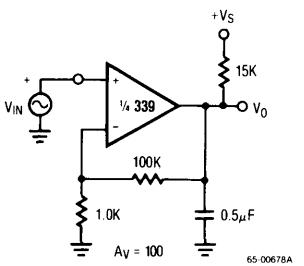


Typical Applications — Single Supply (Continued)

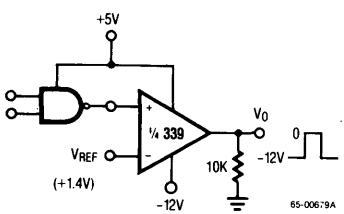
Zero Crossing Detector (Single Power Supply)



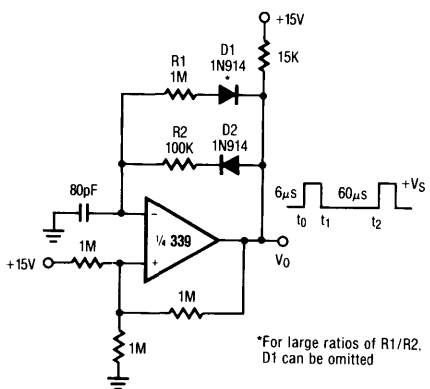
Low Frequency Op Amp



TTL to MOS Logic Converter

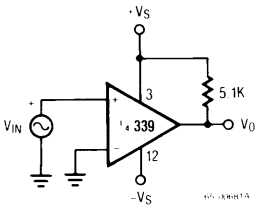


Pulse Generator

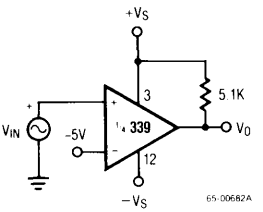


Typical Applications — Split Supply ($+V_S$ = +15V and $-V_S$ = -15V)

Zero Crossing Detector



Comparator With a Negative Reference



Raytheon

Low Power, Low Offset Voltage Dual Comparator

LM393/ RC2403

Features

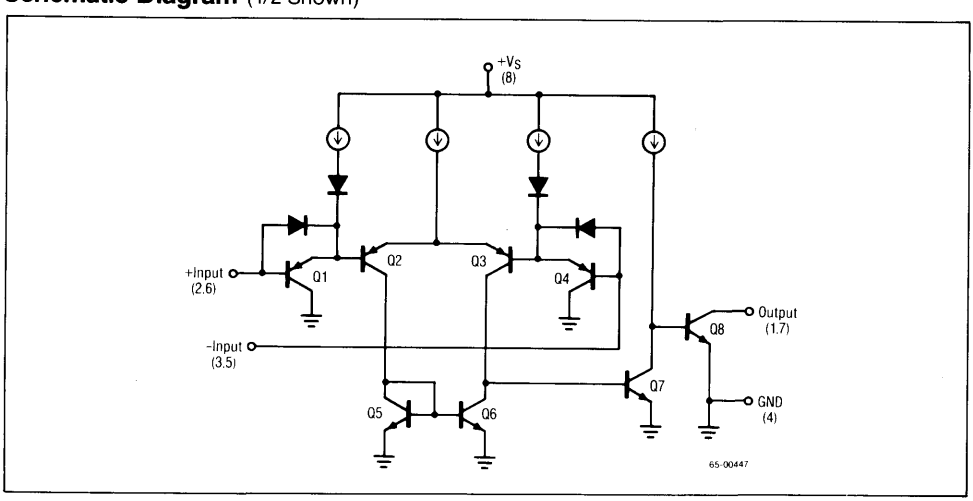
- Wide single supply voltage range — 2.0V to 36V or dual supplies — ±1.0V to ±18V
- Very low supply current drain (0.8mA) independent of supply voltage (1.0mW/comparator at 5.0V)
- Low input bias current — 25nA
- Low input offset current — ±5.0nA and maximum offset voltage — ±3.0mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage
  LM393 — 250mV at 3mA
  RC2403 — 400mV at 15mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems
- Reduced V_{OS} drift over temperature
- Eliminates need for dual supplies
- Allows sensing near ground
- Compatible with all forms of logic
- Power drain suitable for battery operation

Description

The LM393 consists of two independent precision voltage comparators with an offset voltage specification as low as 5.0mV max for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. The LM393 has a unique characteristic: the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog-to-digital converters; pulse, square-wave and time delay generators; wide range V_{CO}; MOS clock timers; multivibrators and high voltage digital logic gates. The LM393 was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM393 will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

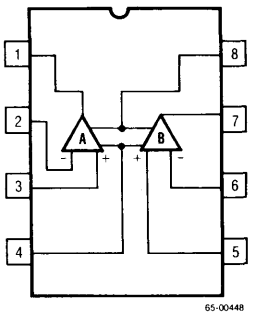
Schematic Diagram (1/2 Shown)



Low Power, Low Offset Voltage Dual Comparator

Connection Diagram

Dual In-Line Package
(Top View)

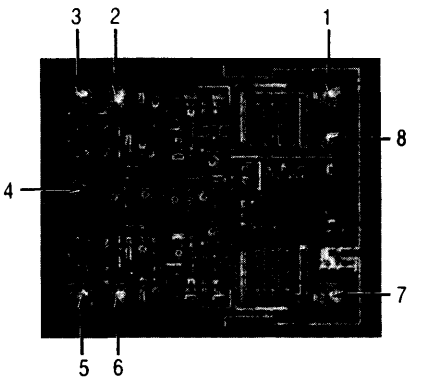


Pin	Function
1	Output A
2	Inverting Input A
3	Non-Inverting Input A
4	GND
5	Non-Inverting Input B
6	Inverting Input B
7	Output B
8	$+V_S$

Absolute Maximum Ratings

Supply Voltage, $+V_S$ ..... +36V or ±18V
Differential Input Voltage 36V
Input Voltage ..... -0.3V to +36V
Output Short Circuit to Ground[2] .. Continuous
Input Current 50mA
Operating Temperature
Range ..... 0°C to +70°C
Lead Soldering Temperature (10 Sec)
LM393NB ..... +300°C
LM393M ..... +260°C

Mask Pattern



Die Size: 52 x 61 mils
Min. Pad Dimensions: 4 x 4 mils

Thermal Characteristics

	8-Lead Micro-Pak Plastic DIP	8-Lead Plastic DIP
Max. Junction Temp.	125°C	125°C
Max. P_D $T_A < 50°C$	300mW	468mW
Therm. Res. θ_{JC}	—	—
Therm. Res. θ_{JA}	240°C/W	160°C/W
For $T_A > 50°C$ Derate at	4.17mW per °C	6.25mW per °C

Ordering Information

Part Number	Package	Operating Temperature Range
LM393NB	Plastic	0°C to +70°C
LM393M	Micro-Plastic	0°C to +70°C
RC2403NB	Plastic	0°C to +70°C
RC2403M	Micro-Plastic	0°C to +70°C

Electrical Characteristics ($+V_S$ = +5V; T_A = +25° C)

Parameters	Test Conditions	LM393			RC2403			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[7]			2.0	5.0		2.0	10	mV
Input Bias Current[3]	Output in Linear Range		25	250		50	500	nA
Input Offset Current			5.0	50		10	100	nA
Input Voltage Range[4]		0		$+V_S$ -1.5	0	$+V_S$	-1.5	V
Supply Current	R_L = ∞ on all Comparators		0.8	10		0.8	1.5	mA
Large Signal Voltage Gain	$R_L \geq 15k\Omega$, V_S = +15V (To Support Large V_O Swing)	50	200		50	200		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{REF} = +1.4V V_{RL} = +5.0V, R_L = 5.1kΩ		300			300		nS
Response Time[5]	V_{RL} = +5.0V, R_L = 5.1kΩ		1.3			1.5		μS
Output Sink Current	$V_{IN-} \geq +1.0V$, V_{IN+} = 0, $V_O \leq +1.5V$	6.0	16		20	40		mA
Output Saturation Voltage	$V_{IN-} \geq +1.0V$, V_{IN+} = 0, $I_{SINK} \leq 3.0mA$		250	400				mV
	$I_{SINK} \leq 15mA$					250	400	mV
Output Leakage Current	V_{IN} = 0, $V_{IN+} \geq +1.0V$, V_O = +5.0V		0.1			0.1		μA
The following specifications apply for V_S = +5V, 0°C ≤ T_A ≤ +70°C								
Input Offset Voltage[7]			3.0	9.0		3.0	12	mV
Input Offset Current			50	150		50	150	nA
Input Bias Current	Output in Linear Range		200	400		200	650	nA
Input Voltage Range		0		$+V_S$ -2.0	0		$+V_S$ -2.0	V
Output Saturation Voltage	$V_{IN-} \geq +1.0V$, V_{IN+} = 0, $I_{SINK} \leq 3.0mA$		400	700				mV
	$I_{SINK} \leq 15mA$					400	700	mV
Output Leakage Current	V_{IN-} = 0, $V_{IN+} \geq +1.0V$, V_O = +30V			1.0			1.0	μA
Supply Current	R_L = ∞ on all Amps, V_S = +30V		1.0	2.5		1.0	3.0	mA

Notes: 1. Short circuits from the output to $+V_S$ can cause excessive heating and eventual destruction. The maximum output current is approximately 20mA independent of the magnitude of $+V_S$.
2. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to

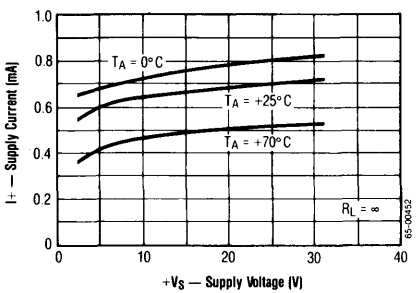
Electrical Characteristics (Continued)

this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the $+V_S$ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3V.

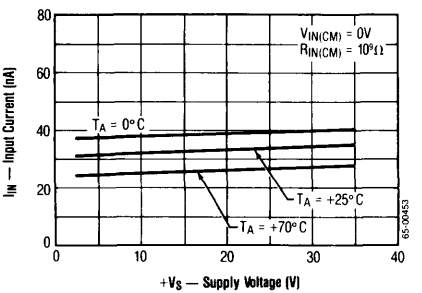
3. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
4. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common mode voltage range is $+V_S$ -1.5V, but either or both inputs can go to 30V without damage.
5. The response time specified is for a 100mV input step with 5.0mV overdrive. For larger overdrive signals 300nS can be obtained, see Typical Performance Characteristics section.
6. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common mode range, the comparator will provide a proper output state. The low input voltage state must not be less than -0.3V (or 0.3V below the magnitude of the negative power supply, if used).
7. At output switch point, $V_O \cong 1.4V$, $R_S = 0\Omega$ with $+V_S$ from +5.0V to +30V; and over the full input common mode range (0V to $+V_S$ -1.5V).
8. For input signals that exceed $+V_S$, only the overdriven comparator is affected. With a +5.0V supply, V_{IN} should be limited to 25V max, and a limiting resistor should be used on all inputs that might exceed the positive supply.

Typical Performance Characteristics

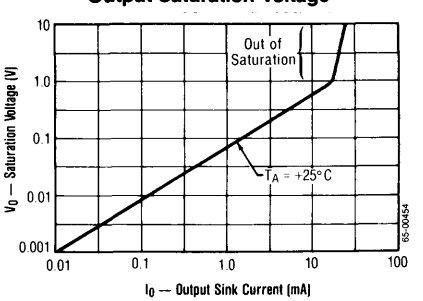
Supply Current



Input Current

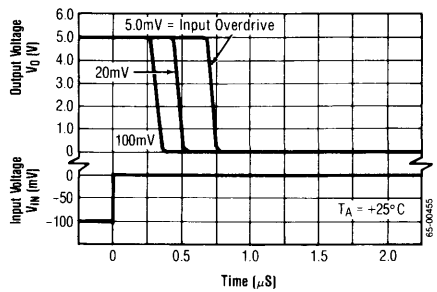


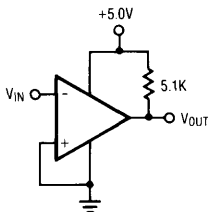
Output Saturation Voltage



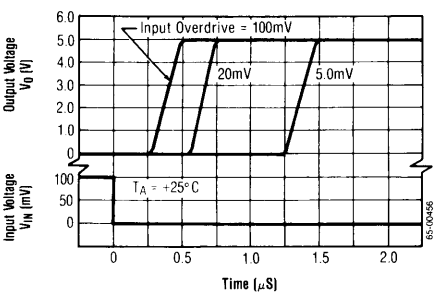
Typical Performance Characteristics (Continued)

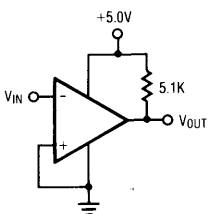
Response Time for Various Input Overdrives — Negative Transition





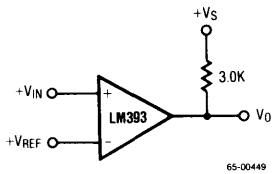
Response Time for Various Input Overdrives — Positive Transition



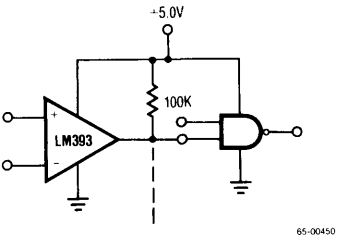


Typical Applications (V_S = +5.0V)

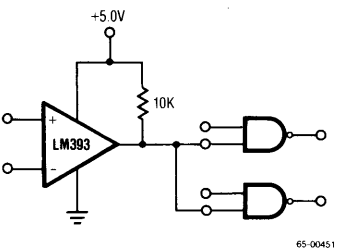
Basic Comparator



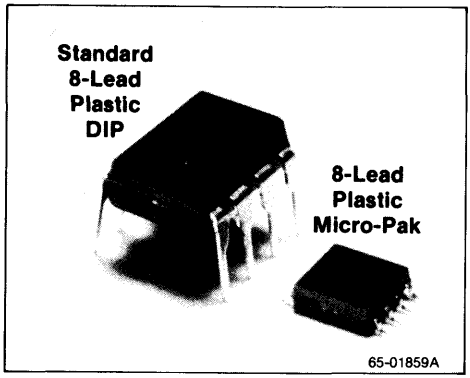
Driving CMOS



Driving TTL



Comparison of Standard
vs Micro-Package



Raytheon

Precision High Speed Latching Comparator

RC4805

Features

- 22nS propagation delay
- Low offset voltage — 100μV
- Low offset current — 15nA
- TTL compatible latch
- TTL output

Description

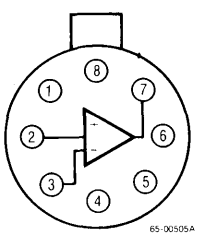
The RC/RM4805 is the ideal comparator for high speed, high precision applications. The input errors are factory trimmed to less than 1/10 LSB of a 12-bit, 10V system. The latch function allows the system designer additional flexibility. When the latch input is a TTL low, the comparator functions normally. When the input is raised to a TTL high, the comparator output is latched in its current state. The latch functions over the full military temperature range.

The 4805 is ideal for ultra precise, very fast system designs. Typical applications include successive approximation A/D converters of 12 or more bits, zero crossing detectors, high speed sampling, or window detectors.

The 4805 high speed comparator is functionally equivalent to the popular comparators HA-4950, AM686, SE527, CMP-05 and μA760. Propagation delay is 35nS with a 1/2 LSB overdrive in a 12-bit, 10V system.

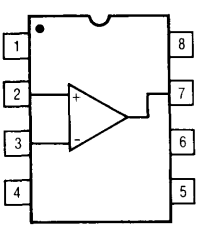
Connection Information

TO-99
Metal Can
(Top View)



65-00505A

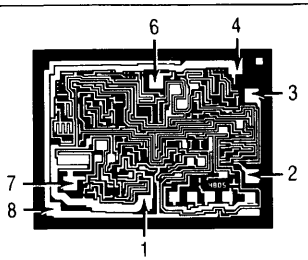
8-Lead
Ceramic Dual In-Line Package
(Top View)



65-00506A

Pin	Function
1	Ground
2	Non-Inverting Input
3	Inverting Input
4	$-V_S$
5	NC
6	Latch Enable
7	V_{OUT}
8	$+V_S$

Mask Pattern

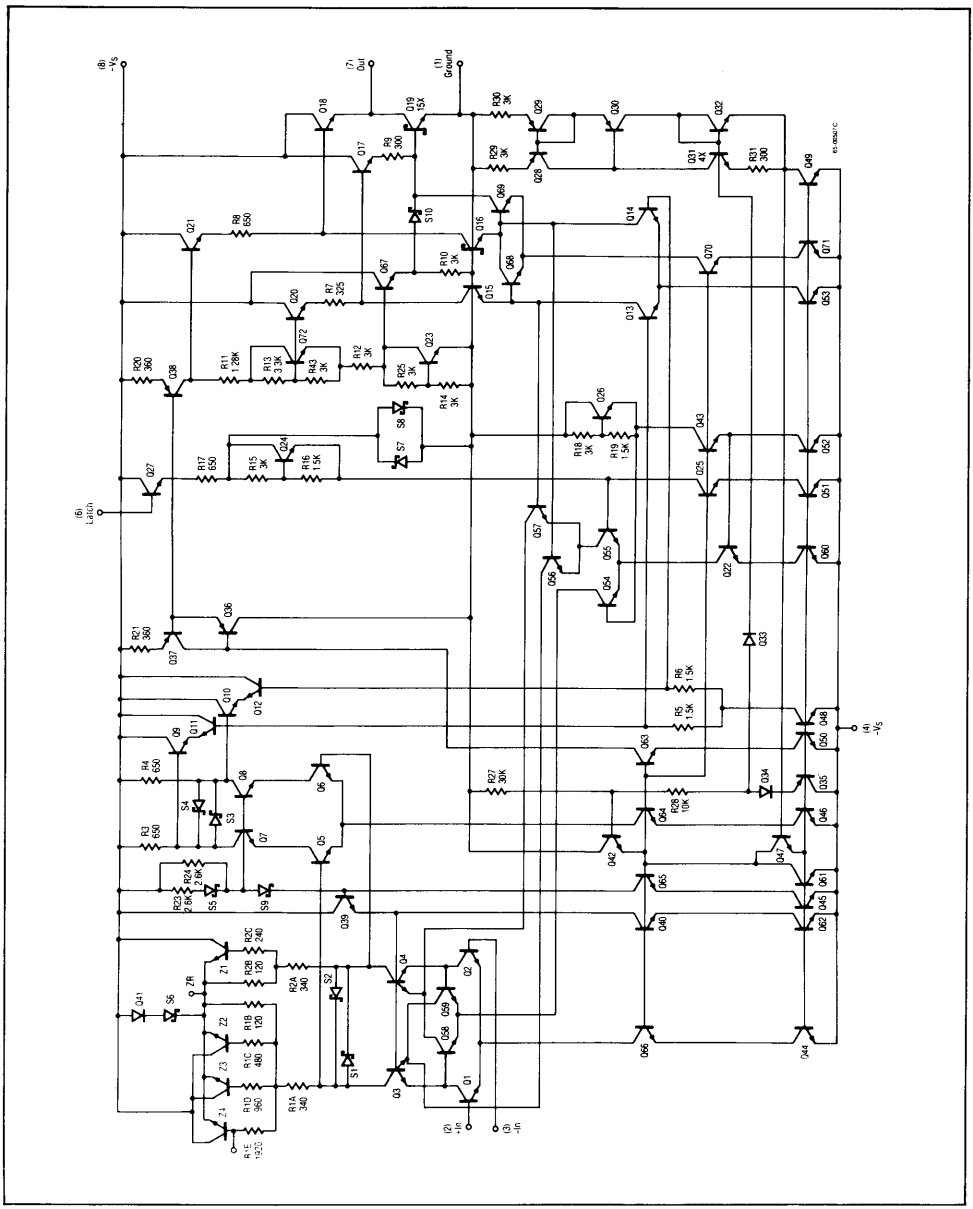


Die Size: 51 x 67 mils
Min. Pad Dimensions: 4 x 4 mils

Thermal Characteristics

	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can
Max. Junction Temp.	175°C	175°C
Max. P_D T_A < 50°C	833mW	658mW
Therm. Res. θ_{JC}	45°C/W	50°C/W
Therm. Res. θ_{JA}	150°C/W	190°C/W
For T_A > 50°C Derate at	8.33mW per °C	5.26mW per °C

Schematic Diagram



Absolute Maximum Ratings

Supply Voltage ..... +5.5V/-16.5V
Internal Power Dissipation[1] 500mW
Differential Input Voltage 3V
Input Voltage ..... ±4V
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range
RM4805 ..... -55°C to +125°C
RC4805 ..... 0°C to +70°C
Lead Soldering Temperature (10 Sec) ..... +300°C

Note: 1. See table of Thermal Characteristics for maximum ambient temperature derating factor.

Ordering Information

Part Number	Package	Operating Temperature Range
RC4805DE	Ceramic	0°C to +70°C
RC4805EDE	Ceramic	0°C to +70°C
RC4805T	TO-99	0°C to +70°C
RC4805ET	TO-99	0°C to +70°C
RM4805DE	Ceramic	-55°C to +125°C
RM4805DE/883B*	Ceramic	-55°C to +125°C
RM4805ADE	Ceramic	-55°C to +125°C
RM4805ADE/883B*	Ceramic	-55°C to +125°C
RM4805T	TO-99	-55°C to +125°C
RM4805T/883B*	TO-99	-55°C to +125°C
RM4805AT	TO-99	-55°C to +125°C
RM4805AT/883B*	TO-99	-55°C to +125°C

*MIL-STD-883, Level B Processing

Electrical Characteristics (V_S = ±5V, RM = -55°C ≤ T_A ≤ +125°C; RC = 0°C ≤ T_A ≤ +70°C, Latch Enable = 0V unless otherwise noted)

Parameters	Test Conditions	RM4805A/RC4805E			RM4805/RC4805			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 50\Omega$		0.25	0.80		0.50	1.5	mV
Average Input Offset Voltage Drift			1.5	7.5		2.5	15	µV/°C
Input Offset Current			200				400	nA
Input Bias Current			2.5				3.8	µA
Large Signal Voltage Gain			15			10		V/mV
Output Voltage Swing	V_{IN} > 10mV, I_O = 200µA	2.2	2.5		2.2			V
	V_{IN} < -10mV, I_{SINK} = 6.4mA		0.3	0.45		0.3	0.45	
Input Voltage Range		±2.0			±2.0			V
Common Mode Rejection Ratio	$R_S \leq 50\Omega$, V_{CM} = ±2.0V	80			77			dB
Power Supply Rejection Ratio	$R_S \leq 50\Omega$ $+V_S$ = +5V, -5.25V ≤ $-V_S$ ≤ -4.75V and $-V_S$ = -5V, +4.75V ≤ $+V_S$ ≤ +5.25V	72			70			dB
Supply Current (Positive)	$V_O \leq 0.4V$		13	18		15	20	mA
Supply Current (Negative)	$V_O \leq 0.4V$		15	20		15	20	mA
Power Consumption	$V_O \leq 0.4V$		140	190		150	200	mW
Propagation Delay	100mV Step, V_{OD} = 5mV		30	50		35	55	nS
	100mV Step, V_{OD} = 1.2mV		50			50		

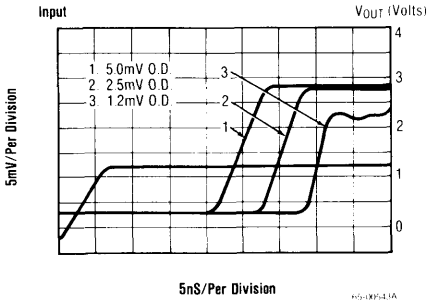
Electrical Characteristics (V_S = ±5V, T_A = +25°C, Latch Enable = 0V unless otherwise noted)

Parameters	Test Conditions	RM4805A/RC4805E			RM4805/RC4805			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 50\Omega$		100	250		250	600	μV
Input Offset Current			10	80		25	150	nA
Input Bias Current			0.7	1.2		0.9	1.8	μA
Large Signal Voltage Gain			20			20		V/mV
Output Voltage Swing	V_{IN} > 10mV, I_O = 200μA	2.4	2.7		2.4	2.7		V
	V_{IN} < −10mV, I_{SINK} = 8.0mA		0.3	0.4		0.3	0.4	
Input Voltage Range		±2.2	±2.7		±2.0	±2.7		V
Common Mode Rejection Ratio	$R_S \leq 50\Omega$, V_{CM} = Min Input Voltage Range	84			80			dB
Power Supply Rejection Ratio	$R_S \leq 50\Omega$, $+V_S$ = +5V, $-5.25V \leq -V_S \leq -4.75V$ and $-V_S$ = −5V, $+4.75V \leq +V_S \leq +5.25V$	80			74			dB
	$R_S \leq 50\Omega$ $+V_S$ = +5V, $-5V \leq -V_S \leq -15V$	80			76			
Supply Current (Positive)	$V_O \leq 0.4V$		11	16		13	18	mA
Supply Current (Negative)	$V_O \leq 0.4V$		12	16		13	18	mA
Power Consumption	$V_O \leq 0.4V$		115	160		130	180	mW
Propagation Delay	100mV Step, V_{OD} = 5mV		22	35		22	35	nS
	100mV Step, V_{OD} = 1.2mV		35			35		
Latch Enable Time	V_{OD} = 5mV		16			16		nS
Disable Time	V_{OD} = 5mV		22			22		
Latch High Voltage		2.0			2.0			V
Low Voltage				0.8			0.8	
Latch High Current	V_{LH} = 3.0V			40			75	μA
Low Current	V_{LL} = 0.8V			10			20	

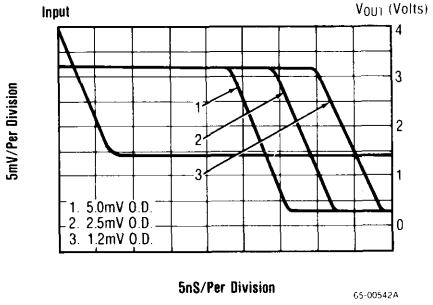
NOTE: Minimize lead lengths by soldering directly to PC board. The use of sockets may cause oscillations from stray capacitive coupling.

Typical Performance Characteristics

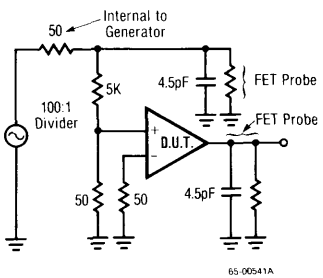
4805 Response Time Rising Edge



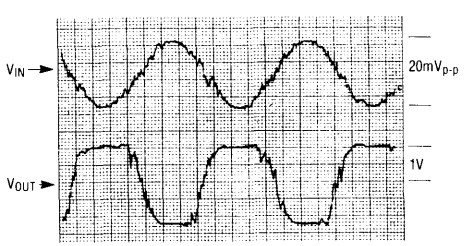
4805 Response Time Falling Edge



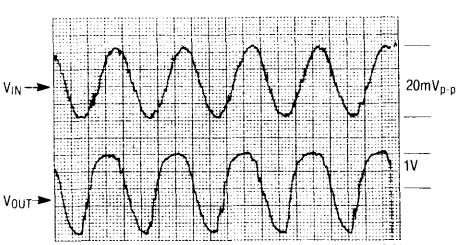
Response Photography Test Setup



Response to 25MHz Sine Wave

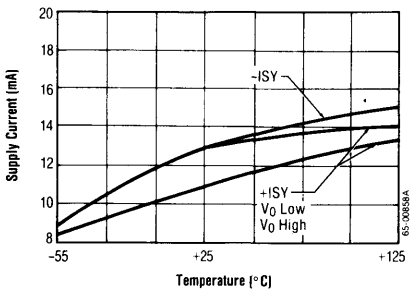


Response to 50MHz Sine Wave

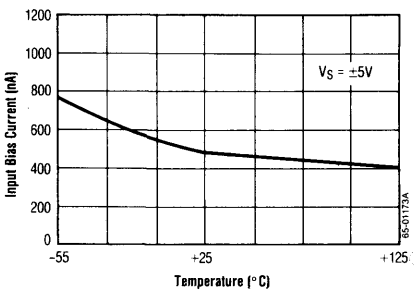


Typical Performance Characteristics (Continued)

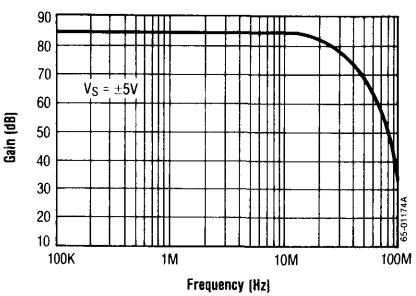
Supply Current vs. Temperature



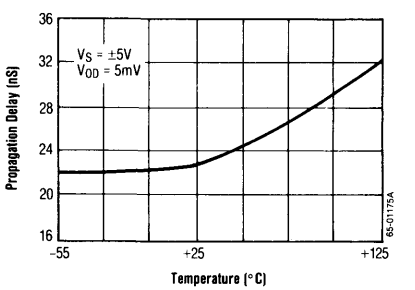
Input Bias Current vs. Temperature



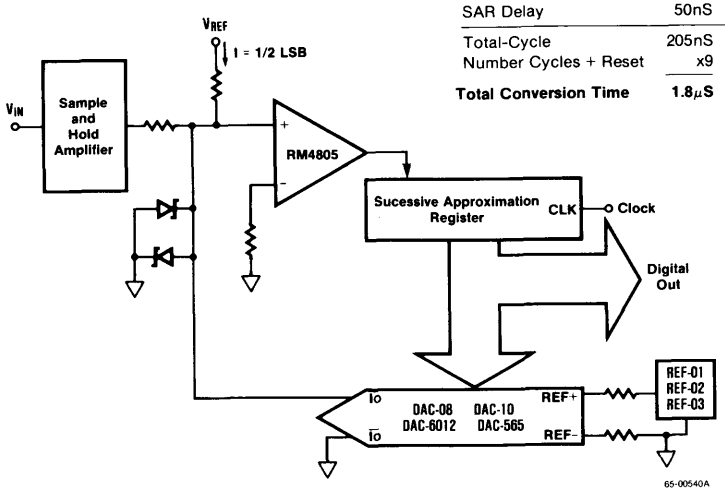
Gain vs. Frequency



Propagation Delay vs. Temperature



Typical Applications



	Conversion Time		
	8-Bit	10-Bit	12-Bit
RM4805 Response	20nS	22nS	50nS
DAC Settling*	135nS	135nS	500nS
SAR Delay	50nS	50nS	50nS
Total-Cycle	205nS	207nS	600nS
Number Cycles + Reset	x9	x11	x13
Total Conversion Time	**1.8μS**	**2.3μS**	**7.8μS**

*Response will be affected by DAC's output capacitance and equivalent resistance.

Figure 1. Successive Approximation 8, 10, or 12-bit Resolution

Typical Applications (Continued)

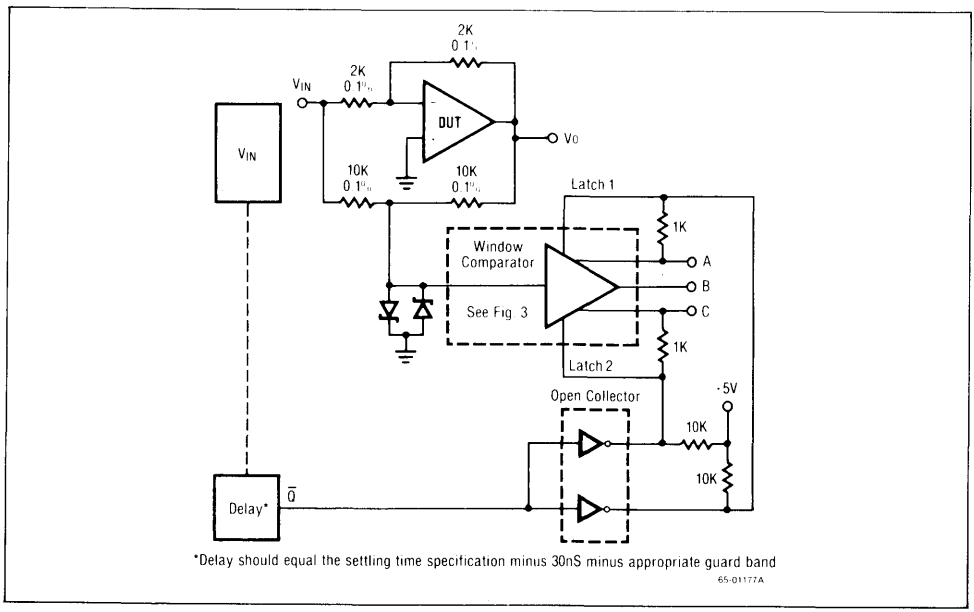
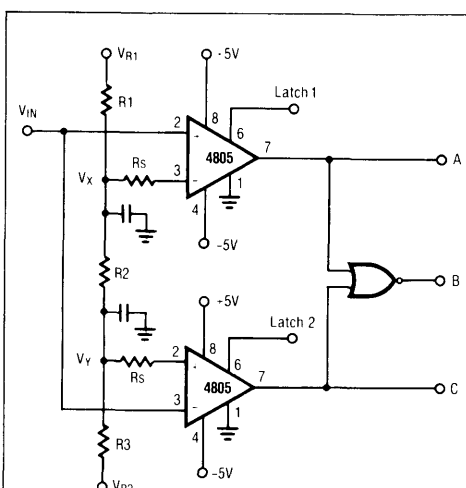


Figure 2. Op Amp Settling Time Tester



The settling time tester uses the precision latching window comparator to automate op amp settling time testing. If the DUT is not settled by the end of the time delay, the A output is latched low.

V_{IN} (V_X > V_Y)*	A	B	C
V_{IN} > V_X	1	0	0
V_X > V_{IN} > V_Y	0	1	0
V_Y > V_{IN}	0	0	1

*Both latches low

65-01176A

Figure 3. Precision Latching Window Comparator (Detail)

Fast Latching ECL to TTL Line Translator, Up to 50MHz

The high speed differential input and the latched TTL output makes the RC4805 ideally suited for use as an ECL to TTL translator. Existing logic supplies of -5.2V and +5.0V are compatible with the RC4805 power supply requirements. With a TTL compatible latch input the RC4805 can be latched from the TTL subsystem or from the ECL subsystem, by using another RC4805 on the latch signal.

In ECL systems the termination resistors and pull-down resistors can be combined in a network as shown in Figure 4, a typical ECL to TTL translator. The configuration shown in Figure 6 has a common mode range of ±2.0V. But either input can swing as low as -5.0V below the input, providing one input stays in the ±2.0V common mode range. By using a -15V supply on the RC4805 the common mode range is extended to -8.0V, +2.0V as shown in Figure 5. The only caution is that the differential mode voltage must not exceed +5.0V.

Not all ECL families have the same logic levels, the same logic level V_S supply voltage, or the same temperature characteristics. By using the same logic type as a reference, a single-end ECL to TTL translator can be made to track changes in logic levels. A typical circuit is shown in Figure 6.

In system design one subsystem may in one configuration be driven with ECL line drivers, but in another configuration the same subsystem may be driven from a TTL gate.

High gain, low input bias current and ±2.0V common mode range on the RC4805 allow the easy design of an adaptive ECL-TTL to TTL translator. The ECL interface is the same as shown in Figure 4. By adding pull-up resistors and a bypassed level shifting resistor to the TTL outputs (see Figure 7), the same subsystem line receiver can interface with ECL or TTL with no hardware change in the receiver.

In summary, the RC4805 is a very flexible system element that allows the system designer to interface ECL to TTL in a number of easy to use configurations. The RC4805 can also be used in an adaptive ECL-TTL to TTL interface.

Typical Examples

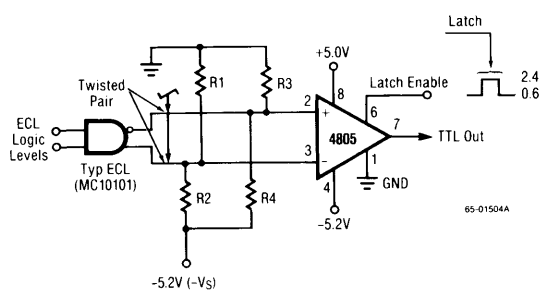
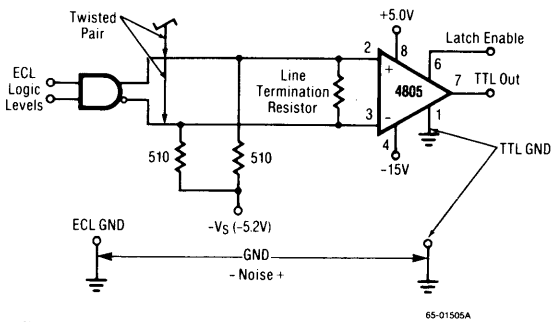


Figure 4. Typical ECL to TTL Translator

Typical Examples (Continued)



Notes:

1. Common mode range of 4805 is -8.0V to +2.0V.
2. The 4805 can stand -3.0V, +5.0V of GND noise from the ECL GND to the TTL GND.

Figure 5. ECL to TTL Translator with Extended Common Mode Range

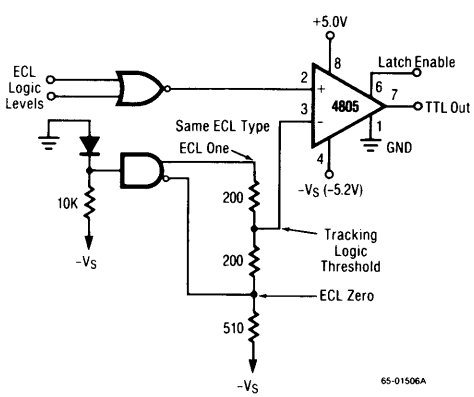


Figure 6. Single-Ended ECL to TTL Translator with Tracking ECL Reference

Typical Examples (Continued)

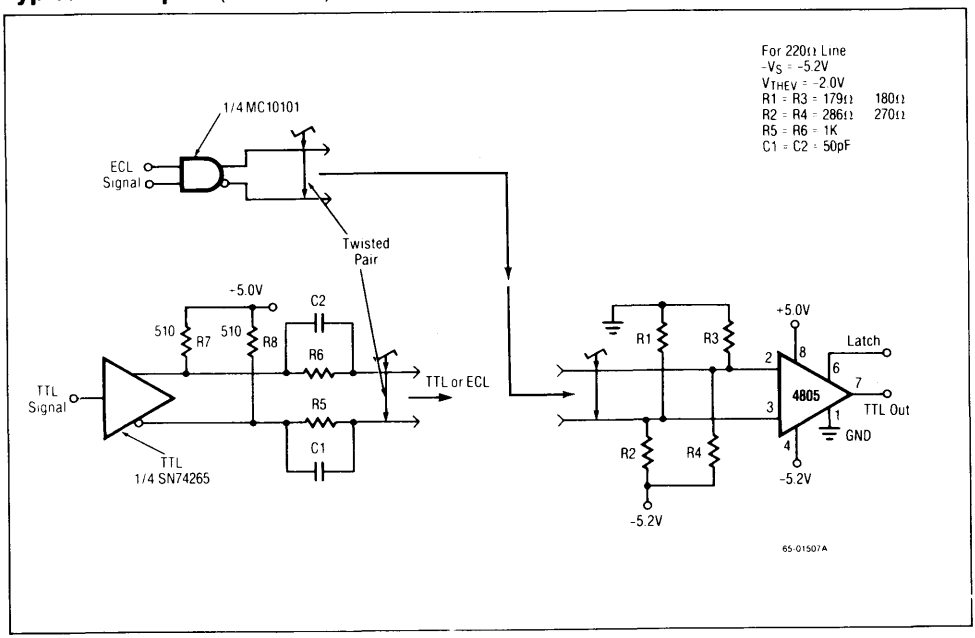


Figure 7. Adaptive ECL-TTL to TTL Translator

Section 8
Digital-to-Analog Converters

Three types of D/A converters are included in this handbook: standard types, the more complete DAC-4565 type, and the complete DAC-4881. The standard type requires several external components for application: a voltage reference, external resistors, and an op amp for output buffering. The REF series of voltage references and the OP series of precision op amps will complement Raytheon's multiplying D/A converters in most applications. The DAC-4565 contains a voltage reference and trimmed application resistors internally and requires only an op amp for stand-alone operation.

The DAC-4881, like the DAC-4565, contains a voltage reference and resistors, but also includes a high speed current-to-voltage conversion amplifier (no op amp needed), plus a microprocessor interface latch/buffer, making it a truly "complete" stand-alone DAC.

The multiplying D/A converters are available in 8, 10, and 12-bit versions. Raytheon's version of the popular DAC-08 is trimmed for accuracy using "zener zap". This increases yields and lowers production costs, and so makes the higher grades more available.

The D/A converter selection is shown below:

DAC-08 ..... 8 bit resolution, 0.1% nonlinearity
DAC-10 .... 10 bit resolution, .05% nonlinearity
DAC-6012 ..... 12 bit resolution, 0.05% nonlinearity
DAC-4565[1] ..... 12 bit resolution, .012% nonlinearity
DAC-4881[2] ..... 12 bit resolution, .012% nonlinearity

[1]Includes trimmed voltage reference and trimmed resistors internally.
[2]Includes reference, resistors, amplifier, and microprocessor latches internally.

DEFINITIONS

Differential Nonlinearity (DNL)
The incremental error from an ideal 1 LSB analog output change when the input is changed 1 LSB; guaranteed monotonicity requires the differential nonlinearity error to be less than 1 LSB. Differential nonlinearity is expressed as a percentage of the full scale output.

Full Scale Current (I_{FS})
The maximum current that can be obtained from the output, for a specified reference current, measured in milliamps (mA). A typical binary D/A produces its full scale output with all ones applied at the input.

Full Scale Symmetry
The difference between the full scale output values of the two outputs of a complementary output D/A, expressed in microamps (μA).

Gain Temperature Coefficient
The variation of full scale current measured over a specified temperature range, expressed in parts per million per degree C (ppm/°C).

$$\text{Gain TC} = \left(\frac{I_{FS} @ T_{(1)} - I_{FS} @ T_{(2)}}{T_{(1)} - T_{(2)}}\right)\left(\frac{10^6}{I_{FS}}\right)$$

Where $T_{(1)}$ and $T_{(2)}$ are the upper and lower limits of the specified temperature range.

Least Significant Bit (LSB)
The digital input line which has the smallest effect on the analog output. LSB can also refer to the measure of the analog output change when the input code is incremented; in that case, the ideal value of 1 LSB is calculated as:

$$1\ \text{LSB} = \left(\frac{1}{2^N}\right)(\text{Full Scale Range})\ \text{in V or mA}$$

where N is the resolution of the converter.

Logic Input Current
The input current into the logic switch at a specified applied voltage, expressed in microamps (μA).

Logic Input Levels
The range of voltages within which the logic trip level is guaranteed to be expressed in volts (V).

Monotonicity
For any one LSB increase in input code the D/A output either increases or remains constant.

Nonlinearity
The difference between the actual analog output and an imaginary straight line drawn between the measured zero scale and full scale readings, for any code combination. Nonlinearity is expressed as a percentage of the full scale output.

Output Capacitance
The value of the internal parasitic capacitances, modeled as a single capacitor from the output to ground, expressed in picofarads (pF).

Output Voltage Compliance
The range of voltages over which the output can be driven while maintaining nonlinearity specifications, measured in volts (V).

Power Consumption
The DC power required to operate the D/A converter with a specified reference current, expressed in milliwatts (mW).

Power Supply Sensitivity
The ratio of change in the full scale output to a change in supply voltage, measured in percent of full scale per percent change in supply voltage (%ΔFS/%ΔV).

Propagation Delay
The time delay between a step input to all inputs and a change in the output, from the 50% point of TTL input swing to the 50% point of the final output value. Propagation delay is expressed in nanoseconds (nS).

Reference Bias Current
The input current to the reference amplifier which subtracts from the reference current, expressed in microamps (μA).

Reference Current Range
The range of currents into the reference terminal over which the D/A converter is guaranteed to meet the resolution specification, measured in milliamps (mA).

DEFINITIONS (Continued)

Reference Input Slew Rate
The average rate of change of the output current for a step change at the reference input, expressed in milliamps per microsecond (mA/μS).

Resolution
The number of inputs or bits. The number of discrete steps or states at the output is equal to 2^N, where N is the resolution of the converter.

Settling Time
The time delay between a 50% of TTL level change at all logic inputs to the point where the output settles within a specified error band of its final value, for either full scale to zero scale or zero scale to full scale changes. Settling time is measured in nanoseconds or microseconds (nS or μS).

Supply Current
The current required from the power supply to operate the D/A converter under specified supply voltage and reference current conditions, expressed in milliamps (mA).

Supply Voltage
The range of power supply voltages over which the D/A converter is guaranteed to meet the resolution specification, expressed in volts (V).

Zero Scale Current
The leakage current flowing into the D/A converter output with all logic inputs off and the output at a specified voltage, expressed in microamps (μA).

Raytheon

8-Bit High Speed Multiplying D/A Converter

DAC-08

Features

- Fast settling output current — 85nS
- Full scale current prematched to ±1.0 LSB
- Direct interface to TTL, CMOS, ECL, HTL, PMOS
- Nonlinearity to ±0.1% max. over temperature range
- High output impedance and compliance — -10V to +18V
- Differential current outputs
- Wide range multiplying capability — 1.0MHz bandwidth
- Low FS current drift — ±10ppm/°C
- Wide power supply range — ±4.5V to ±18V
- Low power consumption — 33mW @ ±5.0V
- Low cost

Description

The DAC-08 series of 8-bit monolithic multiplying Digital-to-Analog Converters provide very high speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 85nS settling times with very low "glitch" and at low power consumption. Monotonic multiplying performance is attained over a wide 40 to 1 reference current range. Matching to within 1 LSB between reference and full scale currents eliminates the need for full scale trimming in most applications.

Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

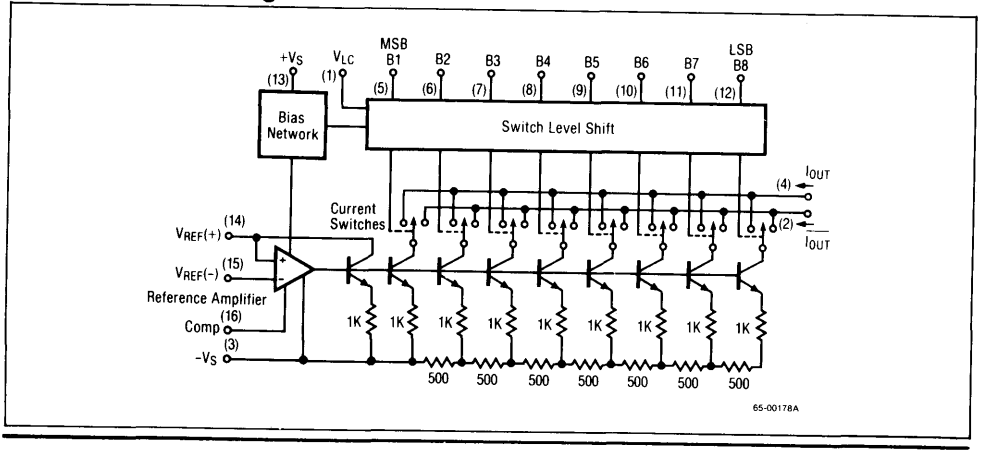
High voltage compliance dual complementary current outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. In many applications, the outputs can be directly converted to voltage without the need for an external op amp.

All DAC-08 series models guarantee full 8-bit monotonicity, and nonlinearities as tight as ±0.1% over the entire operating temperature range are available. Device performance is essentially unchanged over the ±4.5V to ±18V power supply range, with 33mW power consumtion attainable at ±5.0V supplies.

The compact size and low power consumption make the DAC-08 attractive for portable and military/aerospace applications; devices processed to MIL-STD-883A, Level C are available.

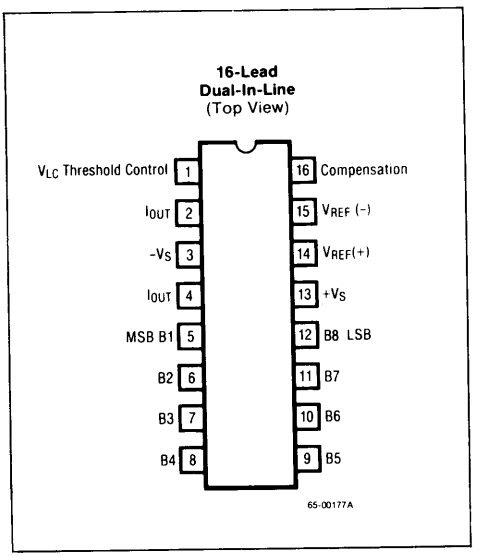
DAC-08 applications include 8-bit, 1.0μS A/D converters, servo-motor and pen drivers, waveform generators, audio encoders and attenuators, analog meter drivers, programmable power supplies, CRT display drivers, high speed modems and other applications where low cost, high speed and complete input/output versatility are required.

Functional Block Diagram

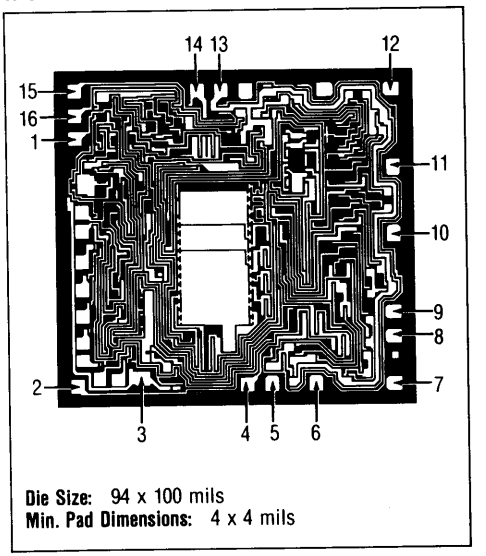


8-Bit High Speed Multiplying D/A Converter

Connection Information



Mask Pattern



Die Size: 94 x 100 mils
Min. Pad Dimensions: 4 x 4 mils

Thermal Characteristics

	16-Lead Ceramic DIP
Max. Junction Temp.	175°C
Max. P_D $T_A < 50°C$	1042mW
Therm. Res. θ_{JC}	60°C/W
Therm. Res. θ_{JA}	120°C/W
For $T_A > 50°C$ Derate at	8.38mW per °C

Ordering Information

Part Number	Package	Operating Temperature Range	Nonlinearity
DAC-08HDC	Ceramic	0°C to +70°C	±0.1%
DAC-08EDC	Ceramic	0°C to +70°C	±0.19%
DAC-08CDC	Ceramic	0°C to +70°C	±0.39%
DAC-08ADM	Ceramic	-55°C to +125°C	±0.1%
DAC-08DM	Ceramic	-55°C to +125°C	±0.19%
DAC-08DM/883B*	Ceramic	-55°C to +125°C	±0.19%
DAC-08ADM/883B*	Ceramic	-55°C to +125°C	±0.1%

*MIL-STD-883, Level B Processing

Absolute Maximum Ratings

(T_A = +25° C unless otherwise noted)

Supply Voltage (between $+V_S$ and $-V_S$) .. 36V
Logic Inputs ..... $-V_S$ to $-V_S$ plus 36V
V_{LC} ..... $-V_S$ to $+V_S$
Analog Current Outputs 4mA
Reference Inputs (V_{14} to V_{15}) ..... $-V_S$ to $+V_S$
Reference Input Differential
Voltage (V_{14} to V_{15}) ..... ±18V
Reference Input Current (I_{14}) 5.0mA
Operating Temperature Range
DAC-08ADM, DM ..... -55° C to +125° C
DAC-08HDC, EDC, CDC .... 0° C to +70° C
Storage Temperature
Range ..... -65° C to +150° C
Lead Soldering Temperature
(60 Sec) ..... +300° C

Electrical Characteristics (V_S = ±15V, I_{REF} = 2.0mA, T_A = -55°C to +125°C for DAC-08 and DAC-08A; T_A = 0°C to +70°C for DAC-08C, DAC-08E and DAC-08H unless other specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.)

Parameters	Test Conditions	DAC-08A/-08H			DAC-08			Units
		Min	Typ	Max	Min	Typ	Max	
Resolution		8	8	8	8	8	8	Bits
Monotonicity		8	8	8	8	8	8	Bits
Nonlinearity	Full Temperature Range			±0.1			±0.19	%FS
Settling Time	To +½LSB, All Bits Switched ON or OFF T_A = +25°C (See Note)		85	135		85	150	nS
Propagation Delay Each Bit	T_A = +25°C (See Note)		35	60		35	60	nS
All Bits Switched			35	60		35	60	nS
Full Scale Tempco			±10	±50		±10	±80	ppm/°C
Output Voltage Compliance	Full Scale Current Change < ½LSB R_{OUT} > 20MΩ Typical	-10		+18	-10		+18	V
Full Scale Current	V_{REF} = 10.000V R_{14}, R_{15} = 5.000kΩ T_A = +25°C	1.984	1.992	2.000	1.94	1.99	2.04	mA
Full Scale Summetry	I_{FS4}-I_{FS2}		±0.5	±4.0		±1.0	±8.0	μA
Zero Scale Current			0.1	1.0		0.2	2.0	μA
Output Current Range	V_{REF} = +15V, $-V_S$ = -10V	2.1			2.1			mA
R_{14}, R_{15} = 5.000kΩ	V_{REF} = +25V, $-V_S$ = -12V	4.2			4.2			mA
Logic Input Levels Logic "0"	V_{LC} = 0V			0.8			0.8	V
Logic "1"		2.0			2.0			V
Logic Input Current Logic "0"	V_{LC} = 0V V_{IN} = -10V to +0.8V		-2.0	-10		-2.0	-10	μA
Logic "1"	V_{IN} = 2.0V to 18V		0.002	10		0.002	10	μA
Logic Input Swing	$-V_S$ = -15V	-10		+18	-10		+18	V
Logic Threshold Range	V_S = ±15V	-10		+13.5	-10		+13.5	V
Reference Bias Current			-1.0	-3.0		-1.0	-3.0	μA
Reference Input Slew Rate		4.0	8.0		4.0	8.0		mA/μS

Note: Guaranteed by Design

Electrical Characteristics (Continued)

Parameters	Test Conditions	DAC-08A/-08H			DAC-08			Units
		Min	Typ	Max	Min	Typ	Max	
Power Supply Sensitivity Positive	$+V_S$ = 4.5V to 18V $-V_S$ = -4.5V to -18V I_{REF} = 1.0mA		±0.0003	±0.01		±0.0003	±0.01	$\frac{\%\Delta FS}{\%\Delta V}$
Negative			±0.002	±0.01		±0.002	±0.01	%/%
Power Supply Current Positive	V_S = ±5.0V, I_{REF} = 1.0mA		2.3	3.8		2.3	3.8	mA
Negative			-4.3	-5.8		-4.3	-5.8	mA
Positive	V_S = +5.0V, -15V, I_{REF} = 2.0mA		2.4	3.8		2.4	3.8	mA
Negative			-6.4	-7.8		-6.4	-7.8	mA
Positive	V_S = ±15V, I_{REF} = 2.0mA		2.5	3.8		2.5	3.8	mA
Negative			-6.5	-7.8		-6.5	-7.8	mA
Power Consumption	V_S = ±5.0V, I_{REF} = 1.0mA		33	48		33	48	mW
	V_S = +5.0V, -15V, I_{REF} = 2.0mA		108	136		108	136	mW
	V_S = ±15V, I_{REF} = 2.0mA		135	174		135	174	mW

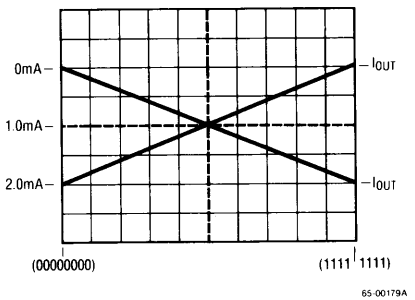
Parameters	Test Conditions	DAC-08E			DAC-08C			Units
		Min	Typ	Max	Min	Typ	Max	
Resolution		8	8	8	8	8	8	Bits
Monotonicity		8	8	8	8	8	8	Bits
Nonlinearity	Full Temperature Range			+0.19			+0.39	%FS
Settling Time	To +½LSB, All Bits Switched ON or OFF T_A = +25°C (See Note)		85	150		85	150	nS
Propagation Delay Each Bit	T_A = +25°C (See Note)		35	60		35	60	nS
All Bits Switched			35	60		35	60	nS
Full Scale Tempco			±10	±50		±10	±80	ppm/°C
Output Voltage Compliance	Full Scale Current Change < ½LSB R_{OUT} > 20MΩ Typical	-10		+18	-10		+18	V
Full Scale Current	V_{REF} = 10.000V R_{14}, R_{15} = 5.000kΩ T_A = +25°C	1.94	1.99	2.04	1.94	1.99	2.04	mA
Full Scale Summetry	I_{FS4}-I_{FS2}		±1.0	±8.0		±2.0	±16.0	μA

Electrical Characteristics (Continued)

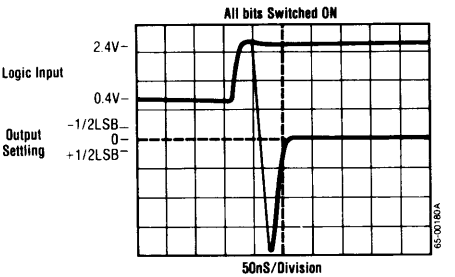
Parameters	Test Conditions	DAC-08E			DAC-08C			Units
		Min	Typ	Max	Min	Typ	Max	
Zero Scale Current			0.2	2.0		0.2	4.0	μA
Output Current Range	V_{REF} = +15V, $-V_S$ = -10V	2.1			2.1			mA
R_{14}, R_{15} = 5.000kΩ	V_{REF} = +25V, $-V_S$ = -12V	4.2			4.2			mA
Logic Input Levels								
Logic "0"	V_{LC} = 0V			0.8			0.8	V
Logic "1"		2.0			2.0			V
Logic Input Current	V_{LC} = 0V							
Logic "0"	V_{IN} = -10V to +0.8V		-2.0	-10		-2.0	-10	μA
Logic "1"	V_{IN} = 2.0V to 18V		0.002	10		0.002	10	μA
Logic Input Swing	$-V_S$ = -15V	-10		+18	-10		+18	V
Logic Threshold Range	V_S = ±15V	-10		+13.5	-10		+13.5	V
Reference Bias Current			-1.0	-3.0		-1.0	-3.0	μA
Reference Input Slew Rate		4.0	8.0		4.0	8.0		mA/μS
Power Supply Sensitivity	$+V_S$ = 4.5V to 18V, $-V_S$ = -4.5V to -18V							
Positive	I_{REF} = 1.0mA		±0.0003	±0.01		±0.0003	±0.01	%ΔFS/%ΔV
Negative			±0.002	±0.01		±0.002	±0.01	
Power Supply Current								
Positive	V_S = ±5.0V,		2.3	3.8		2.3	3.8	mA
Negative	I_{REF} = 1.0mA		-4.3	-5.8		-4.3	-5.8	mA
Positive	V_S = +5.0V, -15V,		2.4	3.8		2.4	3.8	mA
Negative	I_{REF} = 2.0mA		-6.4	-7.8		-6.4	-7.8	mA
Positive	V_S = ±15V,		2.5	3.8		2.5	3.8	mA
Negative	I_{REF} = 2.0mA		-6.5	-7.8		-6.5	-7.8	mA
Power Consumption	V_S = ±5.0V, I_{REF} = 1.0mA		33	48		33	48	mW
	V_S = +5.0V, -15V, I_{REF} = 2.0mA		103	136		103	136	mW
	V_S = ±15V, I_{REF} = 2.0mA		135	174		135	174	mW

Typical Performance Characteristics

True and Complementary Output Operation

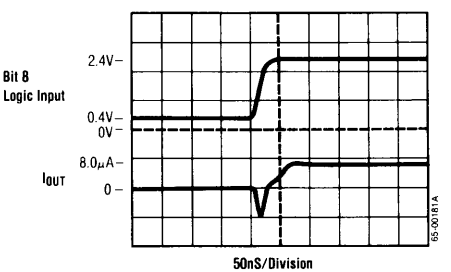


Full Scale Settling Time

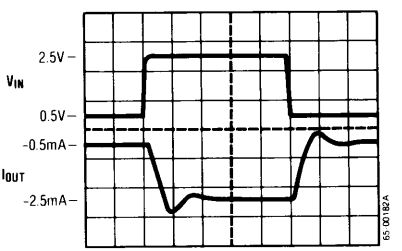


I_{FS} = 2.0mA
R_L = 1.0KΩ
1/2 LSB = 4.0μA

LSB Switching

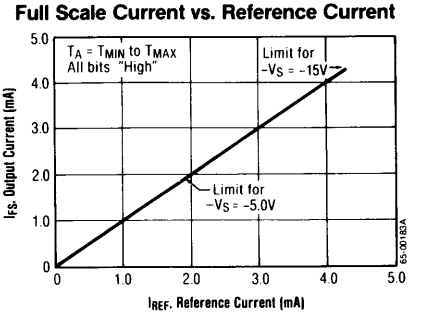


Fast Pulsed Reference Operation



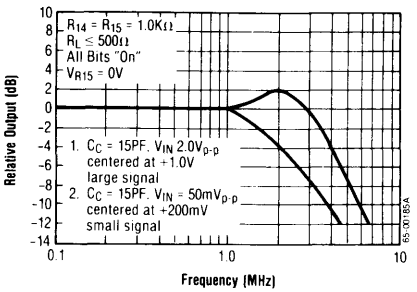
R_{EQ} (Input) 200Ω
R_L 100Ω
C_C 0
R_{IN} 5.0K
V_{IN} 10V

Full Scale Current vs. Reference Current

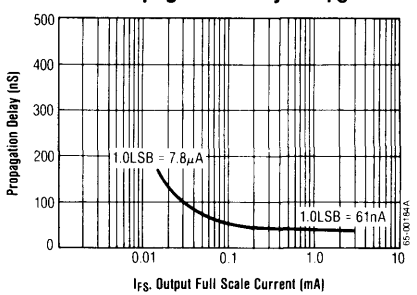


Typical Performance Characteristics (Continued)

Reference Input Frequency Response



LSB Propagation Delay vs. I_{FS}



Applications Information

Reference Amplifier Setup

The DAC-08 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +4.0mA. The full scale output current is a linear function of the reference current and is given by:

$$I_{FS} = \frac{255}{256} \times I_{REF} \text{ where } I_{REF} = I_{14}$$

In positive reference applications, an external positive reference voltage forces current through R_{14} into the $V_{REF(+)}$ terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at pin 15; reference current flows from ground through R_{14} into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. R_{15} (nominally equal to R_{14}) is used to cancel bias current errors; R_{15} may be eliminated with only a minor increase in error.

Bipolar references may be accommodated by offsetting V_{REF} or pin 15. The negative common mode range of the reference amplifier is given by: V_{CM-} = $-V_S$ plus (I_{REF} x 1kΩ) plus 2.5V. The positive common mode range is $+V_S$ less 1.5V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R_{14} should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full scale trimming may be accomplished by adjusting the value of R_{14}, or by using a potentiometer for R_{14}. An improved method of full scale trimming which eliminates potentiometer T.C. effects is shown in the recommended full scale adjustment circuit.

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common mode range. The recommended range for operation with a DC reference current is +0.2mA to +4.0mA.

The reference amplifier must be compensated by using a capacitor from pin 16 to $-V_S$. For fixed reference operation, a 0.01μF capacitor is recommended. For variable reference applications, see section entitled "Reference Amplifier Compensation for Multiplying Applications."

Multiplying Operation

The DAC-08 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 4.0mA to 4.0μA. Monotonic operation is maintained over a typical range of I_{REF} from 100μA to 4.0mA.

Reference Amplifier Compensation for Multiplying Applications

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to $-V_S$. The value of this capacitor depends on the impedance presented to pin 14; for R_{14} values of 1.0, 2.5, and 5.0kΩ, minimum values of C_C are 15, 37, and 75pF. Larger values of R_{14} require proportionately increased values of C_C for proper phase margin.

For fastest response to a pulse, low values of R_{14} enabling small C_C values should be used. If pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R_{14} = 1.0kΩ and C_C = 15pF, the reference amplifier slews at 4.0mA/μS enabling a transition from I_{REF} = 0 to I_{REF} = 2.0mA in 500nS.

Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme. This technique provides lowest full scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff (I_{REF} = 0) condition. Full scale transition (0 to 2.0mA) occurs in 120nS when the equivalent impedance at pin 14 is 200Ω and C_C = 0. This yields a reference slew rate of 16mA/μS which is relatively independent of R_{IN} and V_{IN} values.

Logic Inputs

The DAC-08 design incorporates a unique logic input circuit which enbles direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2.0μA logic input current and completely adjustable logic threshold voltage. For $-V_S$ = -15V, the logic inputs may swing between -10V and +18V. This enables direct interface with +5V CMOS logic, even when the DAC-08 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by: $-V_S$ plus (I_{REF} x 1.0kΩ) plus 2.5V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 1, V_{LC}). The appropriate graph shows the relationship between V_{LC} and V_{TH} over the temperature range, with V_{TH} nominally 1.4V above V_{LC}. For TTL and DTL interface, simply ground pin 1. When interfacing ECL an I_{REF} = 1.0mA is recommended. For general setup of the logic control circuit, it should be noted that pin 1 will source 100μA typical; external circuitry should be designed to accommodate this current.

Fastest settling times are obtained when pin 1 sees a low impedance. If pin 1 is connected to a 1.0kΩ divider, for example, it should be bypassed to ground by a 0.01μF capacitor.

Analog Output Currents

Both true and complemented output sink currents are provided where $I_O + \overline{I_O} = I_{FS}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 4 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 4 and turned on at pin 2. A decreasing logic count increases $\overline{I_O}$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FS}; do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36V above $-V_S$ and is independent of the positive supply. Negative compliance is given by $-V_S$ plus (I_{REF} x 1.0kΩ) plus 2.5V.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection, and other balanced applications such as driving center-tapping coils and transformers.

Power Supplies

The DAC-08 operates over a wide range of power supply voltages from a total supply of 9V to 36V. When operating at supplies of ±5.0V or less, $I_{REF} \leq$ 1.0mA is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at -4.5V with I_{REF} = 2mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible. However, at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC-08 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required. However, an artificial ground may be used to insure logic swings, etc. remain between acceptable limits.

Power consumption may be calculated as follows: $P_d = (I+)\ (+V_S) + (I-)\ (-V_S) + (2\ I_{REF})\ (-V_S)$. A useful feature of the DAC-08 design is that supply current is constant and independent of input logic states; this is useful in cryptographic applications and further serves to reduce the size of the power bypass capacitors.

Temperature Performance

The nonlinearity and monotonicity specifications of the DAC-08 are guaranteed to apply over the entire rated operating temperature range. Full scale output current drift is typically ±10ppm/°C, with zero scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R_{14} should match and track that of the output resistor for minimum overall full scale drift. Settling times of the DAC-08 decrease approximately 10% at -55°C; at +125°C an increase of about 15% is typical.

Typical Applications

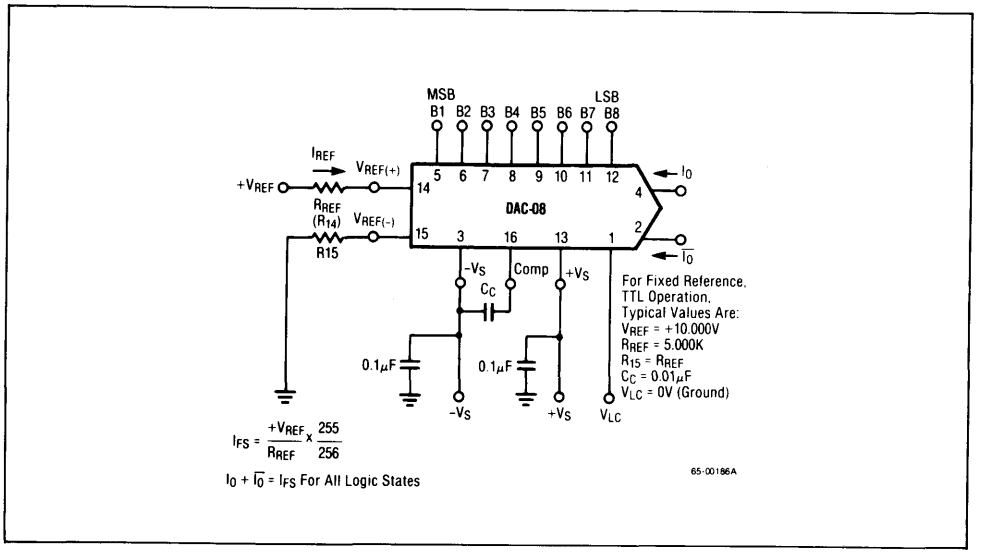


Figure 1. Basic Positive Reference Operation

Typical Applications (Continued)

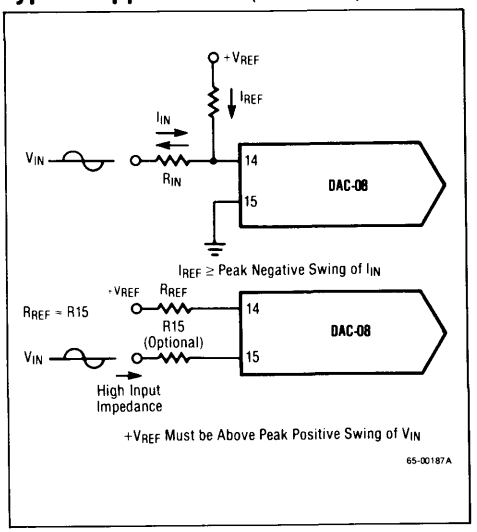


Figure 2. Accommodating Bipolar References

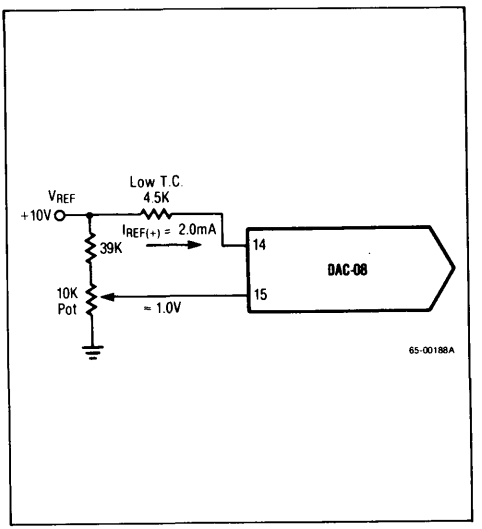


Figure 3. Recommended Full Scale Adjustment Circuit

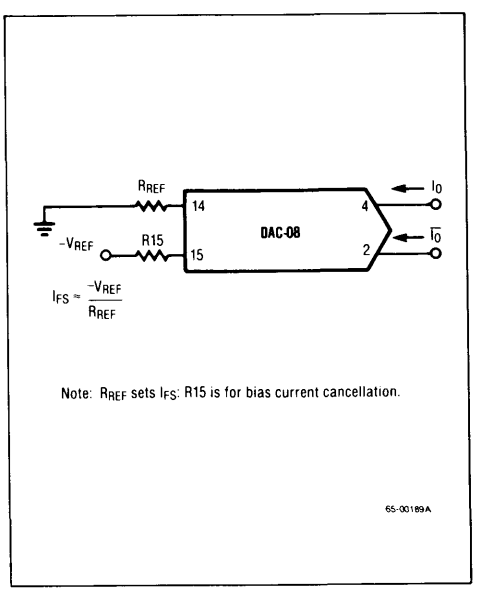
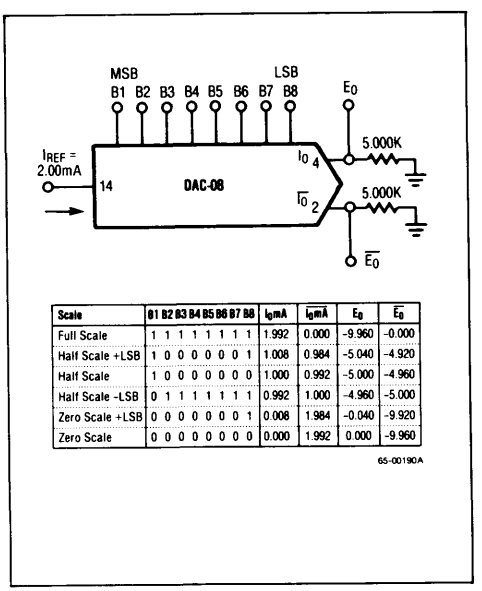


Figure 4. Basic Negative Reference Operation

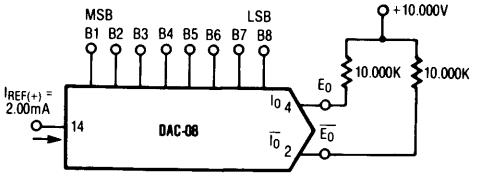


Scale	B1	B2	B3	B4	B5	B6	B7	B8	I_0mA	$\overline{I_0}$mA	E_0	$\overline{E_0}$
Full Scale	1	1	1	1	1	1	1	1	1.992	0.000	-9.960	-0.000
Half Scale +LSB	1	0	0	0	0	0	0	1	1.008	0.984	-5.040	-4.920
Half Scale	1	0	0	0	0	0	0	0	1.000	0.992	-5.000	-4.960
Half Scale -LSB	0	1	1	1	1	1	1	1	0.992	1.000	-4.960	-5.000
Zero Scale +LSB	0	0	0	0	0	0	0	1	0.008	1.984	-0.040	-9.920
Zero Scale	0	0	0	0	0	0	0	0	0.000	1.992	0.000	-9.960

65-00190A

Figure 5. Basic Unipolar Negative Operation

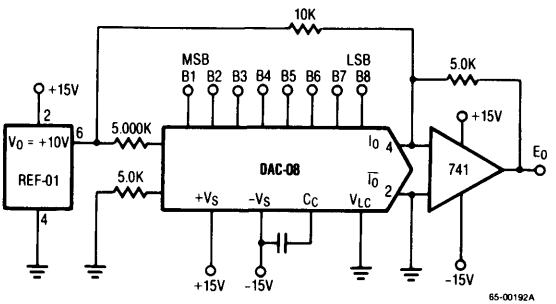
Typical Applications (Continued)



Scale	B1 B2 B3 B4 B5 B6 B7 B8	E_0	$\overline{E_0}$
Pos Full Scale	1 1 1 1 1 1 1 1	-9.920	+10.000
Pos Full Scale -LSB	1 1 1 1 1 1 1 0	-9.840	+9.920
Zero Scale +LSB	1 0 0 0 0 0 0 1	-0.080	+0.160
Zero Scale	1 0 0 0 0 0 0 0	0.000	+0.080
Zero Scale -LSB	0 1 1 1 1 1 1 1	+0.080	0.000
Neg Full Scale +LSB	0 0 0 0 0 0 0 1	+9.920	-9.840
Neg Full Scale	0 0 0 0 0 0 0 0	+10.000	-9.920

65-00191A

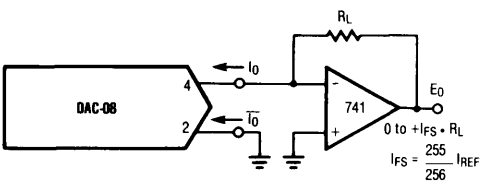
Figure 6. Basic Bipolar Output Operation



65-00192A

Scale	B1 B2 B3 B4 B5 B6 B7 B8	E_0
Pos Full Scale	1 1 1 1 1 1 1 1	+4.960
Zero Scale	1 0 0 0 0 0 0 0	0.00
Neg Full Scale +1 LSB	0 0 0 0 0 0 0 1	-4.960
Neg Full Scale	0 0 0 0 0 0 0 0	-5.000

Figure 7. Offset Binary Operation

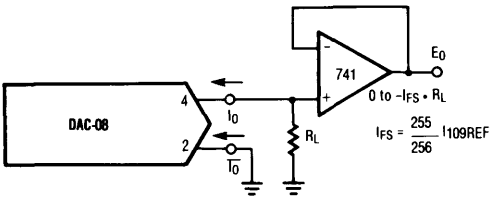


For complementary output (operation as a negative logic DAC), connect inverting input of Op-Amp to I_0 (pin 2); connect I_0 (pin 4) to ground.

65-00193A

Figure 8. Positive Low Impedance Output Operation

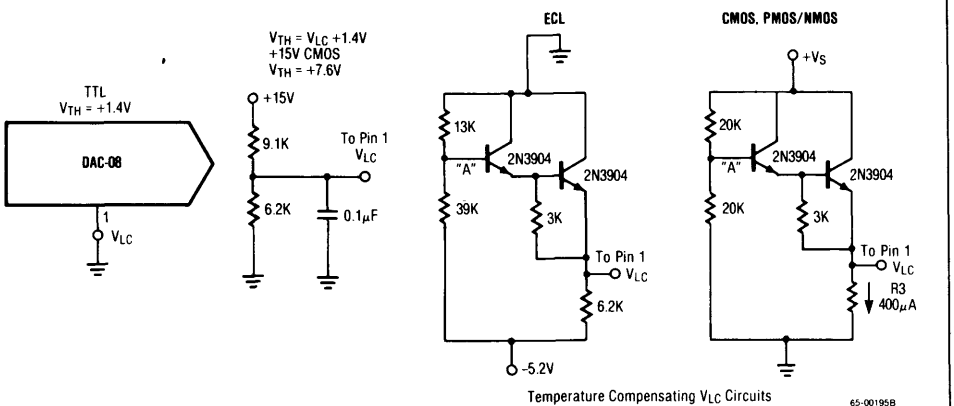
Typical Applications (Continued)



For complementary output (operation as a negative logic DAC), connect non-inverting input of Op-Amp to I_O (pin 2); connect I_O (pin 4) to ground.

65-00194A

Figure 9. Negative Low Impedance Output Operation



Temperature Compensating V_{LC} Circuits

65-00195B

Figure 10. Interfacing With Various Logic Families

Settling Time

The DAC-08 is capable of extremely fast settling times, typically 85nS at I_{REF} = 2.0mA. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 35nS for each of the 8 bits. Settling time to within 1/2 LSB of the LSB is therefore 35nS, with each progressively larger bit taking successively longer. The MSB settles in 85nS, thus determining the overall settling time of 85nS. Settling to 6-bit accuracy requires about 65 to 70nS. The output capacitance of the DAC-08 including the package is approximately 15pF; therefore the output RC time constant dominates settling time if R_L > 500Ω.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 1.0mA, with gradual increases for lower I_{REF} values. The principal advantage of higher I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve ±4.0μA, therefore a 1.0kΩ load is needed to provided adequate drive for most oscilloscopes. The settling time fixture uses a cascode design to permit driving a 1.0kΩ load with less than 5.0pF of parasitic capacitance at the measurement node. At I_{REF} values of less than 1.0mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 01111111 to 10000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ±0.2% of the final value, and thus settling times may be observed at lower values of I_{REF}.

DAC-08 switching transients or "glitches" are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic state; 0.1μF capacitors at the supply pins provide full transient protection.

Typical Applications (Continued)

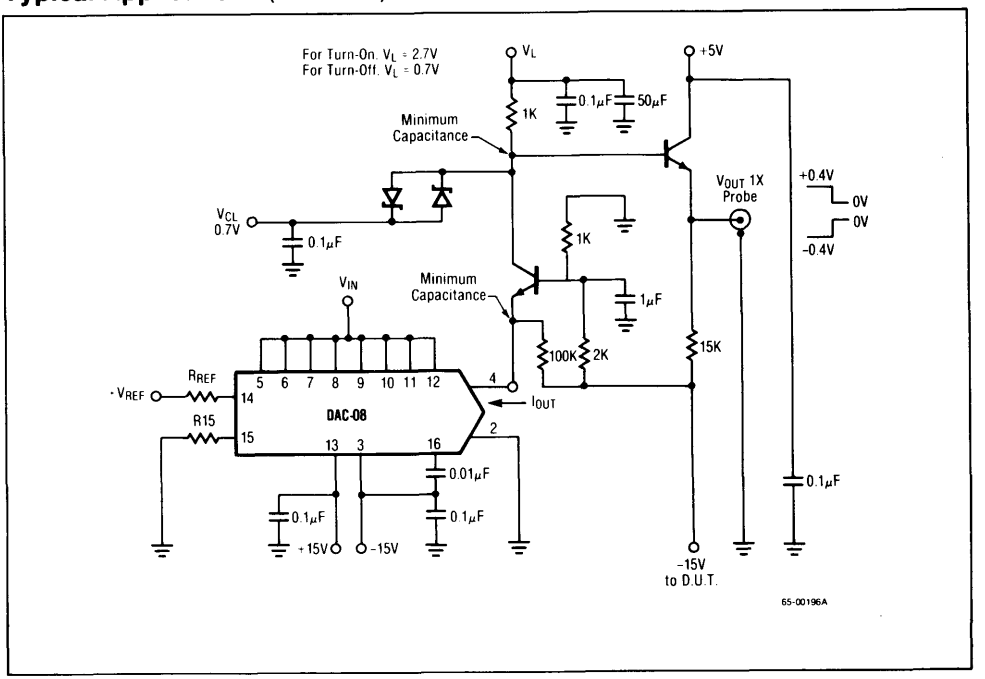


Figure 11. Settling Time Test Fixture

Raytheon

10-Bit High Speed Multiplying D/A Converter

DAC-10

Features

- Nonlinearity to 0.05% max over temperature range
- Low full scale drift — 10ppm/°C
- Wide range multiplying capability — 1.0MHz bandwidth
- Wide power supply range — +5.0V/-7.5V to ±18V
- Two quadrant multiplying
- High output compliance
- High speed — 85nS

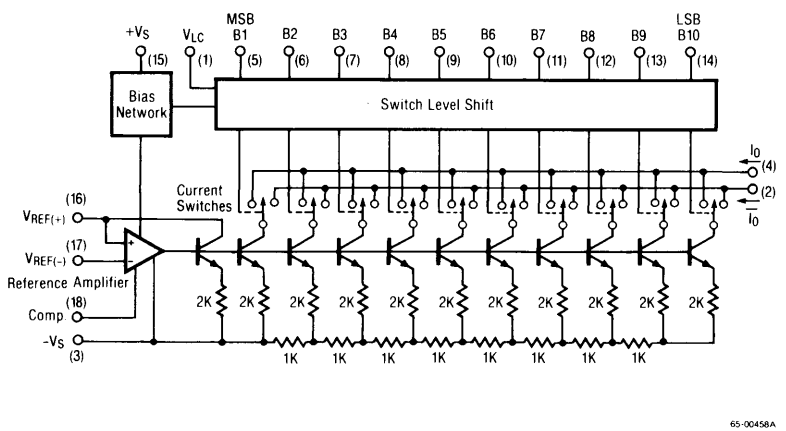
Applications

- A/D converters
- Servo controls
- Waveform generators
- Programmable power supplies
- High Speed Modems

Description

The DAC-10 is a high speed, 10-bit, monolithic, multiplying Digital-to-Analog Converter. Settling times of 85nS are achieved with low power consumption and minimal output glitches. Full scale (10-bit) accuracy is achieved. The DAC-10 can be operated from almost any logic level input due to its adjustable (V_{LC}) threshold. Monotonicity is guaranteed to 10 bits and nonlinearities of ±0.05% are guaranteed over the full operating temperature range. Power consumption can be reduced to 85mW by lowering supply voltages to +5.0V to -7.5V. Operation at supply voltages up to ±18V does not appreciably affect device performance. Zener-Zap trimming is performed at wafer probe to optimize the converter's accuracy.

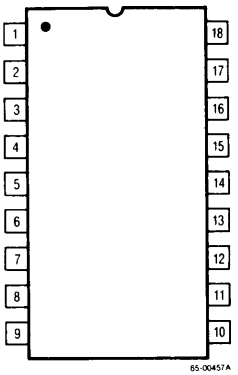
Simplified Schematic Diagram



10-Bit High Speed Multiplying D/A Converter

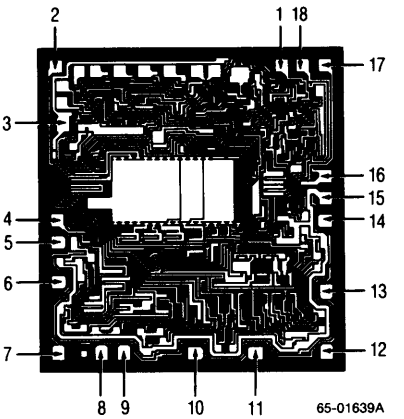
Connection Information

18-Lead
Hermetic Dual In-Line
(Top View)



Pin	Function
1	V_{LC} Trim
2	$\overline{I_O}$
3	$-V_S$
4	I_O
5	MSB B1
6	B2
7	B3
8	B4
9	B5
10	B6
11	B7
12	B8
13	B9
14	B10 LSB
15	$+V_S$
16	$V_{REF(+)}$
17	$V_{REF(-)}$
18	Comp

Mask Pattern



Die Size: 94 x 100 mils
Min. Pad Dimensions: 4 x 4 mils

Thermal Characteristics

	Ceramic DIP
Max. Junction Temp.	175°C
Max. P_D T_A < 50°C	1042mW
Therm. Res. θ_{JC}	60°C/W
Therm. Res. θ_{JA}	120°C/W
For T_A > 50°C Derate at	8.38mW per °C

Ordering Information

Part Number	Package	Operating Temperature Range	Nonlinearity
DAC-10FDC	Ceramic	0°C to +70°C	±0.05%
DAC-10GDC	Ceramic	0°C to +70°C	±0.01%
DAC-10BDM	Ceramic	-55°C to +125°C	±0.05%
DAC-10BDM/883B*	Ceramic	-55°C to +125°C	±0.05%
DAC-10CDM	Ceramic	-55°C to +125°C	±0.05%
DAC-10CDM/883B*	Ceramic	-55°C to +125°C	±0.05%

*MIL-STD-883, Level B Processing

Absolute Maximum Ratings

Operating Temperature Range
DAC-10BD, CD ..... -55°C to +125°C
DAC-10FD, GD ..... 0°C to +70°C
Storage Temperature
Range ..... -65°C to +150°C
Lead Soldering
Temperature (60 Sec) ..... +300°C
Supply Voltage ($+V_S$ to $-V_S$) ..... +36V
Logic Inputs ..... $-V_S$ to $-V_S$ plus 36V
V_{LC} ..... $-V_S$ to $+V_S$
Analog Current Outputs ..... $-V_S$ to $+V_S$
Reference Inputs (V_{16} to V_{17}) ..... $-V_S$ to $+V_S$
Reference Input Differential
Voltage (V_{16} to V_{17}) ..... ±18V
Reference Input Current (I_{16}) 2.5mA

Electrical Characteristics ($V_S = \pm 15V$; $I_{REF} = 2.0mA$, $-55°C \leq T_A \leq +125°C$ for DAC-10B, DAC-10C, $0°C \leq T_A \leq +70°C$ for DAC-10F, DAC-10G. Output characteristics apply to both I_O and $\overline{I_O}$ unless otherwise specified.)

Parameters	Test Conditions	DAC-10B/F			DAC-10C/G			Units
		Min	Typ	Max	Min	Typ	Max	
Monotonicity		10			10			Bits
Nonlinearity			.029	.049		.058	.098	% FS
Differential Nonlinearity			.029	.098		.068		% FS
Output Voltage Compliance	Full Scale Current Change < 1 LSB		-5.5 +10			-5.5 +10		V
Gain Temperature Coefficient	See Note		±10	±25		±10	±50	ppm/°C
Full Scale Current	$V_{REF} = 10.000V$ $R_{16} = R_{17} = 5.000k\Omega$	3.968	3.996	4.024	3.936	3.996	4.056	mA
Full Scale Symmetry	$I_{FS} - \overline{I_{FS}}$		0.1	4.0		1.0	4.0	μA
Zero Scale Current			0.01	0.5		0.01	0.5	μA
Reference Input Slew Rate	$R_{EQ} = 200\Omega$, $C_C = 0$		6.0			6.0		mA/μS
Power Supply Sensitivity Positive	$+4.5V \leq +V_S \leq +18V$		0.001	0.01		0.001	0.01	$\%\Delta_{FS}/$
Negative	$-18V \leq -V_S \leq -10V$		0.0012	0.01		0.0012	0.01	$\%\Delta V$
Supply Current Positive	$V_S = \pm 15V$		2.3	4.0		2.3	4.0	mA
Negative	$I_{REF} = 2.0mA$		9.0	15		9.0	15	
Positive	$V_S = +5.0V/-7.5V$;		1.8	4.0		1.8	4.0	
Negative	$I_{REF} = 2.0mA$		5.9	9.0		5.9	9.0	
Power Consumption	$V_S = \pm 15V$ $I_{REF} = 1.0mA$		231	276		231	276	mW
	$V_S = +5.0V/-7.5V$; $I_{REF} = 1.0mA$		85	107		85	107	
Logic Input Levels Low	$V_{LC} = 0$			0.8			0.8	V
High		2.0			2.0			
Logic Input Currents Low	$V_{LC} = 0$; $-5.0V \leq V_{IN} \leq +0.8V$	-10	-5.0		-10	-5.0		μA
High	$+2.0V \leq V_{IN} \leq +18V$		0.001	10		0.001	10	

Note: Guaranteed by Design.

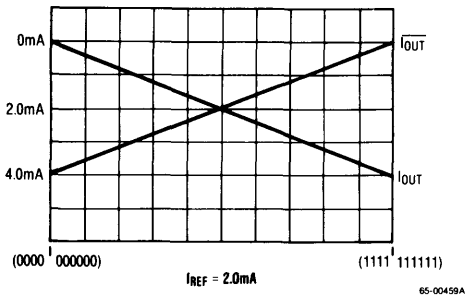
Electrical Characteristics ($V_S = \pm 15V$; $I_{REF} = 2.0mA$; $T_A = +25°C$, unless otherwise noted. Output characteristics apply to both I_O and $\overline{I_O}$.)

Parameters	Test Conditions	DAC-10B/C/F			DAC-10G			Units
		Min	Typ	Max	Min	Typ	Max	
Monotonicity		10			10			Bits
Nonlinearity			.029	.049		.058	.098	% FS
Differential Nonlinearity			.029	.098		.068		% FS
Output Voltage Compliance	Full Scale Current Change < 1 LSB	-5.0	-6/+18	+10	-5.0	-6/+15	+10	V
Full Scale Current	$V_{REF} = 10.000V$, $R_{16} = R_{17} = 5.000k\Omega$	3.978	3.996	4.014	3.956	3.996	4.036	mA
Full Scale Symmetry	$I_{FS} - \overline{I_{FS}}$		0.1	4.0		0.1	4.0	μA
Zero Scale Current			0.01	0.5		0.01	0.5	μA
Settling Time	All Bits Switched ON or OFF Settle to 0.05% of FS See Note		85	135		85	150	nS
Output Capacitance			18			18		pF
Propagation Delay	$R_L = 5.0k\Omega$		50			50		nS

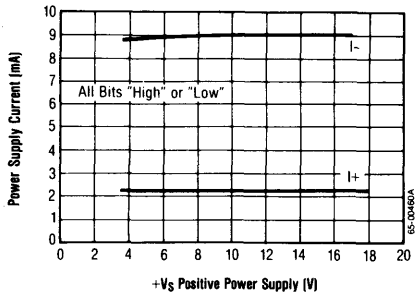
Note: Guaranteed by Design

Typical Performance Characteristics

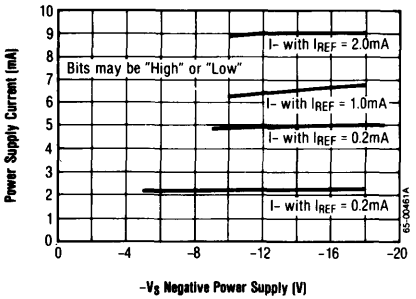
True and Complementary Output Operations



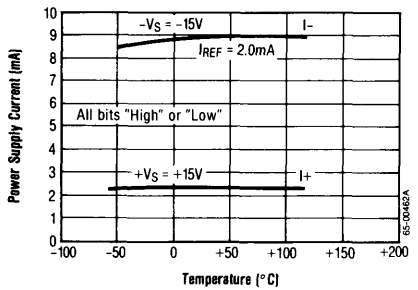
Power Supply Current vs. $+V_S$



Power Supply Current vs. $-V_S$



Power Supply Current vs. Temperature



Propagation and Settling Time

Propagation delays from logic input to analog outputs are typically less than 35nS. Settling times and propagation delays are relatively insensitive to logic input amplitude, power supply voltage or reference current. However, larger reference currents allow for the use of smaller output resistors. This reduces the degradation of speed that occurs due to the DACs output capacitance.

The settling time circuit (Figure 1) yields the optimal settling time that can achieved (85nS). However, in real applications the settling time will be somewhat degraded from ideal. The following applications indicate circuits and settling times for commonly used applications.

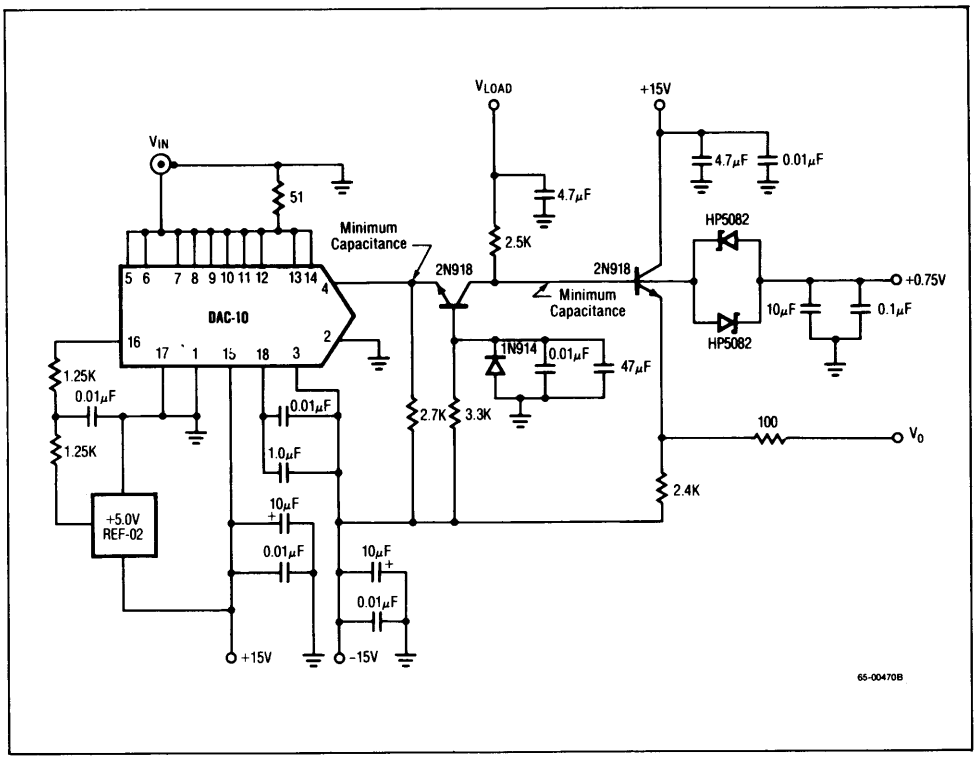


Figure 1. Settling Time Test Fixture

Applications

Output Currents

The analog output currents consist of both true and complemented output sink currents. The sum of the true and complemented currents is always equal to the full scale output current. Full scale output current (I_{FS}) is related to the input reference current by the equation:

$$I_{FS} = 1023/1024 \times 2I_{REF}$$

Input coding of either positive true binary or complementary binary is allowed. The difference of the two output currents is a linear function of the binary input. This feature results in some useful DAC applications where differential outputs are desired, such as differential line driving or digital offset nulling of op amps.

Input Reference

The output current of the DAC-10 is the product of the binary input and the input reference current. The output current is twice the input reference current, defined by the equation:

$$I_O = D/1024 \times 2I_{REF}$$

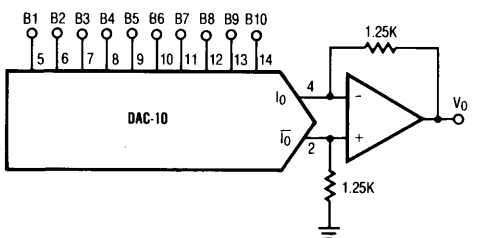
Where I_{REF} is the input reference current into pin 16 and D represents the value of the binary input.

The voltage reference may either be postive or negative. A positive reference is used to force current into pin 16 through bias resistor R16. A negative reference is used to force the voltage at pin 17 negative. The high gain reference amplifier will cause pin 16 to follow pin 17 and again force current into pin 16. The bias resistor is always the resistor in series with pin 16 even when a negative reference is used. Either pin 16 or pin 17 may be offset to accommodate bipolar references.

Noise from the reference supply is reflected into the output. Since the noise output of a reference is directly proportional to bandwidth, the bandwidth must be restricted. A center tapped bias resistor serves as a simple one pole roll-off filter to minimize the effects of wideband noise. A +5V regulated voltage is recommended, with the bias resistor to pin 16 split into two equal resistors having the junction bypassed to ground with a 0.25μF capacitor. A typical +5V bandgap reference (REF-02) puts out a wideband noise voltage of 1 to $2mV_{p-p}$ at the full 10MHz bandwidth. For a multiplying DAC this voltage is transmitted directly to the output such that, for a +5V output system (LSB = 5.0mV) this amount of noise is significant. The simple filter suggested here restricts the noise bandwidth to 1/4RC. For a bias resistor of 1.25kΩ and a bypass capacitor of 0.25μF the noise bandwidth can be reduced to 800Hz and the noise voltage reduced to approximately $80\mu V_{p-p}$, a significant reduction. The +5V TTL supply should **never** be used for a DAC reference.

High Speed Multiplying Applications

For high speed multiplying applications the transient behavior of the input reference amplifier deserves special consideration. The reference amplifier is compensated with a capacitor from pin 18 to the negative supply. The size of this



	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	V_O
Pos Full Scale	1	1	1	1	1	1	1	1	1	1	+4.995
Pos Full Scale -LSB	1	1	1	1	1	1	1	1	1	0	+4.985
(+) Zero Scale	1	0	0	0	0	0	0	0	0	0	+0.005
(-) Zero Scale	0	1	1	1	1	1	1	1	1	1	-0.005
Neg Full Scale +LSB	0	0	0	0	0	0	0	0	0	1	-4.985
Neg Full Scale	0	0	0	0	0	0	0	0	0	0	-4.995

65-00463A

Figure 2. Bipolar Operation

capacitor is a function of the equivalent driving impedance to pin 16. The larger the driving impedance, the larger the capacitor that is required to maintain an adequate phase margin. Although exact mathematical models of the compensated reference amplifier are somewhat involved, it has been established empirically that the compensating capacitor should never be smaller than 15pF per kΩ of driving impedance.

Finally, for a driving point impedance less than 800Ω the compensating capacitor is no longer required. The Pulsed Reference Operation panel shows how to compute driving point impedance R_{EQ}. In general the smaller R_{EQ} the faster the response. The output current will slew at 6.0mA per μS when no compensation capacitor is required.

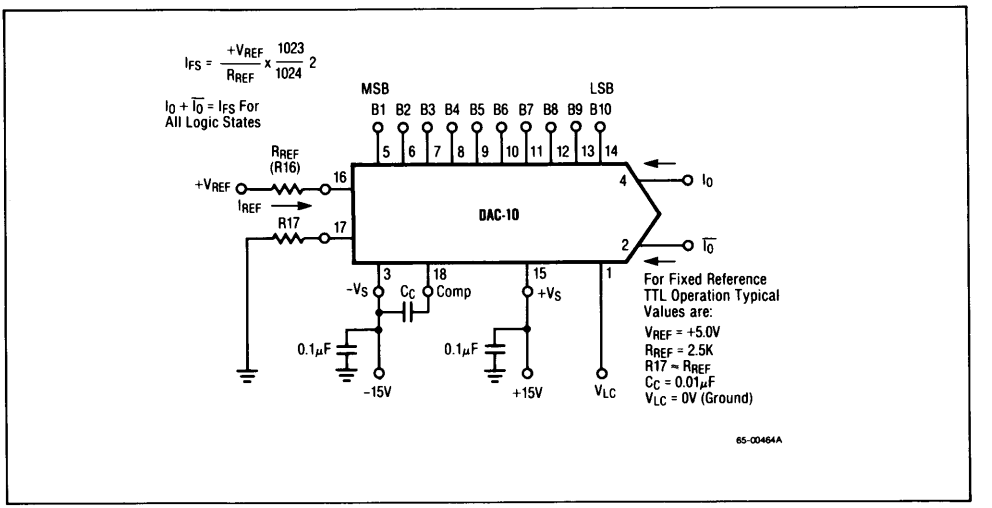


Figure 3. Positive Reference Operation

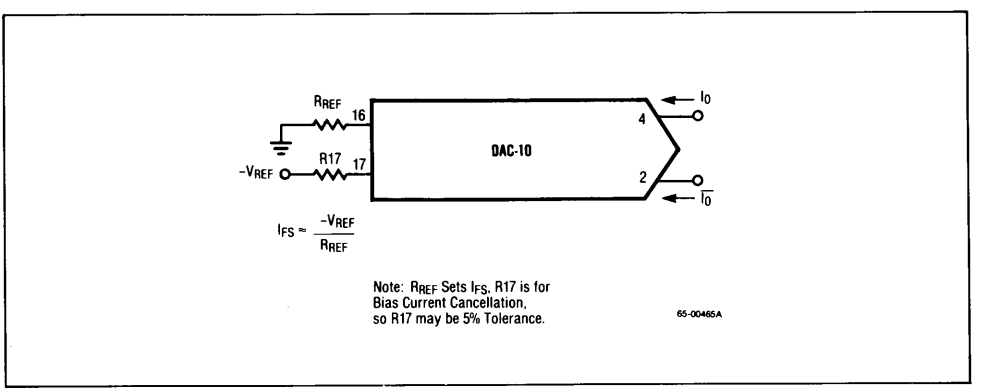
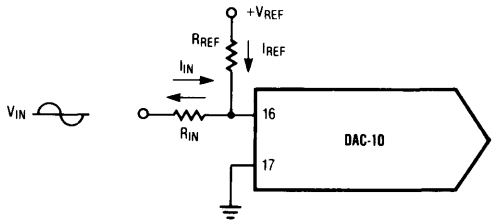


Figure 4. Negative Reference Operation



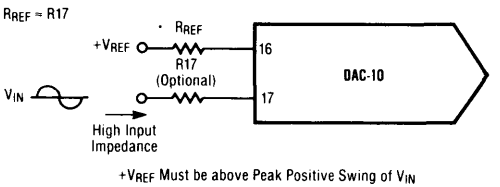


Figure 5. Providing Offsets to Accommodate Bipolar References

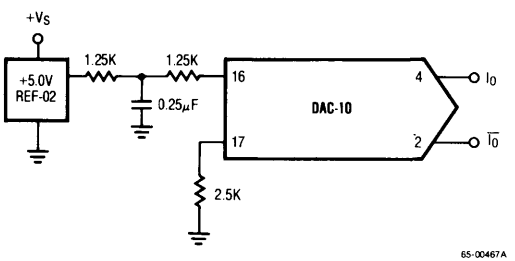


Figure 6. Input Reference Noise Limiting Filter

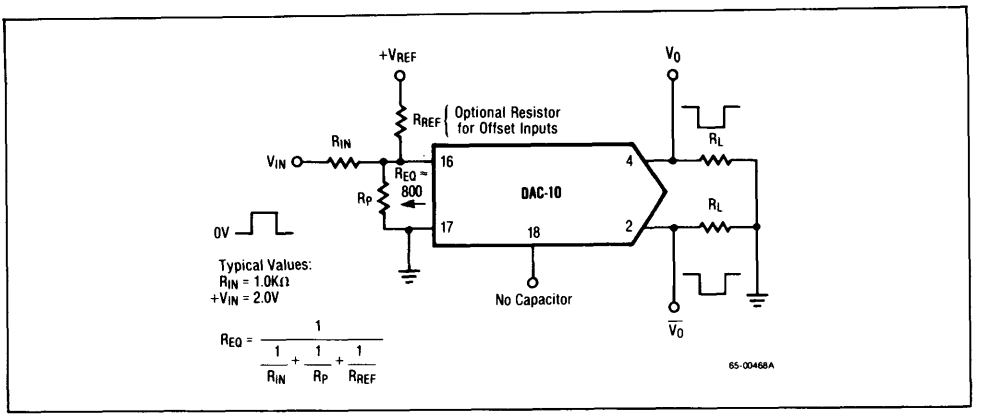


Figure 7. Pulsed Reference Operation

Analog-to-Digital Conversion

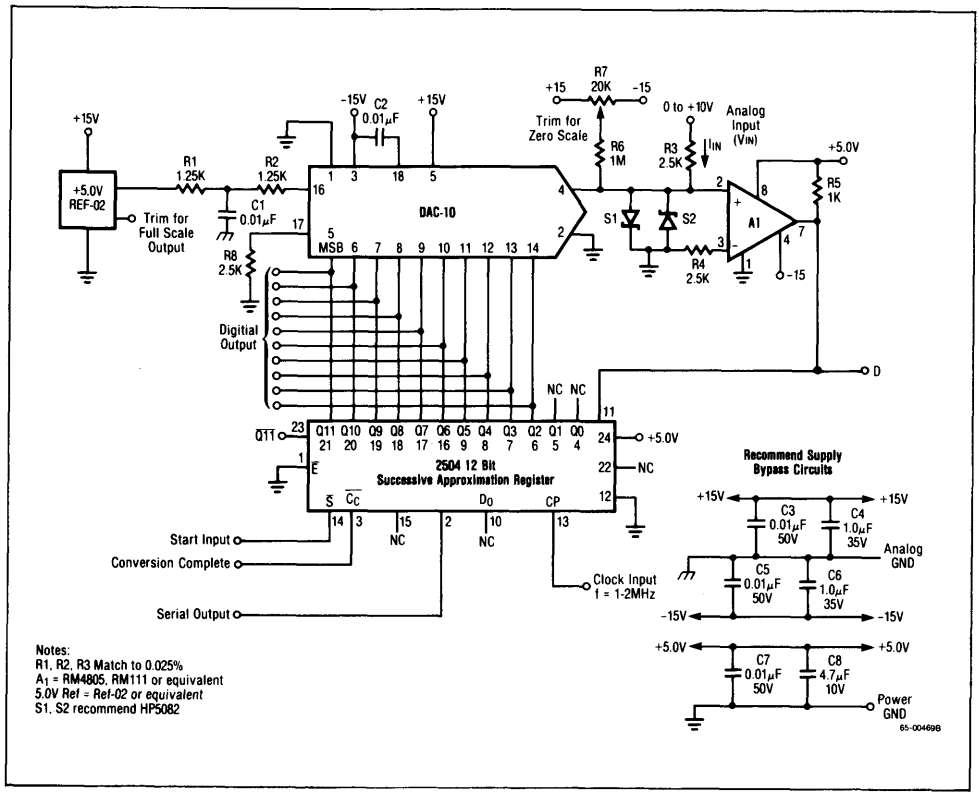
Successive approximation is a logical method of measuring an analog quantity using binary weighted approximation. For example, to measure an unknown weight using a balance scale, the weight is placed on one side of the balance and counterweights are placed on the other side until the scale is balanced. The number of "trials" is made equal to the number of counterweights by starting with the heaviest counterweight first, and either retaining it or rejecting it based on a comparison with the unknown weight. This process is repeated for each weight from heaviest to lightest until all weights have been tried.

By interfacing the DAC-10 with a commercially available successive approximation register (SAR) such as the DM2504 (Figure 8), an analog-to-digital converter (ADC) can be built. The DM2504 register operates as follows.

The register is reset by holding the $\overline{S}$ (Start) input low during a clock (CP) low-to-high transition. After $\overline{S}$ is brought back high, the MSB output (Q11) will be set low and all the remaining register outputs (Q10 - Q12) will be set high, providing a trial binary number for the DAC. This binary number (0111111111) causes the DAC to generate an output current (I_O) which is one half of the full scale output.

I_O is constantly being compared to a current I_{IN}. I_{IN} is generated by the analog input voltage ($I_{IN} = V_{IN}/R_3$). If the first trial number generates an I_O greater than I_{IN}, then the comparator sends a logical zero signal to the SAR. On the next clock low-to-high transition the logical zero is latched into the MSB (Q11) output of the SAR. If the first trial number generates an I_O less than I_{IN}, then the comparator output will be high, and a logical one will be latched into the MSB output. This is a decision making process where the circuit determines, bit by bit, whether the code present on the SAR digital outputs is proportional to the input voltage. After the MSB is latched, the circuit will go through the same decision making process for the next most significant bit, deciding whether it should be latched high or low. The process is repeated successively for each bit until the least significant bit is latched. At this time control logic in the SAR will stop the conversion and signal completion by bringing the QCC output low. The circuit will then stay in its latched output state until conversion is again initiated by the start input.

Since a bit is decided for each clock low to high transition the maximum time needed for a complete conversion will be equal to twelve clock cycles. As each bit is generated it is also latched into the D_O output so that D_O can be used as a serial output. The last two bits will be invalid data because this system uses a 12 bit SAR and a 10 bit DAC.



Notes:
R1, R2, R3 Match to 0.025%
A_1 = RM4805, RM111 or equivalent
5.0V Ref = Ref-02 or equivalent
S1, S2 recommend HP5082

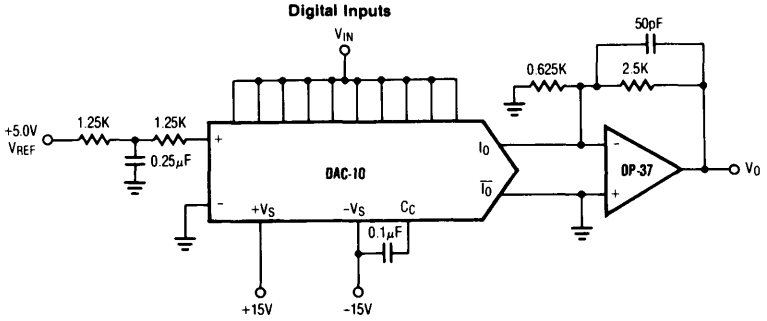
Figure 8. 10-Bit Successive Approximation A/D Converter

Output Voltage Compliance

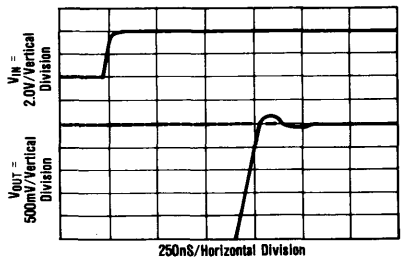
The DAC-10 will operate over a wide range of supply voltages. However, the minimum negative output voltage is a direct function of the full scale output current and the negative supply voltage. Output voltage compliance range is the maximum voltage change from which the $\overline{I_O}$ and I_O can sink current. The minimum negative output voltage (V_S-) can be computed by the equation:

$$V_{OC}- = (-V_S) + 0.5I_{FS} + 2.6V$$

where V_{OC}- is in volts and full scale current I_{FS} is in milliamps. For instance V_{OC}- will be equal to -10.4V when $-V_S$ = -15V and I_{FS} = 4mA. V_{OC} (positive or negative) does not vary significantly over temperature. The maximum positive output voltage (V_{OC}+) has no theoretical limitations except for device breakdown phenomena. For $-V_S$ = -15V, I_{FS} = 4mA, V_{OC} is ±10V. The full scale current will typically change less than 1 LSB over this output range.



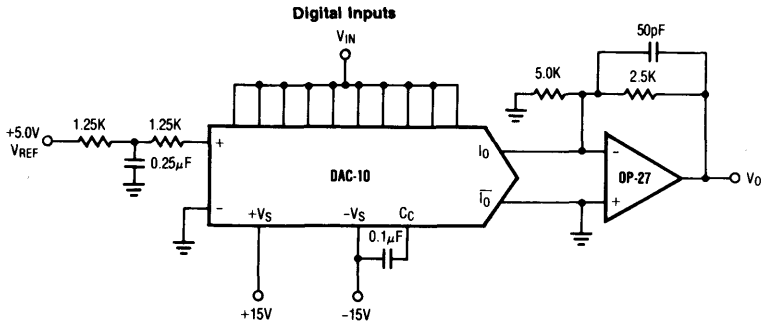
DAC-10/OP-37 Settling Time

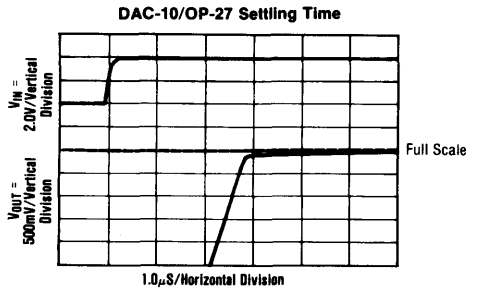


OP-37	F.S. Settling Time (0V to 10V)
0.05% FS	1080nS
0.1% FS	1000nS
0.2% FS	920nS

65-00471B

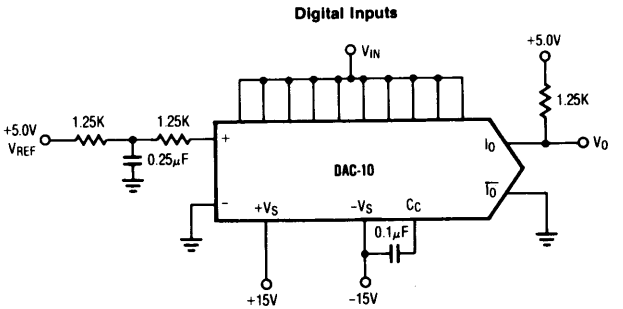
Figure 9. Settling Time Using OP-37



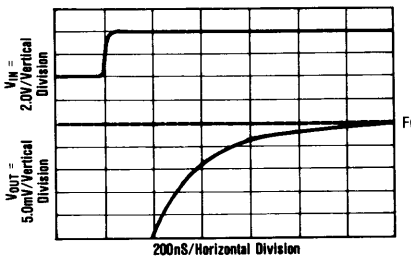


OP-27	F.S. Settling Time (0V to 10V)
0.05% FS	3.0μS
0.1% FS	2.85μS
0.2% FS	2.8μS

Figure 10. Settling Time Using OP-27



DAC-10 with 1.25KΩ Resistive Output Settling Time



1.25KΩ Resistor	F.S. Settling Time (5.0V to 5.0mV)
0.05% FS	450nS
0.1% FS	320nS
0.2% FS	240nS

65-00474B

Figure 11. Settling Time Using 1.25kΩ Resistor Output

Logic Inputs

By programming the V_{LC} pin the DAC-10 can be made to interface with most logic families. The logic threshold voltage is approximately +1.4V above V_{LC}. Thus when V_{LC} = 0 the DAC-10 will interface with TTL logic; for other logic families V_{LC} must be programmed accordingly. Note that V_{LC} must be obtained from a low impedance source. Low impedance can be provided by a 0.1μF capacitor bypass (see Figure 12).

Output Glitches

The DAC-10 is designed for minimal output glitches. However, a further reduction of output glitches is possible, at a slight sacrifice in settling time, by installing small capacitors at the $I_O/\overline{I_O}$ outputs.

Full Scale Adjustment

Full scale trimming is sometimes required to compensate for resistor or voltage reference tolerances. If a potentiometer is used in series with pin 16 the performance of the DAC may be degraded by the temperature coefficient of the potentiometer. A preferred method of trimming is to use the potentiometer as a voltage divider to bias pin 17. With this method the temperature coefficient of the potentiometer has little effect on the circuit since I_{REF} expands on the tracking of the two resistor halves rather than the absolute value (see Figure 13).

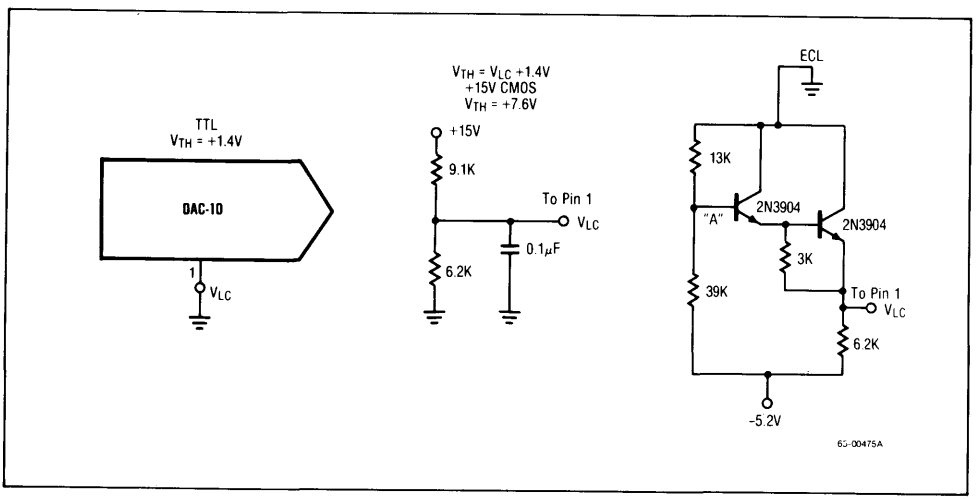


Figure 12. Interfacing With Various Logic Families

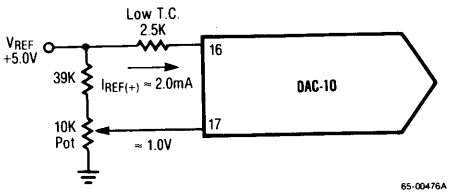
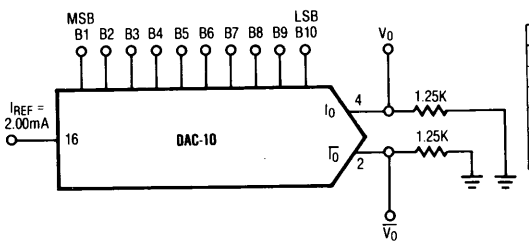


Figure 13. Recommended Full Scale Adjustment Circuit

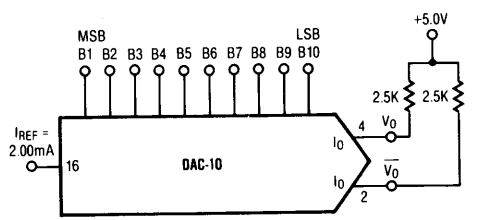
Basic Operation

Resistive terminations can be used to demonstrate basic operation of the DAC-10.



	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	I_0mA	$\overline{I_0}$mA	V_0	$\overline{V_0}$
Full Scale	1	1	1	1	1	1	1	1	1	1	3.996	0.000	-4.995	-0.000
Half Scale +LSB	1	0	0	0	0	0	0	0	0	1	2.004	1.992	-2.505	-2.490
Half Scale	1	0	0	0	0	0	0	0	0	0	2.000	1.996	-2.500	-2.495
Half Scale -LSB	0	1	1	1	1	1	1	1	1	1	1.996	2.000	-2.495	-2.500
Zero Scale +LSB	0	0	0	0	0	0	0	0	0	1	0.004	3.992	-0.005	-4.990
Zero Scale	0	0	0	0	0	0	0	0	0	0	0.000	3.996	-0.000	-4.995

Figure 14. Basic Unipolar Negative Operation

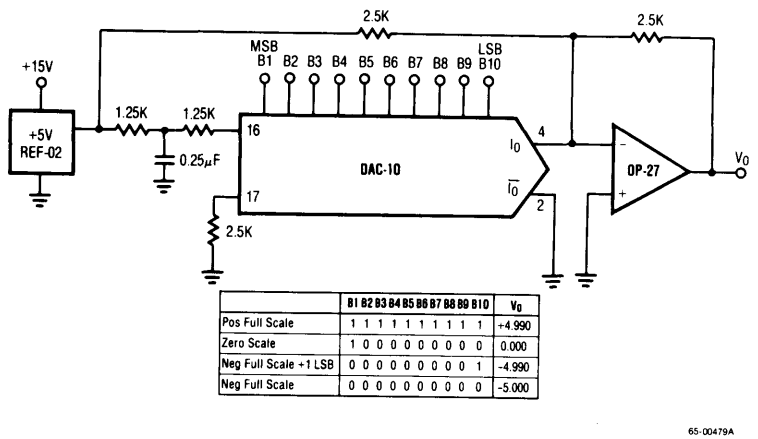


	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	V_0	$\overline{V_0}$
Pos Full Scale	1	1	1	1	1	1	1	1	1	1	-4.990	+5.000
Pos Full Scale -LSB	1	1	1	1	1	1	1	1	1	0	-4.980	+4.990
Zero Scale +LSB	1	0	0	0	0	0	0	0	0	1	-0.010	+0.020
Zero Scale	1	0	0	0	0	0	0	0	0	0	0.000	+0.010
Zero Scale -LSB	0	1	1	1	1	1	1	1	1	1	+0.010	0.000
Neg Full Scale +LSB	0	0	0	0	0	0	0	0	0	1	+4.990	-4.980
Neg Full Scale	0	0	0	0	0	0	0	0	0	0	+5.000	-4.990

Figure 15. Basic Bipolar Output Operation

Offset Binary Operation

By feeding the inverting terminal of the output op amp a current equal to I_{REF} offset binary operation may be implemented.



	B1 B2 B3 B4 B5 B6 B7 B8 B9 B10	V_O
Pos Full Scale	1 1 1 1 1 1 1 1 1 1	+4.990
Zero Scale	1 0 0 0 0 0 0 0 0 0	0.000
Neg Full Scale +1 LSB	0 0 0 0 0 0 0 0 0 1	-4.990
Neg Full Scale	0 0 0 0 0 0 0 0 0 0	-5.000

Figure 16. Offset Binary Operation

Raytheon

Complete High Speed 12-Bit Monolithic D/A Converter

DAC-4565

Features

- Nonlinearity 1/2 LSB — 0.012%
- Differential nonlinearity — 0.012% (13 bits)
- Settles to 1/2 LSB in 200nS
- On-chip bandgap voltage reference
- Linearity guaranteed over temperature
- Low power: 225mW including reference
- Direct interface to all major logic families
- Includes trimmed application resistors

Highlights

- The DAC-4565 is a monolithic 12-Bit DAC that has on-board a self-contained voltage reference plus application resistors.
- The device incorporates interdigitizing of the elements forming the currents of the 3 MSBs of the DAC. Interdigitizing minimizes the effects of thin film sputtering, thermal, and diffusion gradients in the most critical portions of the design. Excellent linearity distributions are achieved prior to trimming, thus ensuring optimal stability of nonlinearity over temperature, as well as ensuring stability versus time.
- The thin film resistors have a trim tab which is distant from the main body of the resistor. This resistor geometry ensures near perfect nonlinearity after trim, and this geometry also reduces damage due to laser trimming.
- The internal reference is laser trimmed to 10.00 Volts with a ±1.0% maximum error. The reference voltage is available externally and can supply 10mA beyond that required for the reference and bipolar offset resistors.
- The DAC-4565 contains SiCr thin film application resistors which can be used with either an external op amp, creating a precision voltage output DAC, or as input resistors for a successive approximation A/D converter. The resistors are inherently matched and are laser trimmed to guarantee minimum full scale and bipolar offset errors.
- The DAC-4565S grade guarantees linearity and monotonicity over the -55° C to +125° C range and is available fully processed to MIL-STD-883, Level B.

Description

The DAC-4565 is a fast 12-bit digital-to-analog converter. Inside the 24 pin DIP package are all of the circuit functions required for a complete DAC: a stable bandgap voltage reference, a reference amplifier and resistors, twelve laser trimmed binary weighted current sources, twelve high speed precision current steering switches, and laser trimmed span and bipolar offset application resistors.

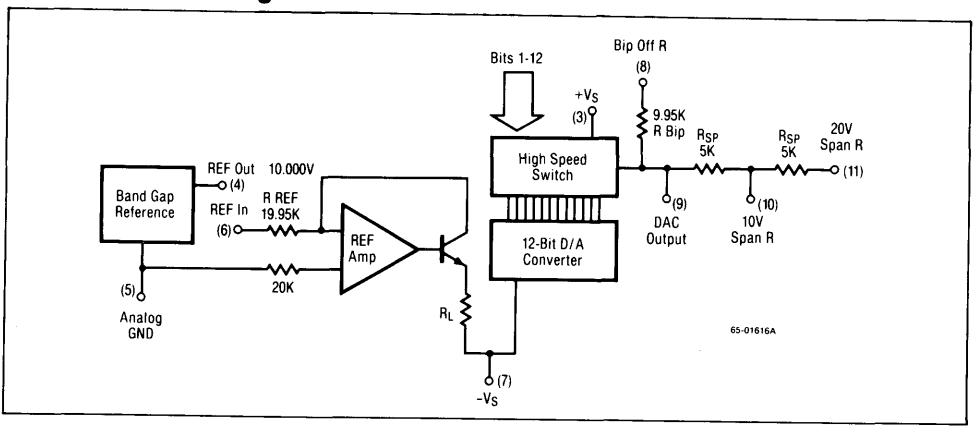
The high performance and flexibility of the DAC-4565 are achieved through circuit design and layout, SiCr thin film resistor processing, and interactive computer-controlled laser trimming. The DAC-4565 settles to 1/2 LSB in 200nS typically, with a maximum settling time of 400nS. Accuracy is specified at a **maximum** of 1/2 LSB for all grades.

High speed and accuracy coupled with inherent high output impedance make the DAC-4565 the ideal DAC for high speed display drivers, high speed control systems, and in conjunction with the RC4805 high speed latching comparator in analog-to-digital converters.

The bandgap voltage reference is laser trimmed to optimize both temperature drift and absolute output voltage. The current sourcing capability of the DAC-4565 reference (10mA typ) allows the reference to drive peripheral circuit elements in addition to the DAC. Typical reference drift is better than 15ppm/° C (S and J grade).

The DAC-4565 is available in three performance grades. The DAC-4565J and DAC-4565D grades are specified over 0° C to +70° C, while the DAC-4565S grade is specified over the -55° C to +125° C temperature range.

Functional Block Diagram



Absolute Maximum Rating

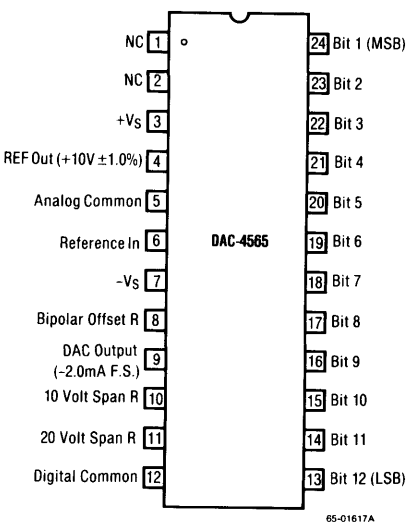
Supply Voltages ..... ±18V
Logic Inputs ..... -1.0V to +18V
Analog Common to
Digital Common ..... ±1.0V
Voltage on DAC
Output (Pin 9) ..... -3.0V to +18V
Reference Input to
Analog Common ..... ±12V
Bipolar Offset to
Analog Common ..... ±12V
10V Span R to Analog Common ..... ±12V
20V Span R to Analog Common ..... ±24V
Ref Out ..... Indefinite Short to Either Common, Momentary Short to +V_S
Lead Soldering Temperature
(60 Sec) ..... +300°C

Thermal Characteristics

	24-Lead Side-Brazed DIP
Max. Junction Temp.	175°C
Max. P_D T_A < 50°C	1042mW
Therm. Res. θ_{JC}	60°C/W
Therm. Res. θ_{JA}	120°C/W
For T_A> 50°C Derate at	8.38mW per °C

Connection Information

24-Lead
Ceramic Side-Brazed
Dual In-Line Package
(Top View)



Complete High Speed 12-Bit Monolithic D/A Converter

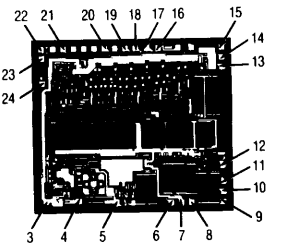
DAC-4565

Ordering Information

Part Number	Package	Operating Temperature Range
DAC-4565JDC	Side-brazed	0°C to +70°C
DAC-4565DDC	Side-brazed	0°C to +70°C
DAC-4565SDM	Side-brazed	-55°C to +125°C
DAC-4565SDM/883B*	Side-brazed	-55°C to +125°C

*MIL-STD-883, Level B Processing

Mask Pattern



Die Size: 116 x 133 mils
Min. Pad Dimensions: 4 x 4 mils

Electrical Characteristics (T_A = +25°C, $+V_S$ = +15V, $-V_S$ = -15V, unless otherwise noted)

Parameter	Test Conditions	DAC-4565S/J			DAC-4565D			Units
		Min	Typ	Max	Min	Typ	Max	
Resolution		12	12	12	12	12	12	Bits
Monotonicity		12	12	12	12	12	12	Bits
Nonlinearity			±.006	±.012		±.006	±.012	%FS
Differential Nonlinearity	Deviation from ideal step size		±.007	±.018		±.007	±.018	%FS
Full Scale Current	Unipolar (All bits on) Internal Reference (Full temperature)	-1.6	-2.0-	-2.4	-1.6	-2.0	-2.4	mA
	Bipolar (Figure 3 R_2 = 50Ω fixed) All bits on or off (Full temperature)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	
Output Resistance		1.0	10		1.0	10		MΩ
Output Voltage Compliance	R_0 > 10MΩ typ (Full temperature)	-1.5		+10	-1.5		+10	V
Output Capacitance			25			25		pF
Offset Unipolar Zero Scale			0.001	0.0025		0.002	0.01	% of F.S.
Bipolar	(Figure 3 R_2 = 50Ω Fixed)		0.05	0.15		0.10	0.30	
Settling Time to 1/2 LSB	All bits on to off or off to on		200	400		200	400	nS

Electrical Characteristics (Continued)

(T_A = +25°C, $+V_S$ = +15V, $-V_S$ = -15V, unless otherwise noted)

Parameter	Test Conditions	DAC-4565S/J			DAC-4565D			Units
		Min	Typ	Max	Min	Typ	Max	
Full Scale Transition Rise Time	10% to 90% Plus Propagation Delay		40			40		nS
Fall Time	90% to 10% Plus Propagation Delay		40			40		
Logic Input Levels Logic "0"	(Full temperature)			0.8			0.8	V
Logic "1"	(Full temperature)	2.0			2.0			
Logic Input Current	V_{IN} = 0V to 18V (Full temperature)			40			40	μA
Reference Input Current	V_{REF} = 10.000V	0.4	0.5	0.6	0.4	0.5	0.6	mA
Input Resistance		15	20	25	15	20	25	kΩ
Supply Voltage	(Full temperature)	±13.5	±15	±16.5	±13.5	±15	±16.5	V
Supply Current	$+V_S$ = +13.5 to +16.5		3.0	5.0		3.0	5.0	mA
	$-V_S$ = -13.5 to -16.5		-10	-18		-10	-18	
Power Consumption			195	345		195	345	mW
Power Supply Sensitivity	$+V_S$ = +15V, ±10%		.0003	.001		.0007	.002	%FS/%
	$-V_S$ = −15V, ±10%		.0015	.0025		.002	.0035	
Reference Output Voltage		9.90	10	10.1	9.7	10	10.3	V
Reference Output Current	(Available for External Loads)	5.0	10		5.0	10		mA
External Adjustments	(Gain Error with Fixed 50Ω Resistor For R_2 (Figure 1)		±0.1	±0.25		±0.1	±0.50	% of F.S.
Bipolar Zero Error with Fixed 50Ω Resistor for R1	(Figure 2)		±0.05	±0.15		±0.05	±1.0	% of F.S.
Gain Adjustment Range		±0.25			±0.50			% of F.S.
Bipolar Zero Adjustment Range		±0.15			±0.3			% of F.S.
Programmable Output Range	(See Figures 1, 2, 3, 4)	0		5.0	0		5.0	V
		-2.5		+2.5	-2.5		+2.5	
		0		10	0		10	
		-5.0		+5.0	-5.0		+5.0	
		-10		+10	-10		+10	

Electrical Characteristics (Continued)

(DAC-4565 = -55°C to +125°C, DAC-4565J/D = 0°C to +70°C, unless otherwise noted)

Parameter	Test Conditions	DAC-4565S/J			DAC-4565D			Units
		Min	Typ	Max	Min	Typ	Max	
Resolution		12	12	12	12	12	12	Bits
Monotonicity		12	12	12	12	12	12	Bits
Nonlinearity			±.012	±.018		±.012	±.018	% FS
Differential Nonlinearity	Deviation from ideal Step size	Monotonicity Guaranteed						
Temperature Coefficients Unipolar Zero			1.0	2.0		1.0	2.0	ppm/°C
Bipolar Zero			5.0	10		10		ppm/°C
Differential Nonlinearity			2.0			2.0		ppm/°C
Gain with Internal Reference	Full Scale		15	30		40		ppm/°C
with External Reference			5.0			5.0	40	ppm/°C
Supply Current	$+V_S$ = +13.5V to +16.5V		4.0	7.0		4.0	7.0	mA
	$-V_S$ = -13.5V to -16.5V		-12	-18		-12	-18	mA

Connecting the DAC-4565 for Buffered Voltage Output

The standard current to voltage conversion connections using an operational amplifier are shown in Figure 1. If a low offset voltage operational amplifier (OP-07, OP-27, OP-37) is used, excellent performance can be obtained in most applications without trimming. If a fixed 50Ω resistor is substituted for the 100Ω trimmer of Figure 1, unipolar zero will be typically much less than ±1/2 LSB and full scale accuracy will be within 0.1% (0.25% max). Substituting a 50Ω resistor for the 100Ω bipolar offset trimmer (R1) of Figure 2 will give a bipolar zero error typically within ±2.0 LSB.

The configuration of Figure 1 will provide a unipolar 0V to +10V output range. In this mode, the bipolar terminal, pin 8, should be grounded if not used for trimming.

Unipolar Configurations

Step 1 — Gain Adjust

Turn all bits on and adjust 100Ω gain trimmer R1 until the output is +9.9976 (full scale should be adjusted to 1 LSB less than +10.000V). If a +10.2375V full scale is desired (exactly 2.5mV/bit), insert a 120Ω resistor in series with the gain resistor at pin 10 to the op amp output.

In most cases a zero trim is not needed, due to the extremely low zero scale output current. Pin 8 should be connected to pin 9 for unipolar operation.

Bipolar Configurations

These configurations will yield ±5.0V, ±10V, or ±2.5V, with positive full scale occurring with all bits on (all 1's).

Step 1 — Offset Adjust

Turn on all bits and adjust trimmer R2 to give a reading of +4.9976, +9.9951, or +2.4998V depending upon the range.

Step 2 — Gain Adjust

Turn on all bits and adjust trimmer R2 to give a reading of +4.9976, +9.9951, or +2.4988V depending upon the range.

If a precision op amp such as the OP-07, OP-27, or OP-37 is used no separate trimming of the operational amplifier is required or recommended.

0V to +5.0V Range

A 0V to +5V output can be achieved by modifying the configuration of Figure 1. Tie pin 11 to pin 9 rather than to pin 10 and adjust full scale to +4.9988V.

Internal/External Reference Use

The DAC-4565 has an internal bandgap voltage reference which is trimmed for both temperature coefficient and absolute accuracy. The reference is buffered with an internal operational amplifier and is capable of driving a minimum of 5.0mA in addition to the 0.5mA into REF_{IN} and 1.0mA into Bipolar Offset for the DAC. The reference is typically trimmed to ±0.2% but specified to 1.0% (J, S grades) max error. Testing and specifying of absolute unipolar and bipolar full scale is done using the internal reference. For noise performance of the reference see Figure 6.

Digital Input Considerations

The DAC-4565 uses a positive true straight binary code for unipolar outputs (all 1's give full scale output) and an offset binary code for bipolar output ranges. In the bipolar mode, all 0's give -F.S., with only the MSB on give 0.00V, and with all 1's, +F.S. is achieved.

The threshold of the digital input circuitry is set at +1.4V independent of supply voltage. The bit lines are compatible with TTL, DTL, CMOS, and unbuffered CMOS.

Application of Analog and Digital Commons

The DAC-4565 separates analog and digital grounds to optimize accuracy and noise. 200mV difference between the two grounds can be tolerated without degradation in performance.

Output Voltage Compliance

The Raytheon DAC-4565 has a minimum output voltage compliance range of -1.5V to +10V and is independent of both the positive and negative supply voltages. The output can be modeled as a 25pF capacitance shunted by a 10MΩ resistance across the output current source to ground. This is a dramatic improvement over competitive DAC-565 designs which have an 8kΩ output impedance. The DAC-4565's output current varies insignificantly as a function of output voltage, allowing direct conversion to voltage by an external resistor in many applications.

More significantly, the errors introduced by the input errors of the external output operational amplifier are not magnified by a low output impedance. The output system error from the op amp is equal to:

$$(V_{ERR} \text{ in op amp}) \left(\frac{R_{SPAN} + R_{IN}}{R_{IN}}\right)$$

and defaults to only the inherent input errors of the op amp.

Settling Time

The internally compensated reference amplifier and differential bit switch are optimized for fast settling operation. Worst case settling time occurs when all bits are switched and is specified as 400nS maximum. Note: The settling time specification is for the output current, not for a voltage. When using an external op amp as a current to voltage converter, the settling time will usually be dominated by the speed performance of the operational amplifier. When using the DAC in a successive approximation A/D application, care in the selection of the comparator is critical in determining accuracy and speed. Raytheon recommends the use of the RM4805 comparator to optimize A/D performance. Please refer to the 4805 application notes for further details on speed and accuracy characteristics of successive approximation A/D converters.

Direct Unbuffered Voltage Output for Cable Driving

The high output impedance and compliance range allow for direct current to voltage conversion using the bipolar and span resistors. The circuit configurations of Figure 5 yield complementary unipolar coding (+10V to 0V) as well as ±1.0V bipolar coding. The 10MΩ output impedance of the Raytheon DAC-4565 allows for direct current to voltage conversion without any degradation of linearity performance.

12-Bit Analog-to-Digital Converter

Figure 7 shows an application of the DAC-4565 coupled with the 4805 comparator to make a successive approximation 12-bit analog-to-digital converter. The SAR selected is the AM2504. Latched output capability is provided by the 25LS374. Conversion time with the 1K summing mode resistance should be set by the clock at 13μS.

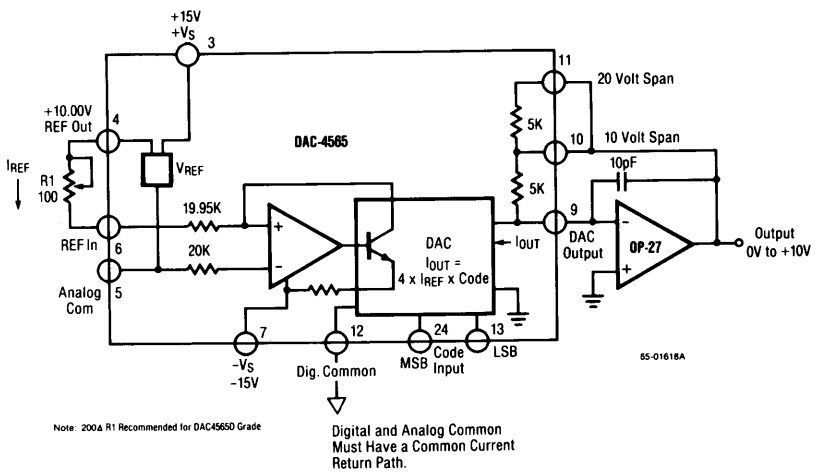


Figure 1. 0V to +10V Unipolar Voltage Output

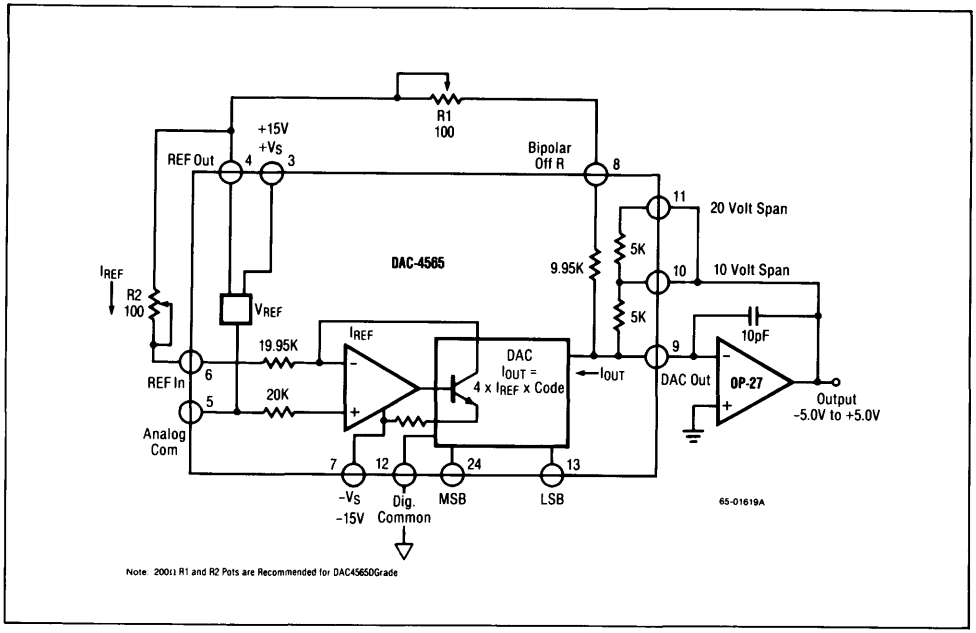


Figure 2. ±5.0V Bipolar Voltage Output

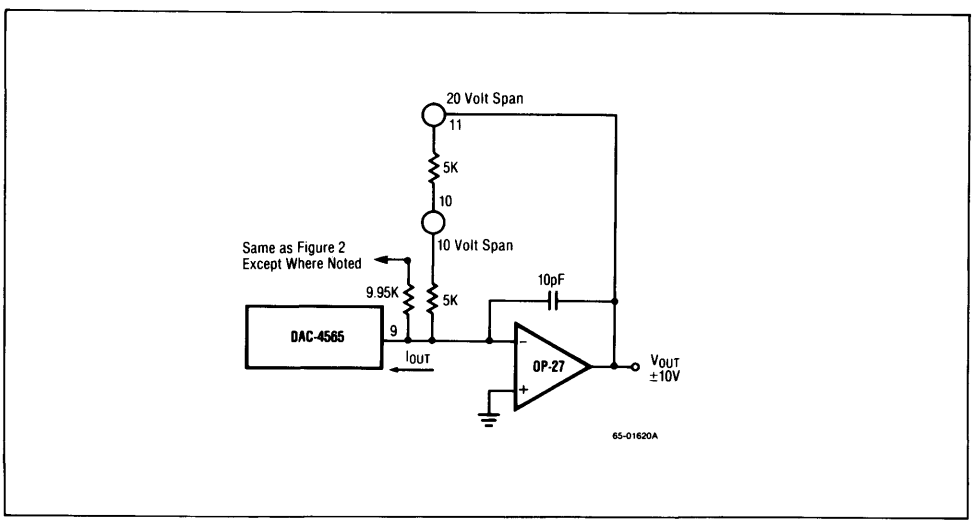


Figure 3. ±10V Bipolar Voltage Output

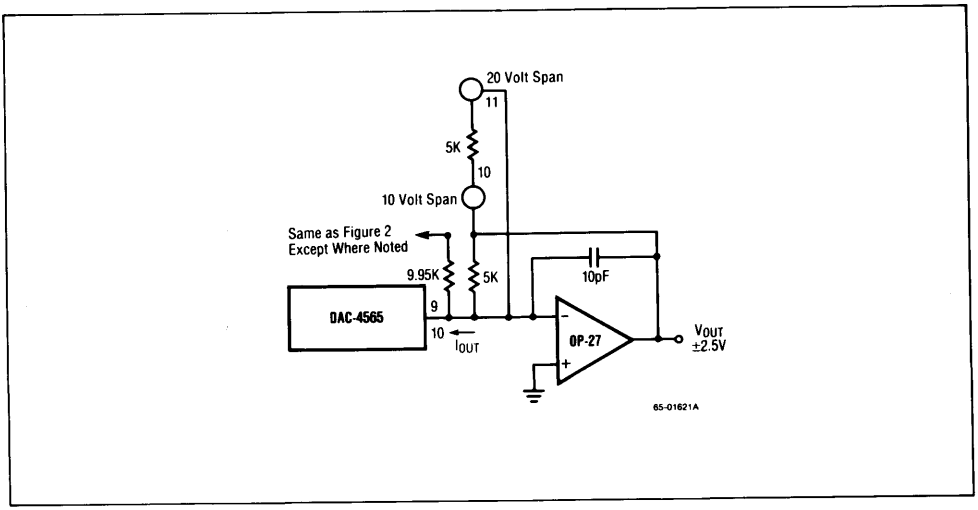


Figure 4. ±2.5V Bipolar Voltage Output

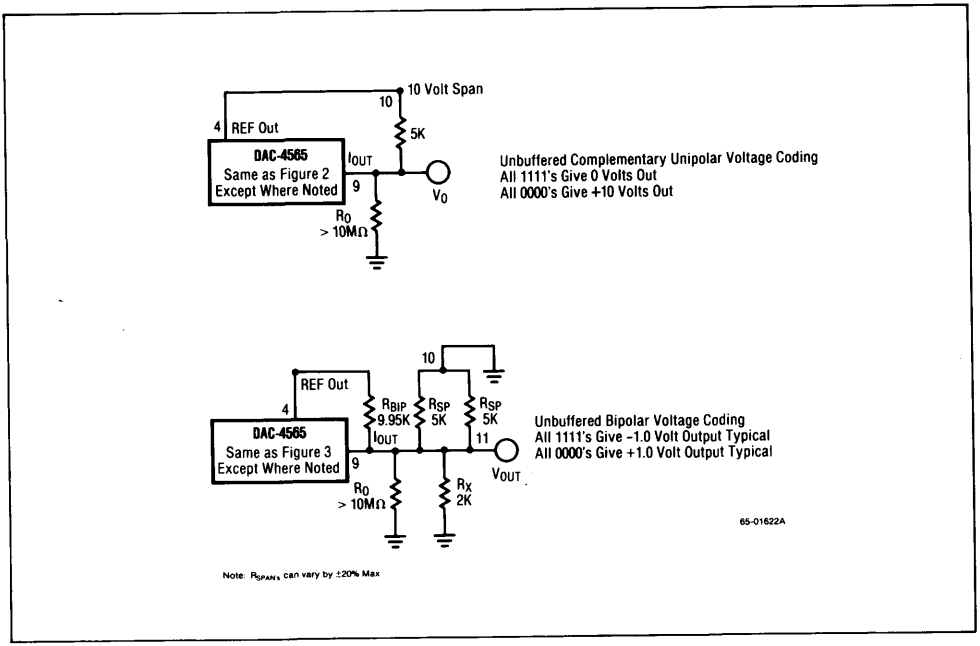


Figure 5. Unbuffered Voltage Output Configurations

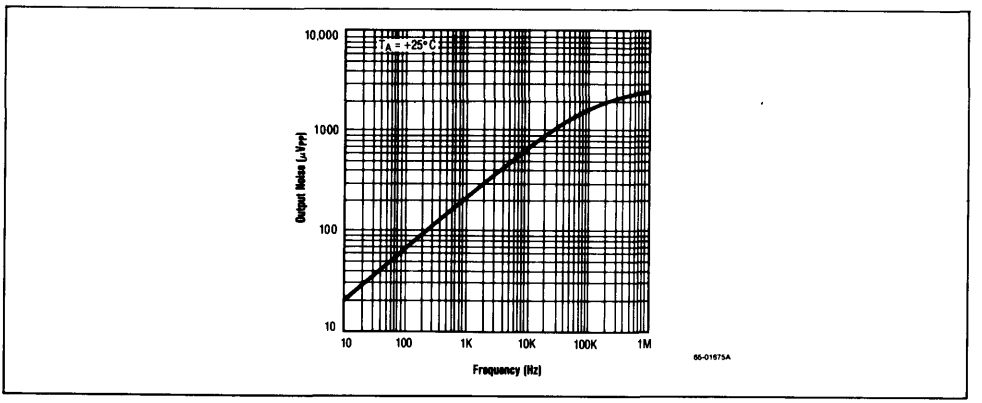


Figure 6. Output Wideband Noise vs Bandwidth (0.1Hz to Frequency Indicated)

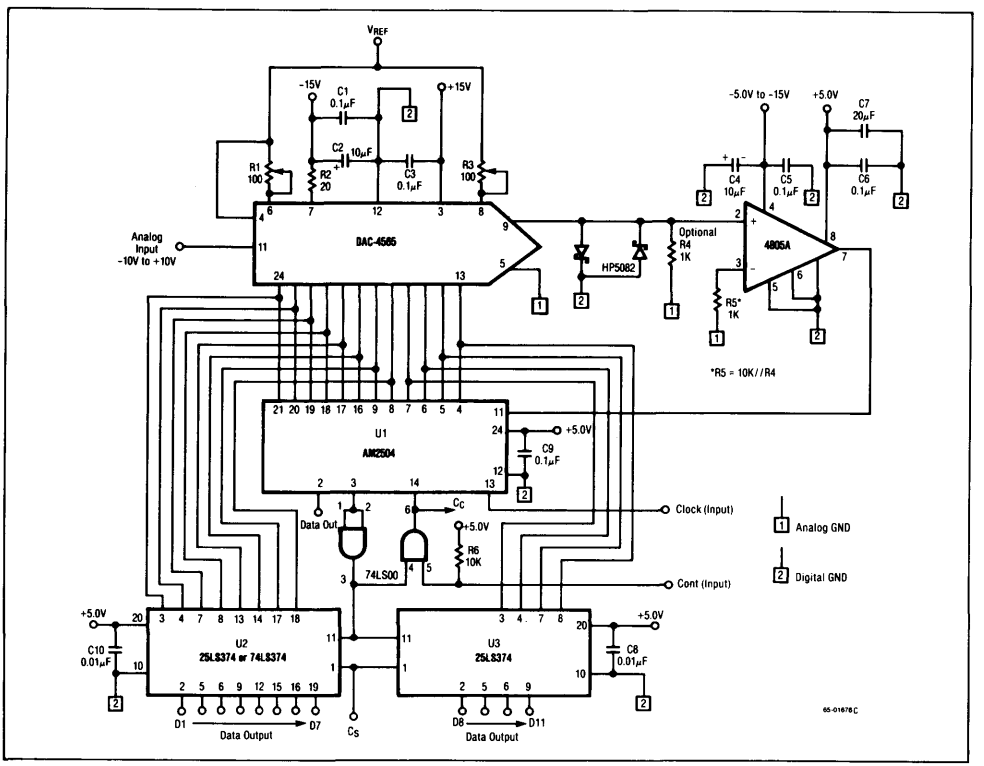


Figure 7. 12-Bit Analog-to-Digital Converter

12-Bit D/A Converter With Microprocessor Interface Latches

Raytheon **DAC-4881**

Features

- Complete —
  High speed op amp for voltage output
  Precision trimmed thin film resistors
  Voltage reference — bandgap, 15ppm/°C
  Input latches for microprocessor compatibility
  Internal AC compensation
- Accurate —
  Nonlinearity — ±1/2 LSB over temp. range
  Monotonic — differential nonlinearity ±1/2 LSB over temperature range
- High speed —
  Settling time — 200nS (current output)
  Settling time — 2μS (voltage output)
- Versatile —
  High compliance, complementary current outputs
  Input codes — binary, complementary binary, offset binary, complementary offset binary
  Voltage output ranges — 0 to +10V, 0 to +5V, ±2.5V, ±5V, ±10V
  Direct interface to major logic families
  Direct interface to 8- and 16-bit busses
  Operates with ±12V to ±15V supplies
  Low power dissipation — 330mW
- Monolithic
- Metal/ceramic package
- 883B processing available

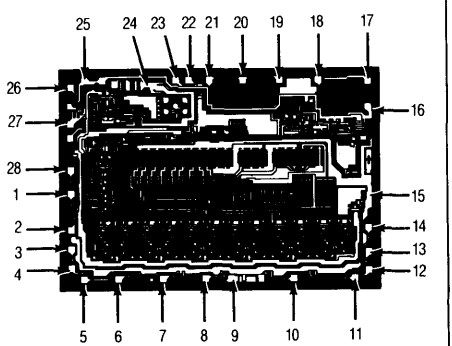
Description

Raytheon's DAC-4881 is a "complete" 12-bit digital-to-analog converter. All of the functions needed for a D/A conversion system have been included on a single chip: a precision 12-bit D/A converter (laser trimmed to .005% non-linearity), a bandgap voltage reference (15ppm/°C drift), a high speed, high accuracy current-to-voltage conversion amplifier (2μS settling time, 200μV offset error), laser trimmed temperature tracking application resistors, and microprocessor interface latches (50nS logic time).

The heart of the device is a 12-bit interdigitized laser trimmed resistor ladder network. The DAC is supported by a bandgap reference derived from the REF-01 Series 10V Voltage Reference, by a high speed interface amplifier which uses slew enhancement to increase speed without degrading accuracy, and by a switch and latch circuit (single buffered, not double buffered, to improve data throughput rates) which are integrated as a cell to improve microprocessor interface time while simultaneously improving the die size. This high level of integration and performance makes the DAC-4881 an ideal choice for both microprocessor interface applications as well as 12-bit high performance applications. For 8- and 10-bit applications, please refer to the DAC-4882 data sheet.

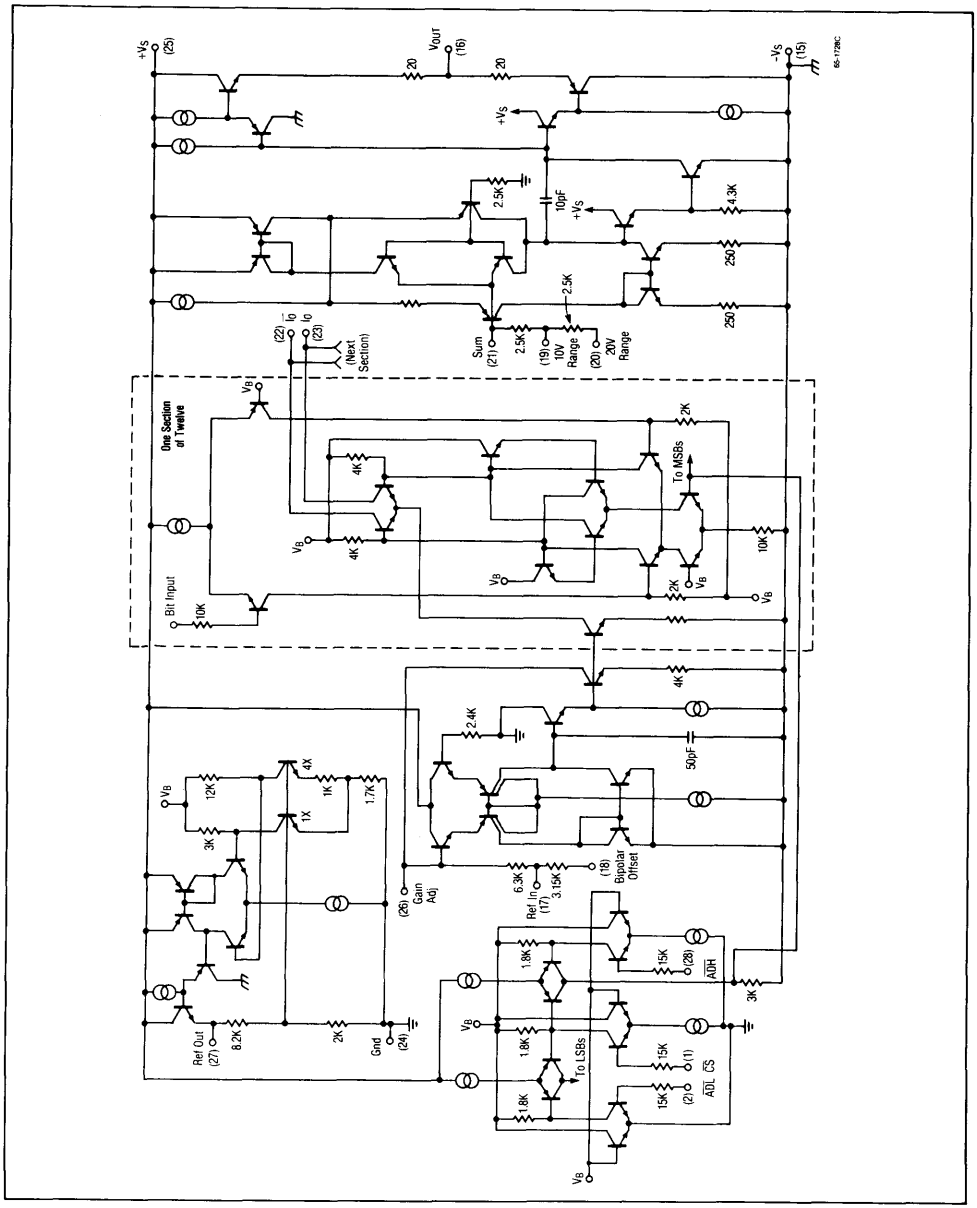
The DAC-4881 is available in three performance grades. The DAC-4881B is specified over the -55°C to +125°C temperature range while the F and D grades are specified over the 0°C to 70°C temperature ranges. All three grades are packaged in a 28-lead side brazed hermetic DIP.

Mask Pattern



Die Size: 125 x 181 mils
Min. Pad Dimensions: 4 x 4 mils

Simplified Schematic Diagram

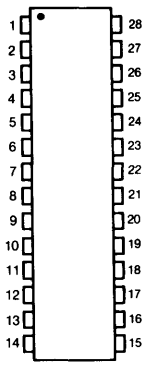


12-Bit D/A Converter With Microprocessor Interface Latches

DAC-4881

Connection Information

28-Lead Ceramic Side-Brazed Dual In-Line Package
(Top View)



65-01730A

Pin	Function
1	$\overline{CS}$
2	$\overline{ADH}$
3	Bit 1 (MSB)
4-13	Input Bits
14	Bit 12 (LSB)
15	$-V_S$
16	V_{OUT}
17	Ref In
18	Bip Off
19	10V Span
20	20V Span
21	Sum Node
22	$\overline{I_O}$
23	I_O
24	Gnd
25	$+V_S$
26	Gain Adj
27	Ref Out
28	$\overline{ADL}$

Absolute Maximum Ratings

Supply Voltage ..... ±18V
Logic Input Voltages ..... -5V to $+V_S$ +36V
I_O and $\overline{I_O}$ Voltages ..... -5V to +12V
Reference Input Voltage ..... $-V_S$ to $+V_S$
Reference Input Current 2mA
Storage Temperature
Range ..... -65°C to +150°C
Lead Soldering Temperature
(60 Sec) ..... +300°C

Thermal Characteristics

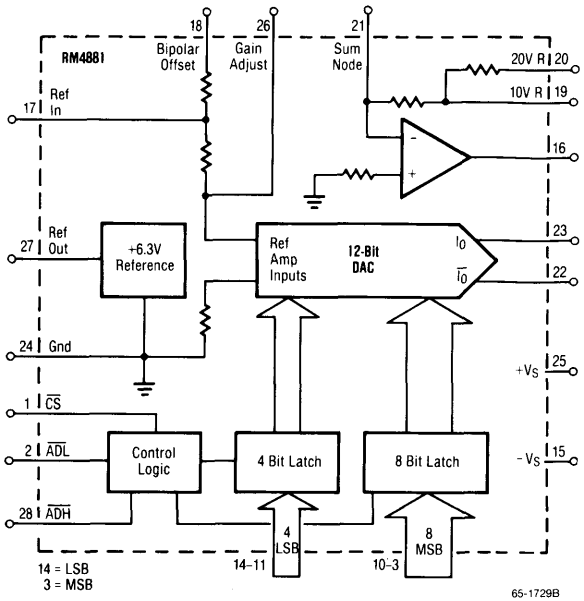
	28-Lead DIP
Max. Junction Temp.	175°C
Max. P_D $T_A < 50°C$	2000mW
Therm. Res. θ_{JC}	15°C/W
Therm. Res. θ_{JA}	60°C/W
For $T_A > 50°C$ Derate at	17mW per °C

Ordering Information

Part Number	Package	Operating Temperature Range
DAC-4881F	Side-brazed	0°C to +70°C
DAC-4881D	Side-brazed	0°C to +70°C
DAC-4881B	Side-brazed	-55°C to +125°C
DAC-4881B/883B*	Side-brazed	-55°C to +125°C

*MIL-STD-883, Level B Processing

Functional Block Diagram



Electrical Characteristics ($+V_S$ = +15V; $-V_S$ = -15V; and T_A = +25°C unless otherwise noted)

Parameters	4881B			4881F			4881D			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Resolution Full Temperature	12			12			12			Bits
Monotonicity Full Temperature	12			12			12			Bits
Linearity Error Full Temperature		.003	.012		.006	.012		.008	.029	LSB
Differential Linearity Error		.006	.012		.012	.012		.012	.029	LSB
Gain Error (ext. ref.)		.05	.1		.08	.2		.1	.3	% of FS
Offset Error Unipolar 10V Range		.003	.012		.003	.025		.003	.15	% of FSR
Bipolar			.1			.15			.15	% of FSR
Reference Output	6.27	6.30	6.33	6.24	6.30	6.36	6.174	6.30	6.426	V
Load Regulation — 9.0mA			.05			.05			.1	%/mA
Line Regulation — V_S +10%			.01			.01			.1	%/V
Noise		1.5			1.5			1.5		mV_{p-p}
Reference Input Impedance	5.0	6.3	7.5	5.0	6.3	7.5		6.3		kΩ
Voltage Output Ranges	0V to +10V, 0V to +5V, ±10V, ±5V, ±2.5V									
External Current	±5		±100	±5		±100	±5			mA
Noise 0.1 to 1MHz		2.0			2.0			2.0		mV_{p-p}
Current Output Full Scale	3.2	4.0	4.8	3.2	4.0	4.8	3.2	4.0	4.8	mA
Zero Scale			250			250			250	nA
Impedance in Parallel with 15pF	2.0	7.0		2.0	7.0		2.0	7.0		MΩ
Compliance	-1.5		+10	-1.5		+10	-1.5		+10	V
Full Scale Symmetry		.005	0.1			0.1				% of FS
Voltage Settling Time 20V Change to .01% of FSR		3.0			3.0			3.0		μS
10V Change to .01% of FSR		1.8			1.8			1.8		μS
1 LSB Change to .01% of FSR		1.3			1.3			1.3		μS
Slew Rate		20			20			20		V/μS
Current Settling, FS Transition		500			500			500		nS
Power Supply Sensitivity +15V ±10%			.001			.001			.001	$\frac{\%\Delta FS/}{\%\Delta V}$
-15V ±10%			.006			.006			.006	

Electrical Characteristics (Continued)

($+V_S$ = +15V; $-V_S$ = −15V; and T_A = +25°C unless otherwise noted)

Parameters	4881B			4881F			4881D			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Power Supply Current										
+ISY			13			13			13	mA
-ISY			19			19			19	mA
Logic Levels	0.8		2.0	0.8		2.0	0.8		2.0	V
Logic Currents										
Data Hi = 5.5V			1.0			1.0			1.0	μA
Data Lo = −0.5V			80			80			80	μA
cbits Hi = 5.5V			500			500			500	μA
cbits Lo = −0.5V			100			100			100	μA
Logic Times										
Data Set-Up		50			50			50		nS
Data Hold		50			50			50		nS
Propagation Delay										
Data to V_{OUT} 10V Unipolar		0.25			0.25			0.25		μS
Data to I_{OUT}		50			50			50		nS
cbits to V_{OUT}		0.30			0.30			0.30		μS
cbits to I_{OUT}		75			75			75		nS
Minimum Write Pulse		60			60			60		nS
Total Bipolar Drift			25			35			35	ppm/°C
Total Error 0°C to +70°C										
Unipolar			0.18			0.33			0.45	% of FSR
Bipolar			0.17			0.28			0.33	% of FSR
Total Error -55°C to +125°C										
Unipolar			0.40							% of FSR
Bipolar			0.40							% of FSR
Gain Drift — External Reference			10			20			20	ppm/°C
Offset Drift										
Unipolar			3.0			3.0			3.0	ppm of FSR/°C
Bipolar			15			15			15	ppm of FSR/°C
Reference Drift			25			50			75	ppm/°C
Linearity Drift			1.3			2.7			5.9	ppm/°C
Differential Linearity Drift			1.3			2.7			5.9	ppm/°C

Digital Input

The interface latches are arranged in two sections: an 8-bit latch for bits 1 through 8, enabled by $\overline{ADH}$, and a 4-bit latch for bits 9 through 12, enabled by $\overline{ADL}$. This 8-bit-4-bit division allows easy interface to an 8-bit microcomputer data bus using the connection shown in Figure 1.

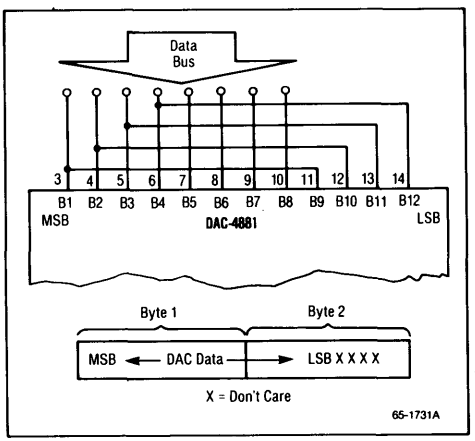


Figure 1. Typical 8-Bit Data Bus Connection — Left Justified Format

TTL, PMOS or CMOS logic levels from the data bus drive the DAC inputs; the logic threshold is typically +1.4V. The voltage level at the inputs can be high going positive, even somewhat higher than the + supply voltage, but can go negative only to about -5V.

Figure 2 shows a timing diagram for a typical 8-bit data bus interface. The DAC-4881 appears to the microprocessor as two locations in memory; the first location for the 8 MSBs and the second location for the 4 LSBs. The addresses for these two locations can be selected by checking the processor's memory map for unused spaces, or by using ROM space (ROMs will only be enabled by read instruction, while the DAC-4881 will only respond to a write). Address decoding can be realized by hard wired logic gates designed to respond with a low output or by using a digital comparator IC such as a DM8131. If the processor used has double byte write instructions with an automatic address incrementation then the system can be simplified, putting the two addresses consecutively and storing the data to be written in a two byte stack.

The sequence in the timing diagram (Figure 2) is as follows: first, the R/W line from the processor, which is tied to the $\overline{CS}$ control input, goes low to start a write to the DAC-4881. Then the address code for the 8 MSBs is sent out on the address bus, is decoded by logic, bringing $\overline{ADH}$ low. The 8 MSB latches are now enabled and the data present on the data bus will change the DAC output. When the $\overline{ADH}$ line goes high again the MSB data is latched in. This sequence of write, address, data is repeated for the 4 LSB latches, and then the $\overline{CS}$ input goes high, ensuring that the data will stay latched in.

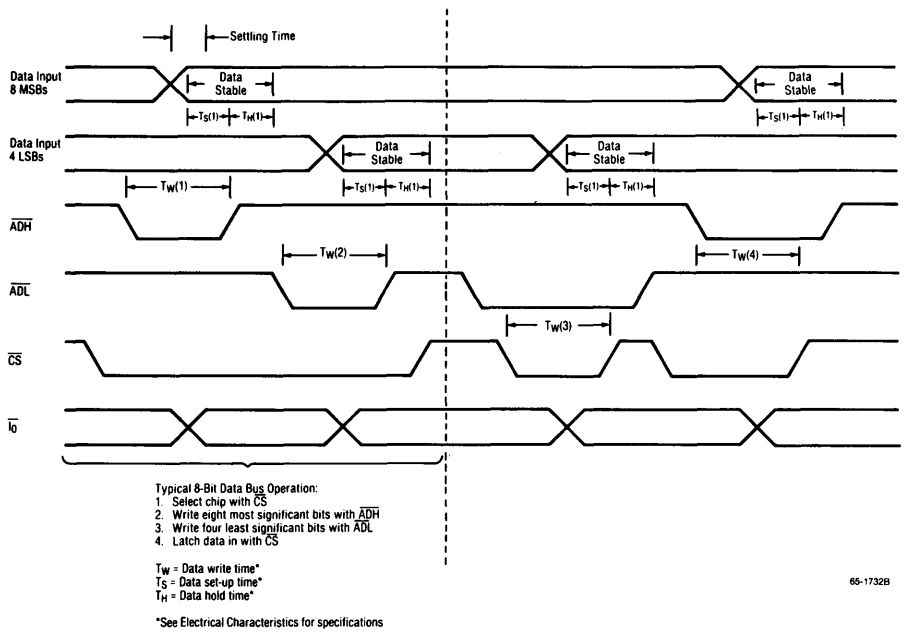


Figure 2. Timing Diagram

Control Inputs

Figure 3 shows a truth table for the three control inputs. Note that minimum durations for these signals are required for proper operation (see the table of Electrical Characteristics for specifications of T_W, T_S, and T_H). T_W is the minimum low state pulse width to guarantee enabling the latch. The data (bit) inputs must also stay in a known state for a minimum amount of time, both before and after the control signal goes high again. The time before the control input goes high is T_S, the data set-up time, and the time after is T_H, the data hold time. This timing is generally created through wait statements in the computer program, or with a one shot if necessary.

The specifications for logic current into the control inputs seem to imply that the logic driving the inputs must have a high output current capability, but note that the logic high is specified at 5.5V, while the logic threshold is down at 1.4V. The actual requirement is for the logic to supply 15μA at 2V, which is within the capability of CMOS and PMOS.

If all the control bits are wired to ground then the DAC-4881 will function just like a conventional D/A converter; that is, any data input will immediately flow through to the output.

$\overline{CS}$	$\overline{ADH}$	$\overline{ADL}$	Result
1	X	X	All inputs disabled — output latched
0	0	0	All inputs active
0	0	1	8 MSBs active — others latched
0	1	0	4 LSBs active — others latched
0	1	1	All inputs disabled — output latched

X = don't care

Figure 3. Control Input Truth Table

Analog Output

The heart of the DAC-4881 is a binary weighted current source DAC. Refer to the Functional Block Diagram.

The reference amplifier forces the reference amplifier input (pin 26, Gain Adjust) to virtual ground (0V). When the +6.3V reference voltage is connected to pin 17 the entire 6.3V is applied across the 6.3kΩ reference resistor. The resultant 1mA current (6.3V/6.3K = 1mA) flows into the ref amp input where it is mirrored and scaled by the binary weighted current sources. The scaling of these current sources is such that the full scale output current is four times the input current; for a 1mA reference the full scale output will be -4mA. (Actually, because the code combination starts at all zeros for 0 output full scale is -4mA +1 LSB, which is -3.99902mA. For a similar reason with 3 decimal digits one can only count up to 999, not to 1000.)

Two outputs are provided, I_O and $\overline{I_O}$. The logic inputs can be complemented (the sense of 1 and 0 reversed) by taking the output from $\overline{I_O}$ instead of I_O. For all zeros at the bit inputs $\overline{I_O}$ will be at full scale, -3.99902mA. If either output is unused it should be grounded, and not left unconnected.

An option for bipolar output (both positive and negative output currents over the input code range — normally both output currents are negative — current flowing into the DAC) is provided with the bipolar offset resistor between pins 17 and 18. For example, what if I_O is connected to pin 18, and I_O is also monitored with a current meter to ground? The reference voltage connected to pin 17 will be applied across the bipolar offset resistor, because pin 18 is wired to ground through the current meter. This creates a 2mA offset current (6.3V/3.15K = 2mA) which adds to the normal output current. So, for all zeros at the inputs the output will be +2mA. For all ones at the inputs the output will be at -2mA +1 LSB (-3.99902mA +2mA = -1.99902).

The op amp is provided as a current to voltage converter, i.e., it changes the -4mA output current into a selectable output voltage. When the output current is connected to the sum node, all of the current will flow into the sum node, and, having nowhere else to go, will flow through the 2.5K span resistors and into the op amp output. Feedback holds the sum node at virtual ground (0V); the IR drop across the span resistor adds to the 0V virtual ground to produce a proportional output voltage at the op amp output.

For example, if pin 19 is wired to pin 16, no offset resistor used, and full scale current of ≈ -4mA is flowing into I_O, then 4mA will flow out of the op amp output, through the 2.5K resistor, and into I_O. 4mA x 2.5K = 10V, so V_{OUT} will equal approximately +10V. Figure 4 shows a table of all the possible combinations of offset and output ranges.

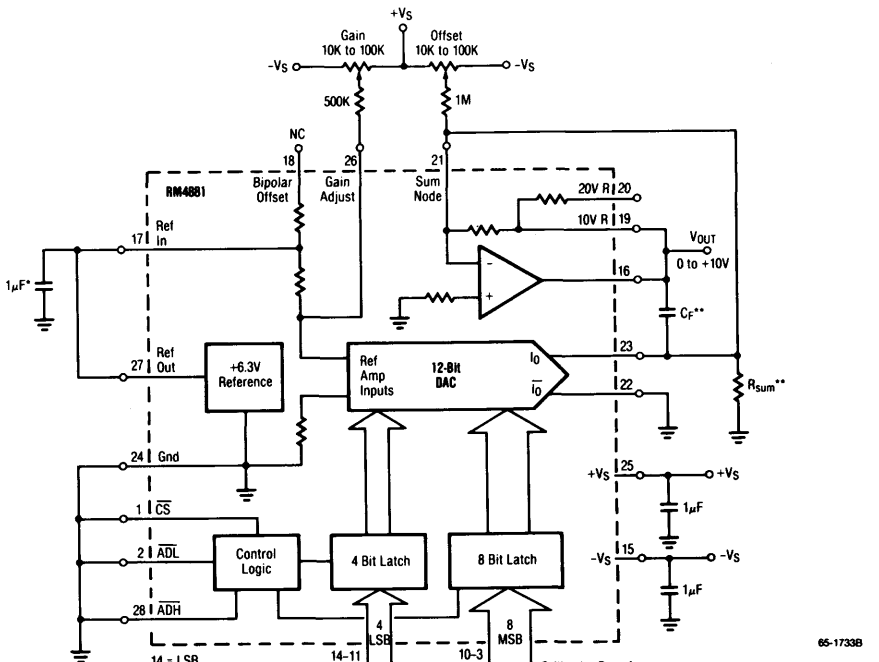
Output Range (zeros to ones)	Pin Connections (always connect 17 to 27)
0V to +5V	20 to 21, 16 to 19, 21 to 23, 22 to Gnd
+5V to 0V	20 to 21, 16 to 19, 21 to 22, 23 to Gnd
0V to +10V	16 to 19, 21 to 23, 22 to Gnd
+10V to 0V	16 to 19, 21 to 22, 23 to Gnd
-2.5V to +2.5V	16 to 19, 18 and 20 to 21, 21 to 23, 22 to Gnd
+2.5V to -2.5V	16 to 19, 18 and 20 to 21, 21 to 22, 23 to Gnd
-5V to +5V	16 to 19, 18 to 21, 21 to 23, 22 to Gnd
+5V to -5V	16 to 19, 18 to 21, 21 to 22, 23 to Gnd
-10V to +10V	16 to 20, 18 to 21, 21 to 23, 22 to Gnd
+10V to -10V	16 to 20, 18 to 21, 21 to 22, 23 to Gnd

Figure 4. Connections for Various Output Formats

Some improvement of settling time can be made with the addition of R_{sum} and C_F in Figures 6 and 7. Figure 5 gives a table of values for the various output combinations. C_F can also be added in aplications where speed is not critical but output noise is. Larger values of C_F will overcompensate the amplifier, slowing it down, but simultaneously integrating out high frequency noise. Noise can also be reduced by adding a large capacitor from the reference output to ground.

Output Range	CF	R_{sum}
0V to +5V	15pF	10K
0V to +10V	5pF	2.5K
±2.5V	15pF	3.3K
±5V	0pF	∞
±10V	0pF	∞

Figure 5. Component Values for Improved Settling Time



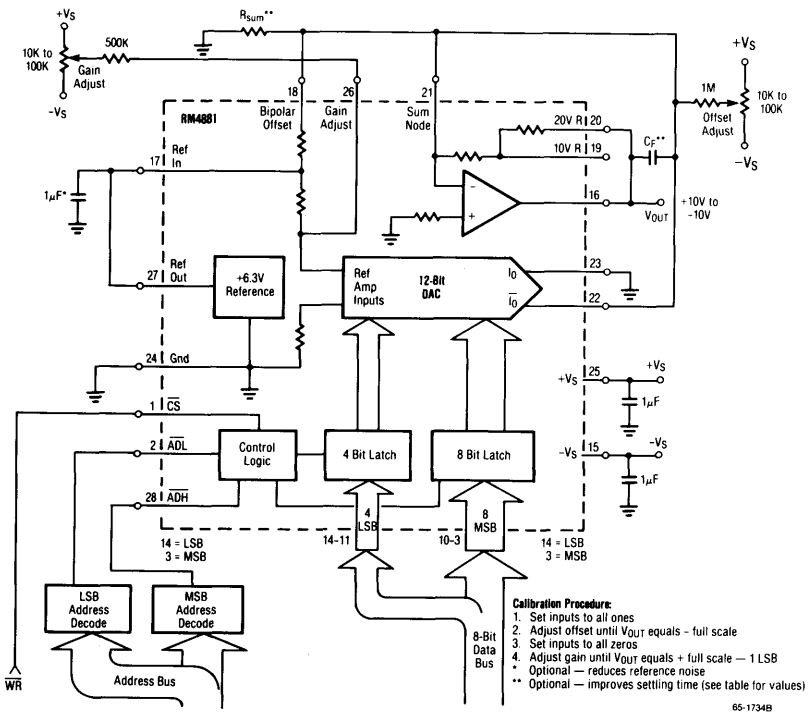
Calibration Procedure:

1. Set inputs to all zeros
2. Adjust offset until V_{OUT} equals 0V
3. Set inputs to all ones
4. Adjust gain until V_{OUT} equals correct full scale value

* Optional — reduces reference noise
** Optional — improves settling time (see table for values)

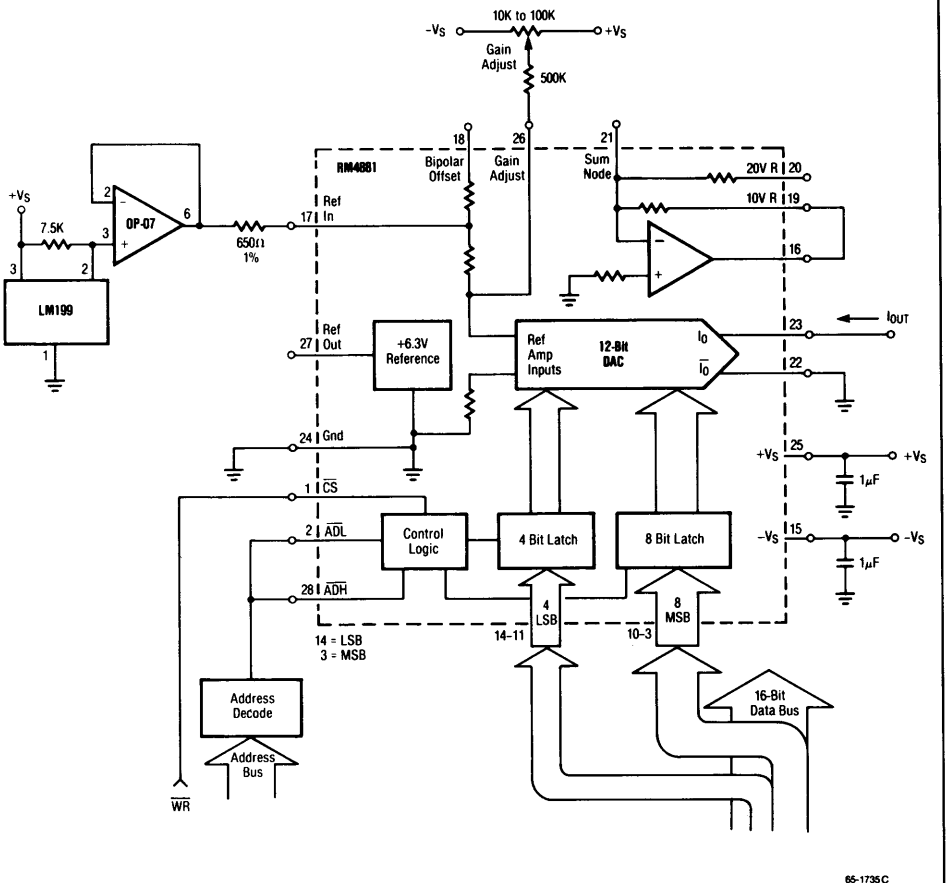
Format	Output Scale	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_O(mA)	$\overline{I_O}$(mA)	V_{OUT}
Straight Binary; Unipolar with True Input Code, True Zero Output	Positive Full Scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
	Positive Full Scale — LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9951
	LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.0001	3.998	0.0024
	Zero Scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	0.0000
Complementary Binary; Unipolar with Complementary Input Code, True Zero Output	Positive Full Scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	9.9976
	Positive Full Scale — LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	9.9951
	LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	0.0024
	Zero Scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	0.0000

Figure 6. Stand-Alone, 0 to +10V, 12-Bit Straight Binary With Gain and Offset Adjust Connections



Format	Output Scale	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_O(mA)	$I_{\overline{O}}$(mA)	V_{OUT}
Offset Binary; True Zero Output	Positive Full Scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9951
	Positive Full Scale — LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9902
	+ LSB	1	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	0.0049
	Zero Scale	1	0	0	0	0	0	0	0	0	0	0	0	0.000	2.000	1.999
	- LSB	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	-0.0049
	Negative Full Scale +LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	-9.9951
	Negative Full Scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	-10.000
2's Complement; True Zero Output MSB Complemented (Need Inverter at B1)	Positive Full Scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9951
	Positive Full Scale — LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9902
	+ LSB	0	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	0.0049
	Zero Scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.0000
	- LSB	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	-0.0049
	Negative Full Scale +LSB	1	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	-9.9951
	Negative Full Scale	1	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	-10.000

Figure 7. Microprocessor Interface, 8-Bit Data Bus, +10V to -10V Output With Complementary Binary Input (All Zeros Equal + Full Scale)

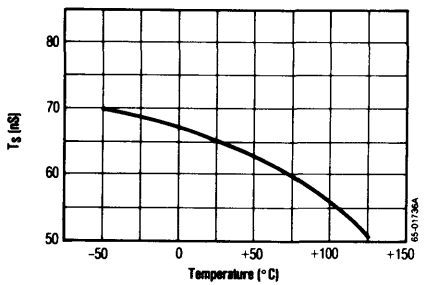


Calibration Procedure:
Zero scale error is entirely leakage curent — no adjustment necessary
1. Set inputs to all ones
2. Adjust gain until I_O equals correct full scale value

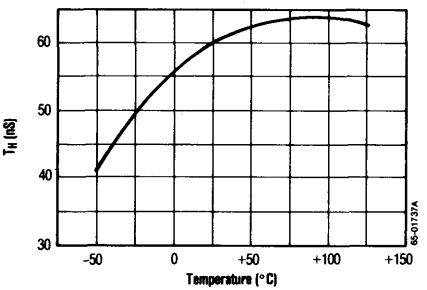
Figure 8. Microprocessor Interface, 16-Bit Data Bus, 0 to -4mA Output With Straight Binary Input and External Reference

Typical Performance Characteristics

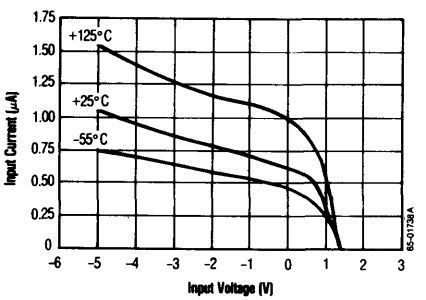
Data Set-Up Time vs. Temperature



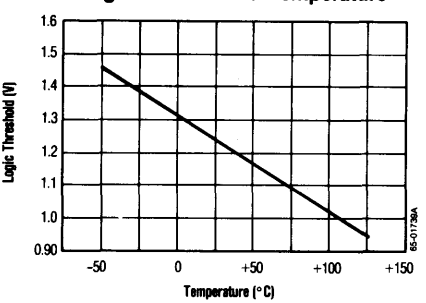
Data Hold Time vs. Temperature



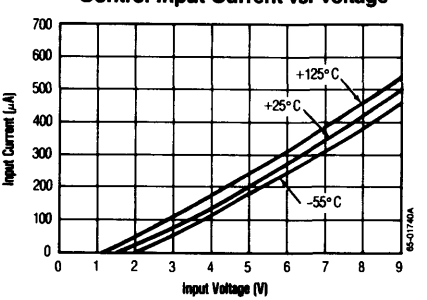
Digital Input Current vs. Voltage



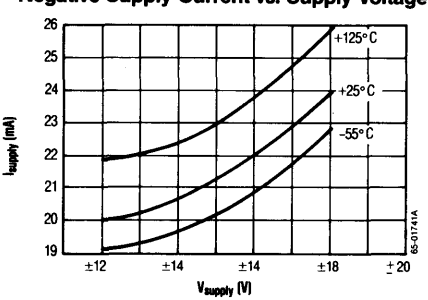
Logic Threshold vs. Temperature



Control Input Current vs. Voltage

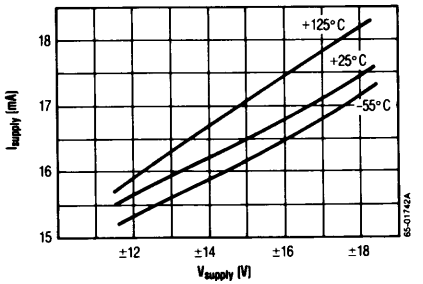


Negative Supply Current vs. Supply Voltage

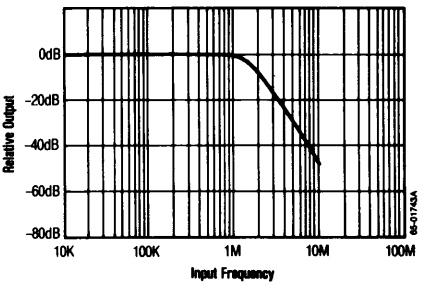


Typical Performance Characteristics (Continued)

Positive Supply Current vs. Supply Voltage



Reference Input Multiplying Frequency Response (V_S 100mV_{p-p})



Raytheon

12-Bit High Speed Multiplying D/A Converter

DAC-6012

Features

- Differential nonlinearity — 0.012% (13 bits)
- Guaranteed monotonicity to 12 bits over temperature
- Relative accuracy — 0.05% all grades
- Fast settling time — 250nS to ±0.5 LSB
- Full scale output current — 4mA
- Complementary current outputs
- Output compliance — -5V to +10V
- Full scale tempco — ±10ppm/° C
- Power consumption — 230mW
- Direct interface to all major logic families
- Standard processing without resistor trimming

Description

The Raytheon DAC-6012 series of monolithic Multiplying Digital-to-Analog Converters guarantee differential nonlinearity to better than ±0.5 LSB (0.012%) for the 6012A and ±1 LSB (0.025%) for the 6012 over the full military and commercial temperature ranges. In addition to the excellent differential nonlinearity specifications, the 6012 series also include many features that previously were found in expensive hybrid modules or required full use of monolithic thim film laser or zener zap trimming techniques.

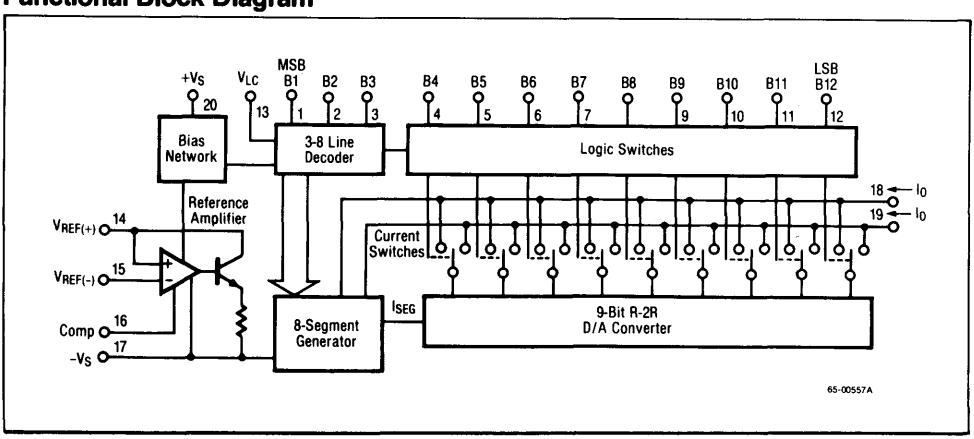
The Raytheon DAC-6012 incorporates a segmented design technique which reduces the requirement for high accuracy resistor ladder networks as an integral part of the DAC. The DAC-6012 design is structured with a 3-bit segment decoder, 5-bit master R-2R ladder DAC and 4-bit Slave DAC. This circuit configuration actually contains less ladder resistors than the traditional R-2R ladder approach as well as effectively improving the accuracy of the ladder resistors by a factor of 8.

The performance of the DAC-6012 is virtually independent of supply voltage variations due to the inherent nature of its design and processing. As an example, the DAC-6012 may be operated at any voltage from +4/-10V to ±18V with minimal effect on the full scale current, DNL, relative accuracy and settling time. The 5MΩ output impedance and -5V to +10V compliance range make the DAC-6012 ideal for high speed applications where output load resistors can be used in place of an output interface amplifier.

The complementary current outputs of the DAC-6012 are useful in symmetrical offset DAC applications and A/D converters requiring constant current loads to ensure significant reduction of switching transients.

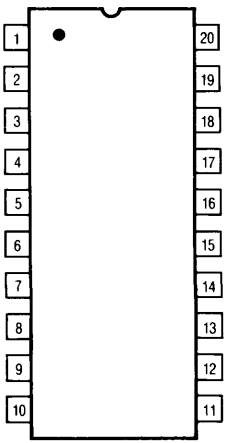
In conjunction with the REF-01 and REF-02 voltage references, and the RC4805 fast precision voltage comparator, the DAC-6012 can be used as the main building block in a wide variety of data conversion applications.

Functional Block Diagram



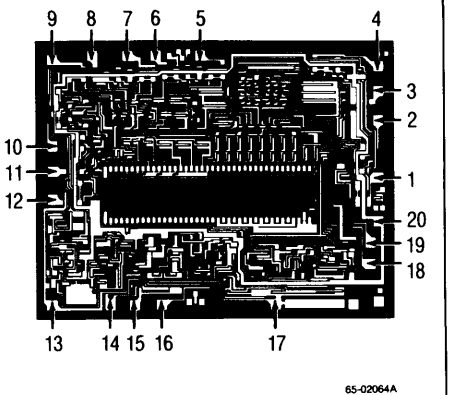
Connection Information

20-Lead
Ceramic Dual In-Line
(Top View)



Pin	Function
1	MSB B1
2	B2
3	B3
4	B4
5	B5
6	B6
7	B7
8	B8
9	B9
10	B10
11	B11
12	B12 LSB
13	V_{LC}/A_{GND}
14	$V_{REF}(+)$
15	$V_{REF}(-)$
16	Comp
17	$-V_S$
18	I_O
19	$\overline{I_O}$
20	$+V_S$

Mask Pattern



Die Size: 104 x 133 mils
Min. Pad Dimensions: 4 x 4 mils

Thermal Characteristics

	20-Lead Ceramic DIP
Max. Junction Temp.	175°C
Max. P_D $T_A < 50°C$	1042mW
Therm. Res. θ_{JC}	60°C/W
Therm. Res. θ_{JA}	120°C/W
For $T_A > 50°C$ Derate at	8.38mW per °C

Ordering Information

Part Number	Package	Operating Temperature Range
DAC-6012ADC	Ceramic	0°C to +70°C
DAC-6012DC	Ceramic	0°C to +70°C
DAC-6012ADM	Ceramic	-55°C to +125°C
DAC-6012DM/883B*	Ceramic	-55°C to +125°C

*MIL-STD-883, Level B Processing

Absolute Maximum Rating

Power Supply Voltage ..... ±18V
Logic Inputs ..... -5.0V to +18V
Analog Current Outputs ..... -8.0V to +12V
Reference Inputs V_{14}, V_{15} ..... $-V_S$ to $+V_S$
Reference Input Differential
Voltage (V_{14}, V_{15}) ..... ±18V
Reference Input Current (I_{14}) 1.25mA
Operating Temperature Range
DAC-6012ADM, DM ..... -55°C to +125°C
DAC-6012ADC, DC ..... 0°C to +70°C
Storage Temperature
Range ..... -65°C to +150°C
Lead Soldering Temperature
(60 Sec) ..... +300°C

Electrical Characteristics

(V_S = ±15V, I_{REF} = 1.0mA, over the operating temperature range unless otherwise specified)

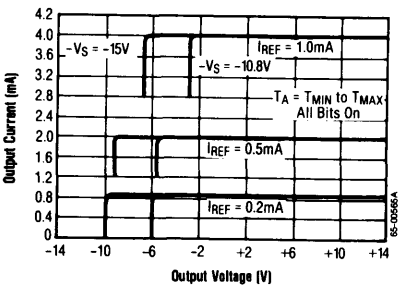
Parameters	Test Conditions	DAC-6012A			DAC-6012			Units
		Min	Typ	Max	Min	Typ	Max	
Resolution		12	12	12	12	12	12	Bits
Monotonicity		12	12	12	12	12	12	Bits
Differential Nonlinearity	Deviation From Ideal Step Size			±0.012			±0.025	%FS
		13			12			Bits
Nonlinarity	Deviation From Ideal Straight Line			±0.05			±0.05	%FS
Full Scale Current	V_{REF} = 10.000V $R_{14} = R_{15}$ = 10.000kΩ T_A = +25°C	3.967	3.999	4.031	3.935	3.999	4.063	mA
Full Scale Tempco			±5.0	±20		±10	±40	ppm/°C
			±0.0005	±0.002		±0.001	±0.004	%FS/°C
Output Voltage Compliance	D.N.L. Specification Guaranteed Over Compliance Range R_{OUT} > 10MΩ Typ.	-5.0		+10	-5.0		+10	V
Full Scale Symmetry	$I_{FS} - I_{FS}$		±0.2	±1.0		±0.4	±2.0	μA
Zero Scale Current				0.2			0.2	μA
Settling Time	To ±1/2 LSB. All Bits ON or OFF. T_A = +25°C		250	500		250	500	nS
Propagation Delay — All Bits	50% to 50%		25	50		25	50	nS
Output Capacitance			20			20		pF
Logic Input Levels Logic "0"				0.8			0.8	V
Logic "1"		2.0			2.0			
Logic Input Current	V_{IN} -5.0V to +18V			40			40	μA
Logic Input Swing	V_S = -15V	-5.0		+18	-5.0		+18	V
Reference Current Range		0.2	1.0	1.1	0.2	1.0	1.1	mA
Reference Bias Current		0	-0.5	-2.0	0	-0.5	-2.0	μA
Reference Input Slew Rate	$R_{14(eq)}$ = 800Ω C_C = 0pF	4.0	8.0		4.0	8.0		mA/μS
Power Supply Sensitivity Positive	V_S = +13.5V to +16.5V, V_S = -15V		±0.0005	±0.001		±0.0005	±0.001	%FS/%
Negative	V_S = -13.5V to -16.5V, V_S = +15V		±0.00025	±0.001		±0.00025	±0.001	

Electrical Characteristics (Continued)

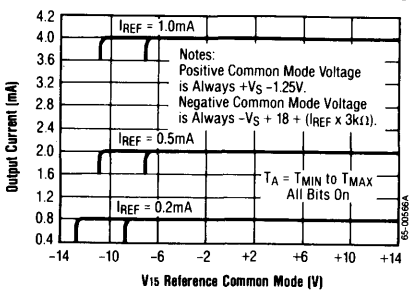
Parameters	Test Conditions	DAC-6012A			DAC-6012			Units
		Min	Typ	Max	Min	Typ	Max	
Power Supply Range Positive	V_{OUT} = 0V	4.5		18	4.5		18	V
Negative		-18		-10.8	-18		-10.8	
Power Supply Current Positive	V_S = +5.0V, V_S = -15V		5.7	8.5		5.7	8.5	mA
Negative			-13.7	-18		-13.7	-18	
Positive	V_S = +15V, V_S = -15V		5.7	8.5		5.7	8.5	
Negative			-13.7	-18		-13.7	-18	
Power Dissipation	V_S = +5.0V, V_S = -15V		234	312		234	312	mW
	V_S = +15V, V_S = -15V		291	397		291	397	

Typical Performance Characteristics

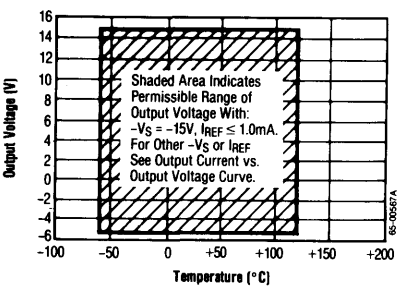
Output Current vs. Output Voltage (Output Voltage Compliance)



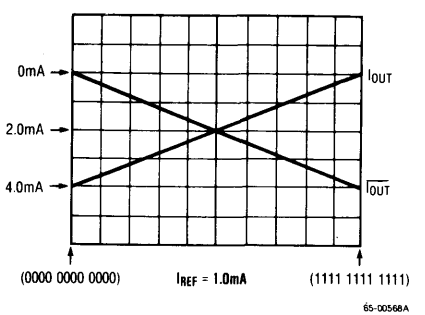
Reference Amplifier Common Mode Range



Output Compliance vs. Temperature



True and Complementary Output Operation



Segmented Design Information

To achieve the linearity necessary to manufacture a 12-bit DAC, previously designed 12-bit DACs have required the use of high precision trimmed thin film resistors arranged in an R-2R ladder configuration (Figure 1). The DAC-6012 deviates from the traditional design by using a segment decoder controlled by bit 1 (MSB) through bit 3. Bits 4 through bit 12 (LSB) control a 9-bit master/slave DAC similar in design to the type used in the DAC-08 and DAC-10 8-bit and 10-bit DACs. The 3-bit segment decoder consists of 8 equal current sources of 0.5 I_{REF} each, and a priority decoder which determines, through the 3-bit code, which one and only one of 8 current sources provide the reference current to the 9-bit DAC and which of the other 7 feed either the I_O or $\overline{I_O}$ ports (Figure 2).

As an example, when bit 1 through bit 3 are 000, the I_A current source is used as the reference current for the 9-bit DAC, I_B through I_H go to the $\overline{I_O}$ port. The outputs of the 9-bit DAC go to either I_O or $\overline{I_O}$ depending on the code at bits 4 through 12. A major segment decoder transition occurs when the code changes from (MSB) 000111111111 (LSB) to 001000000000.

At the transition the I_A current source switches from the 9-bit DAC to the I_O port and the I_B current source switches from $\overline{I_O}$ to become the reference current for the 9-bit DAC, which has just changed from its full scale current (I_A -1 LSB) to its zero scale current at the I_O port. As the input code is increased toward 4095_{10}, the output of each segment current source is switched from $\overline{I_O}$ to become the reference current for the 9-bit DAC, and is then switched to I_O.

Monotonicity is guaranteed using this technique since the current source that was used as the 9-bit DAC reference current is then added directly to the I_O port when the 9-bit DAC changes from its full scale to its zero scale current.

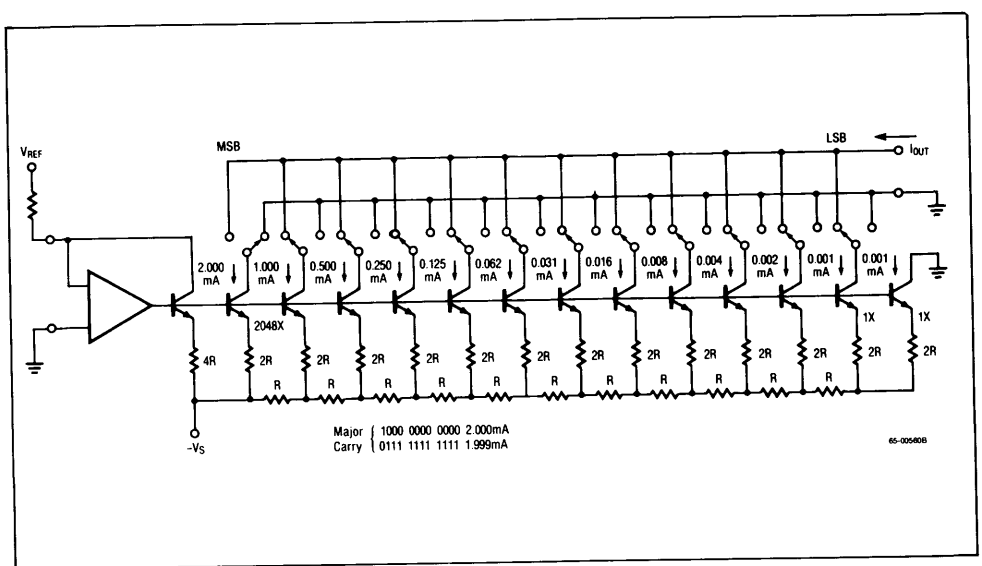


Figure 1. Traditional R-2R D/A Converter

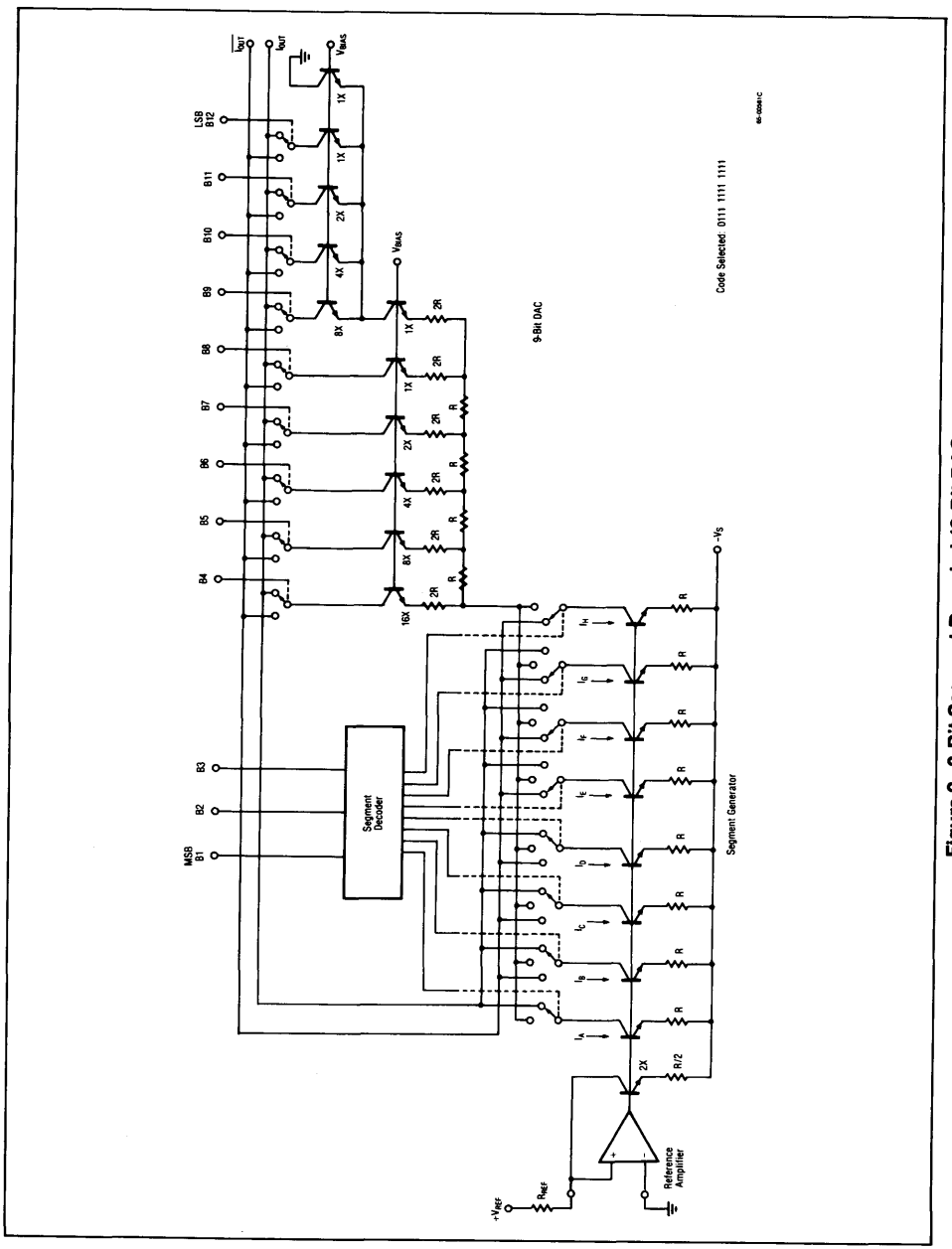


Figure 2. 3-Bit Segment Decoded 12-Bit DAC

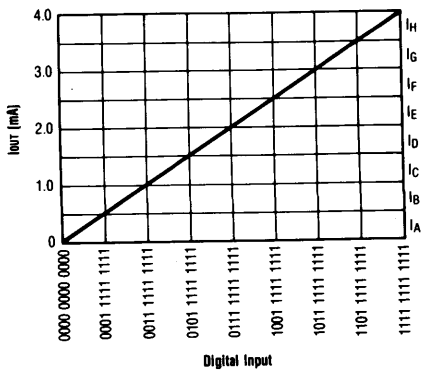


Figure 3. I_O vs. Code for DAC-6012

Recommended Basic Connections

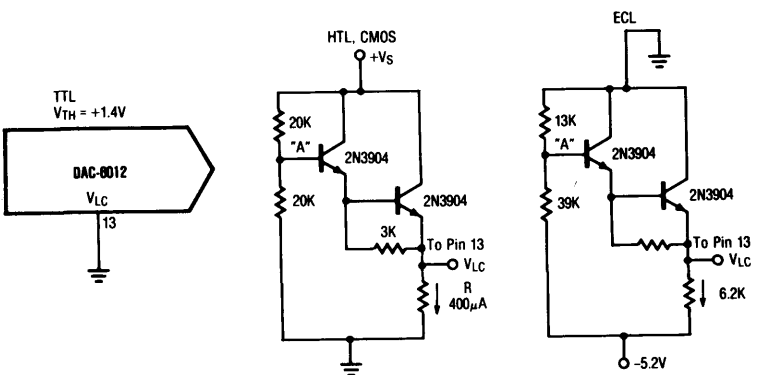
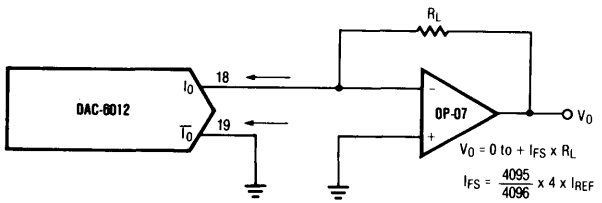


Figure 4. Interfacing With Various Logic Families

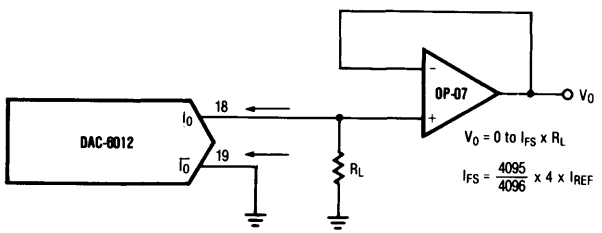
Recommended Basic Connections (Continued)



For Complementary Output (Operation as a Negative Logic DAC), Connect Inverting Input of Op Amp to $\overline{I_O}$ (Pin 19); Connect I_O (Pin 18) to Ground.

65-00569A

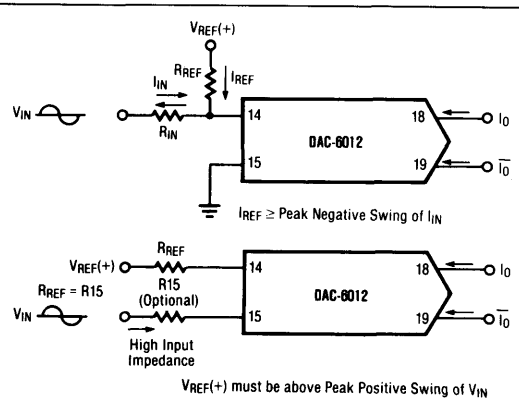
Figure 5. Negative Low Impedance Output Operations



For Complementary Output (Operation as a Negative Logic DAC), Connect Inverting Input of Op Amp to $\overline{I_O}$ (Pin 19); Connect I_O (Pin 18) to Ground.

65-00570A

Figure 6. Positive Low Impedance Output Operations



65-00571A

Figure 7. Accommodating Bipolar References

Recommended Basic Connections (Continued)

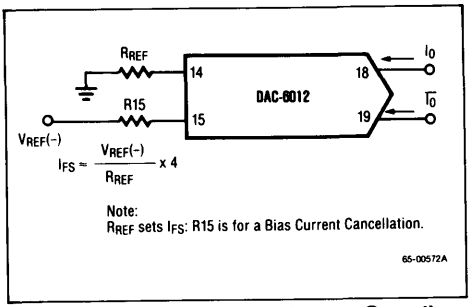


Figure 8. Basic Negative Reference Operation

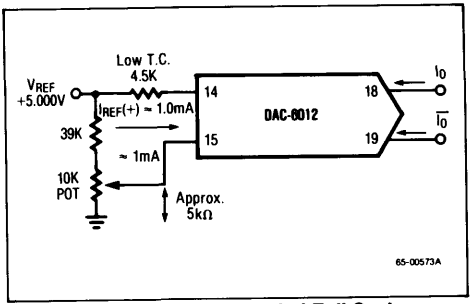


Figure 9. Recommended Full Scale Adjustment Circuit

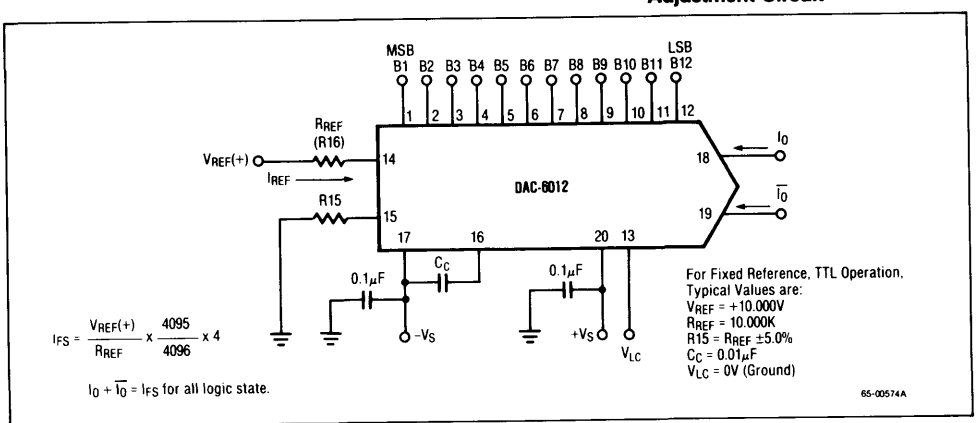


Figure 10. Basic Positive Reference Operation

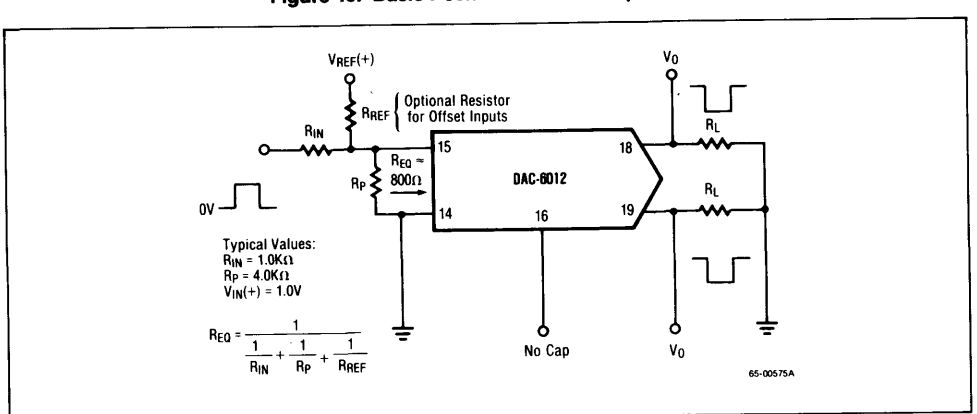
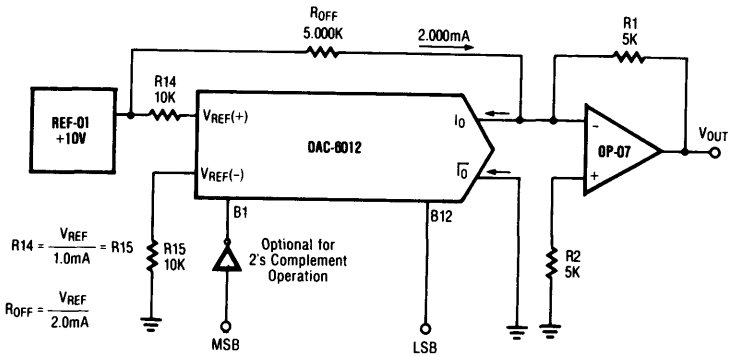


Figure 11. Pulsed Reference Operation

Recommended Basic Connections (Continued)



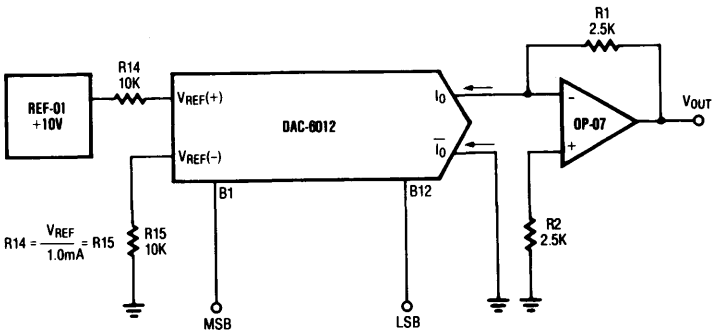
Note: Code may be Complemented by Reversing I_O and $\overline{I_O}$.

Code Format	Output Scale	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_O(mA)	$\overline{I_O}$(mA)	V_{OUT}
Offset Binary; True Zero Output.	Positive Full Scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9951
	Positive Full Scale — LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9902
	+ LSB	1	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	0.0049
	Zero Scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.0000
	- LSB	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	-0.0049
	Negative Full Scale +LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	-9.9951
	Negative Full Scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	-10.000
2's Complement; True Zero Output MSB Complemented (need Inverter at B1).	Positive Full Scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9951
	Positive Full Scale — LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9902
	+ LSB	0	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	0.0049
	Zero Scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.0000
	- LSB	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	-0.0049
	Negative Full Scale + LSB	1	0	0	0	0	0	0	0	0	0	0	0	0.001	3.998	-9.9951
	Negative Full Scale	1	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	-10.000

65-00576B

Figure 12. Bipolar Offset (True Zero)

Recommended Basic Connections (Continued)



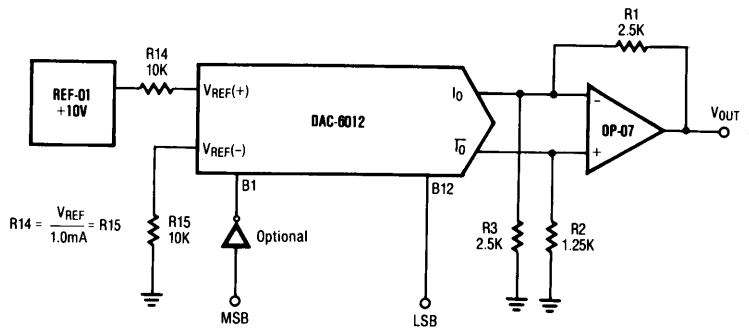
Note: Code may be Complemented by Reversing I_O and $\overline{I_O}$.

Code Format	Output Scale	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_O(mA)	$\overline{I_O}$(mA)	V_{OUT}
Straight Binary; Unipolar with True Input Code, True Zero Output.	Positive Full Scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
	Positive Full Scale — LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9951
	LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.0001	3.998	0.0024
	Zero Scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	0.0000
Complementary Binary; Unipolar with Complementary Input Code, True Zero Output.	Positive Full Scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	9.9976
	Positive Full Scale — LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	9.9951
	LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	0.0024
	Zero Scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	0.0000

65-00577B

Figure 13. Basic Unipolar Operation

Recommended Basic Connections (Continued)



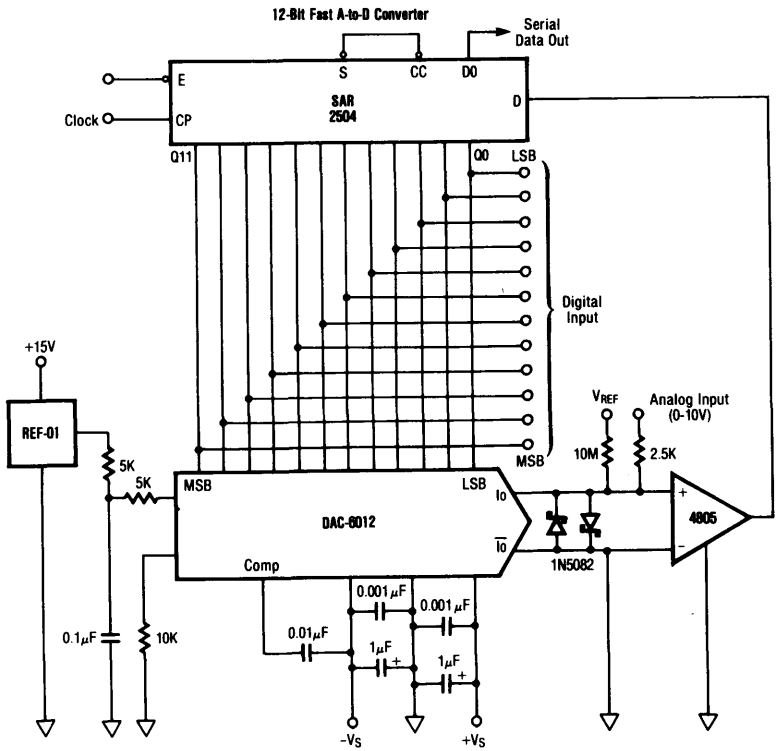
Note: Code may be Complemented by Reversing I_O and $\overline{I_O}$.

Code Format	Output Scale	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_O(mA)	$\overline{I_O}$(mA)	V_{OUT}
Straight Offset Binary; Symmetrical about Zero, No True Zero Output.	Positive Full Scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
	Positive Full Scale — LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9927
	(+) Zero Scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.0024
	(-) Zero Scale	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	-0.0024
	Negative Full Scale — LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	-9.9927
	Negative Full Scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	-9.9976
1's Complement; Symmetrical about Zero, No True Zero Output MSB Complemented (need Inverter at B1).	Positive Full Scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
	Positive Full Scale — LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9927
	(+) Zero Scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.0024
	(-) Zero Scale	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	-0.0024
	Negative Full Scale — LSB	1	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	-9.9927
	Negative Full Scale	1	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	-9.9976

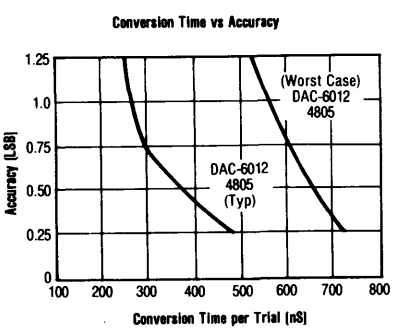
65-00578B

Figure 14. Symmetrical Offset Operation

Recommended Basic Connections (Continued)



Note:
Device(s) connected to analog input must be capable of sourcing 4.0mA a buffer may be required



Conversion Time (nS)	Typ	Worst Case
SAR	33nS	55nS
4805	92nS	125nS
Total	375nS	680nS
x 13	4.9μS	8.8μS

65-00579B

Figure 15. Fast 12-Bit Analog-to-Digital Converter Application

Design and Applications Information

Logic Input

The DAC-6012 uses a unique logic input circuit which allows the user to interface the 6012 with all major logic families. Inputs from -5.0V to +10V may be used when using ±15V supplies. The internal logic threshold is 1.3V nominal and must be adjusted for logic families other than TTL and 5V CMOS by using the circuits in Figure 4. The logic threshold may be adjusted over a wide range using the relationship $V_{TH} = V_{LC} + 1.3V$. Care must be taken when connecting the V_{LC} pin since it typically sinks 3mA. When interfacing with ECL a reference current less than 1mA is recommended since internal voltage compliance problems may exist using negative logic threshold voltages greater than -5V with a -15V supply.

Power Supplies

The DAC-6012 operates over a supply range of +5.0V, -10V to ±18V when using an I_{REF} = 1.0mA. Below -10V voltage headroom limitations inside the DAC-6012 will reduce output compliance to near 0V. Operation below -8V will seriously degrade the overall linearity of the DAC-6012. The positive supply voltage is not critical, and voltage between +4.0V and +18V can be used since most of the circuitry is used to bias the internal logical inputs.

Reference Current and Amplifier

The full scale output current (I_{FS}) at the I_O port is in direct proportion to the reference current into pin 14. The relationship is given as $I_{FS} = 4095/4096\ I_{REF} \times 4 \times 4095/4096$. When I_{REF} = 1.000mA, I_{FS} = 3.999mA. I_{REF} can be varied over a wide range from 1.0μA to 1.1mA for multiplying digital-to-analog converter applications.

For high accuracy, DC reference application circuits require a high quality voltage reference such as the +10V REF-01 or +5.0V REF-02. A stable output current free from excess noise, supply voltage glitches and temperature variations is possible when using a high quality voltage reference and a low TC high accuracy source resistor. If the reference has a 100ppm/°C TC then the output of the DAC will have a similar TC due to the reference alone. Standard 3 terminal voltage regulators used for regulating logic or op amp supply voltage are normally not accurate enough to be used as a reference for 12-bit DAC applications, and therefore are not recommended.

The close relationship between I_{FS} and I_{REF} (±0.8% max error) will, in many applications, not require adjustment of the source or output scaling resistors. If adjustment is necessary, keep in mind the TC of many potentiometers is poorer than fixed resistors. When using DC references it is recommended to split the source resistor in two and bypass with a 0.01μF capacitor from the junction of the two resistors to analog ground. A resistor connected to analog ground from pin 15 should have an ohmic value similar to the total reference resistor so that reference amplifier input bias current effects can be cancelled.

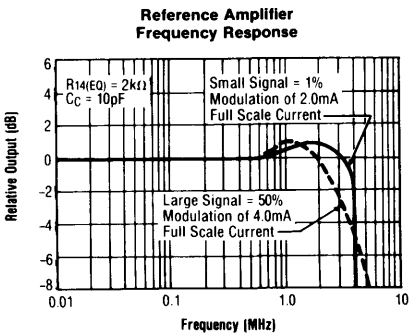
A negative reference voltage may be used as shown in Figure 8. Care must be taken to not exceed the negative common mode voltage of the reference amplifier. This voltage is given by $V_{CM} - = -|-V_S| + 1.8V + (I_{REF} \times 3k\Omega)$.

The reference amplifier must be compensated with a 0.01μF capacitor from pin 16 to pin 17 when using a DC reference. For AC reference applications refer to Figure 16. The value for C_C will depend on the value of the unbypassed source resistor at pin 14. For pulsed reference operation, minimum value source resistors should be used. Compensation is not required for source resistors less than 800Ω, resulting in a fast slew rate and wide bandwidth for the reference amplifier.

For AC reference applications, a minimum value compensation capacitor (C_C) is normally used. The value of this capacitor depends on the equivalent resistance at pin 14. The values to maximize bandwidth without oscillation are as follows:

Minimum Size Compensation Capacitor (I_{FS} = 4.0mA, I_{REF} = 1.0mA)

$R_{14(EQ)}$ (kΩ)	C_C (pF)
10	50
5.0	25
2.0	10
1.0	5.0
0.5	0



Note: A 0.01μF capacitor is recommended for fixed reference operation.

65-00563A

Figure 16. Reference Amplifier Compensation

Analog Output Currents

The true (I_O) and complemented ($\overline{I_O}$) outputs both sink current. The sum of I_O and $\overline{I_O}$ equals I_{FS} for all codes. Complementary outputs are useful for driving balanced cables, CRT deflection coils and center tapped transformers. The current at I_O will increase when "1" (true) is applied at any logic input and decrease when "0" (false) is applied to any logic input. Conversely the $\overline{I_O}$ current decreases when a "1" is applied and increases when a "0" is applied.

The output compliance voltage of the DAC-6012 is between +10V to +25V above the $-V_S$ voltage and as such is useful in applications requiring fast current to voltage conversion since load resistors are used in place of an output amplifier.

If either output is unused it should be grounded. It cannot be left unconnected.

Settling Time

Typical full scale settling time to within +0.5 LSB for the DAC-6012 is 250nS using an I_{REF} between 0.5mA and 1.0mA. The full potential of the DAC-6012 is realized only through careful PC board design. Special care must be taken to separate the analog ground from the digital and power supply grounds. Connect the grounds together at one point near the power supply ground. Logic traces must be kept short and supply bypassing near the DAC-6012 must be generous using a minimum of 1.0μF and 0.01μF in parallel.

If output load resistors are used a pole will be created by the 20pF output capacitance of the DAC-6012 and the load resistor. To prevent degradation of the settling time the load resistor must be kept to less than 500Ω.

Measurement of the settling time requires the ability to resolve less than ±0.5μA. The schematic in Figure 17 and a fast, high resolution oscilloscope (250MHz at 2mV/Div.) are capable of measuring settling times to less than ±0.5 LSB at 12 bits (±0.01%).

The MSB of the DAC-6012 determines the overall settling time of 250nS. If the 6012 is operated as a 10-bit DAC by grounding the MSB and LSB pins, settling times of typically 90nS to 130nS can be achieved.

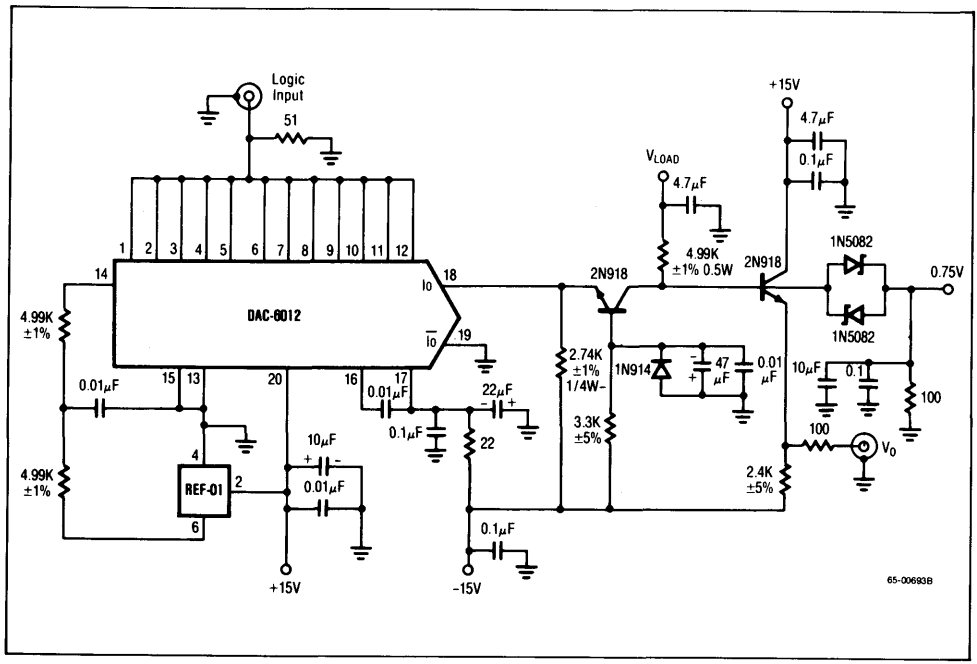


Figure 17. Settling Time Measurement Circuit

Settling Time Measurement

The settling time measurement circuit (Figure 17) must be constructed using the same techniques used for RF circuits. All component leads must be kept short and a very generous ground plane used. Coaxial connectors should be used for the digital input signal as well as the output. 1X probes to monitor the input and output should be used in conjunction with a high speed (>100MHz) oscilloscope with a vertical resolution to at least 2mV/Div. A ±0.5 LSB change at the output of the DAC-6012 will result in a ±2.5mV change at V_O.

A. Set-up procedure — Low to high settling time measurement.
   1. Adjust the DAC-6012 digital inputs to 2V.
   2. Adjust V_{LOAD} so that V_O = 0mV ±10mV. (V_{LOAD} will be about +47V)
   3. Adjust the pulse generator (<10nS rise time) for a 500kHz square wave.
   4. Adjust pulse generator output amplitude so the logic 0 = 0.8V and logic 1 = 2.4V.
   5. Set scope for 100nS/Div. and 2.0mV/Div. and measure time for V_O to fall within ±2.5mV of the final value after the digital inputs change from 0.8V to 2.4V.

B. Set-up procedure — High to low settling time measurement.
   1. Adjust the DAC-6012 digital inputs to 0V.
   2. Adjust V_{LOAD} so that V_O = 0mV ±10mV (V_{LOAD} will abe about +27V).
   3. Repeat steps 3 to 4 above.
   4. Set scope for 100nS/Div. and 2.0mV/Div. and measure time for V_O to fall within ±2.5mV of final value after the digital inputs change from 2.4V to 0.8V.

Temperature Considerations

The DAC-6012 is fully specified for DNL, nonlinearity, and other major DC parameters over temperature. The temperature coefficient (TC) of the full scale output current (I_{FS}) is typically ±8.0ppm/°C drift over the full military temperature range. In most cases, parameters external to the DAC-6012 will contribute most of the errors due to temperature variations. The temperature coefficient (TC) of the reference voltage will cause a directly proportional TC at the output of the DAC-6012. Other factors which enter into the temperature error budget are the TC of the reference (R14) and output scaling resistors. Ideally it should be sufficient that the two resistors track each other so that the TC errors will cancel. Unfortunately the reference resistor power dissipation is constant (assuming a constant reference voltage), therefore, always at a constant temperature rise above the ambient temperature. The output scaling resistor has a power dissipation proportional to the square of the output voltage. For a 0V output in a 10V full scale output system the scaling resistor dissipates 0mW, but at full scale current the resistor (2.5kΩ) is dissipating 40mW. If the TC of the "matched" source and scaling resistors is high enough it can cause a substantial artificial error in the relative accuracy.

Section 9
Voltage-to-Frequency Converters

Modern integrated circuit technology has made the voltage-to-frequency converter (VFC) a cost effective alternative to other analog-to-digital (A/D) systems. A few years ago the VFC was a black box; bulky and expensive. Then hybrid and modular versions were introduced, bringing efficiency and priced under $100.00. In 1976 Raytheon introduced the world's first monolithic VFC, the 4151. Since then the 4152 and 4153 have been designed for increased performance and with fewer external components. Raytheon's monolithic converters offer competitive performance when compared with modular versions, while providing increased flexibility in modifying design parameters, and costing much less.

The future will see increased use of VFCs in places where other methods of conversion are presently employed in addition to a variety of newer non-conventional applications. The advantages of VFCs are in their size, cost, and in serial output which allows them to be located near the source of analog data. VFCs can provide the inverse function, frequency-to-voltage conversion. Raytheon converters can be connected in a number of configurations to fill most needs.

Raytheon offers the following VFCs:

RC4151	8 pin package, 0.013% nonlinearity
RC4152	8 pin package, 0.007% nonlinearity
RC4153	14 pin package, 0.002% nonlinearity

DEFINITIONS

Compliance
The measure of the output impedance of a switched current source, given as a maximum current for a specified voltage change, in microamps (μA).

Full Scale Frequency
A voltage-to-frequency converter can operate up to the guaranteed full scale frequency without violating any of the performance specs for this frequency range. Full scale frequency is expressed in Hertz (Hz).

Nonlinearity Error
On a plot of input voltage versus output frequency, a straight line is drawn from the origin to the full scale point which is defined by the intersection of the maximum input voltage and maximum output frequency.

The actual plot of output frequency versus input voltage should not deviate from this straight line by more than increment $\Delta F_{O(MAX)}$. Nonlinearity is defined here as $(\Delta F_O/\Delta F_S)$ x 100% where F_S is the maximum frequency for the range in question. For instance, when specifying nonlinearity error for the 0.1Hz to 10kHz range, then F_S = 10kHz. When specifying nonlinearity error for a frequency-to-voltage converter, nonlinearity error is defined as $(\Delta V/V_{FS})$ x 100%.

Leakage Current
The current that flows into the open collector output transistor when the logic output transistor is in the "off" state, as a result of the application of the maximum supply voltage to the output. Leakage current is measured in microamps (μA).

Reference Current (4153)
The current flowing into pin 5 as a result of applying a reference voltage of exactly 7.3V, measured in milliamps (mA).

Reference Voltage (V_{REF})
The voltage output of the internal reference as measured from pin 3 to the common terminal (pin 2) of the 4153 — cannot be directly measured for the 4151 and 4152. V_{REF} is expressed in volts (V).

Scale Factor
Scale factor K is the ratio of F_O/V_{IN}.

Scale Factor Tolerance (4153)
Scale factor tolerance is defined for V_{REF}, R_{IN}, and C_O equal to 7.3V, 20,000Ω and 3500pF, respectively. The scale factor tolerance is the amount a measured value of K deviates from the computed value.

Raytheon

Voltage-to-Frequency Converters

RC4151, 4152

Features

- Single supply operation
- Pulse output compatible with all logic forms (DTL/TTL/CMOS)
- Programmable scale factor (K)
- High noise rejection
- Inherent monotonicity
- Easily transmittable output
- Simple full scale trim
- Single-ended input, referenced to ground
- V-F or F-V conversion
- Voltage or current input
- Wide dynamic range

Applications

- Precision voltage-to-frequency converters
- Pulse-width modulators
- Programmable pulse generators
- Frequency-to-voltage converters
- Integrating analog-to-digital converters
- Long-term analog integrators
- Signal conversion —
  Current-to-Frequency
  Temperature-to-Frequency
  Pressure-to-Frequency
  Capacitance-to-Frequency
  Frequency-to-Current
- Signal isolation —
  VFC — opto-isolation — FVC
  ADC with opto-isolation
- Signal Encoding —
  FSK modulation/demodulation
  Pulse-width modulation
- Frequency scaling
- DC motor speed control

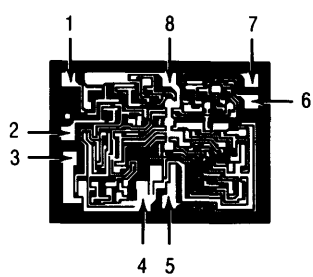
Description

The 4151 and 4152 are monolithic circuits containing all of the active components needed to build a complete voltage-to-frequency converter. Circuits that convert a DC voltage to a pulse train (VFC) can be built by adding a few resistors and capacitors to the internal comparator, one-shot, voltage reference, and switched current source. Frequency-to-voltage converters (FVCs) and many other signal conditioning circuits are also easily created using these converters.

Raytheon was the first company to introduce a monolithic VFC. The low cost 4151 was followed by the 4152, a pin compatible replacement offering guaranteed temperature and accuracy specifications. Both converters are available in a standard 8-pin ceramic or plastic DIP and in an 8-pin metal can.

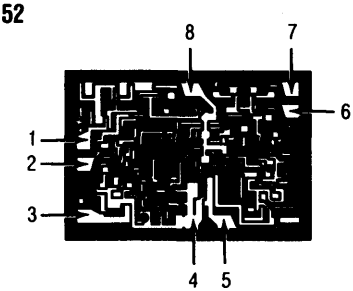
Mask Pattern

4151



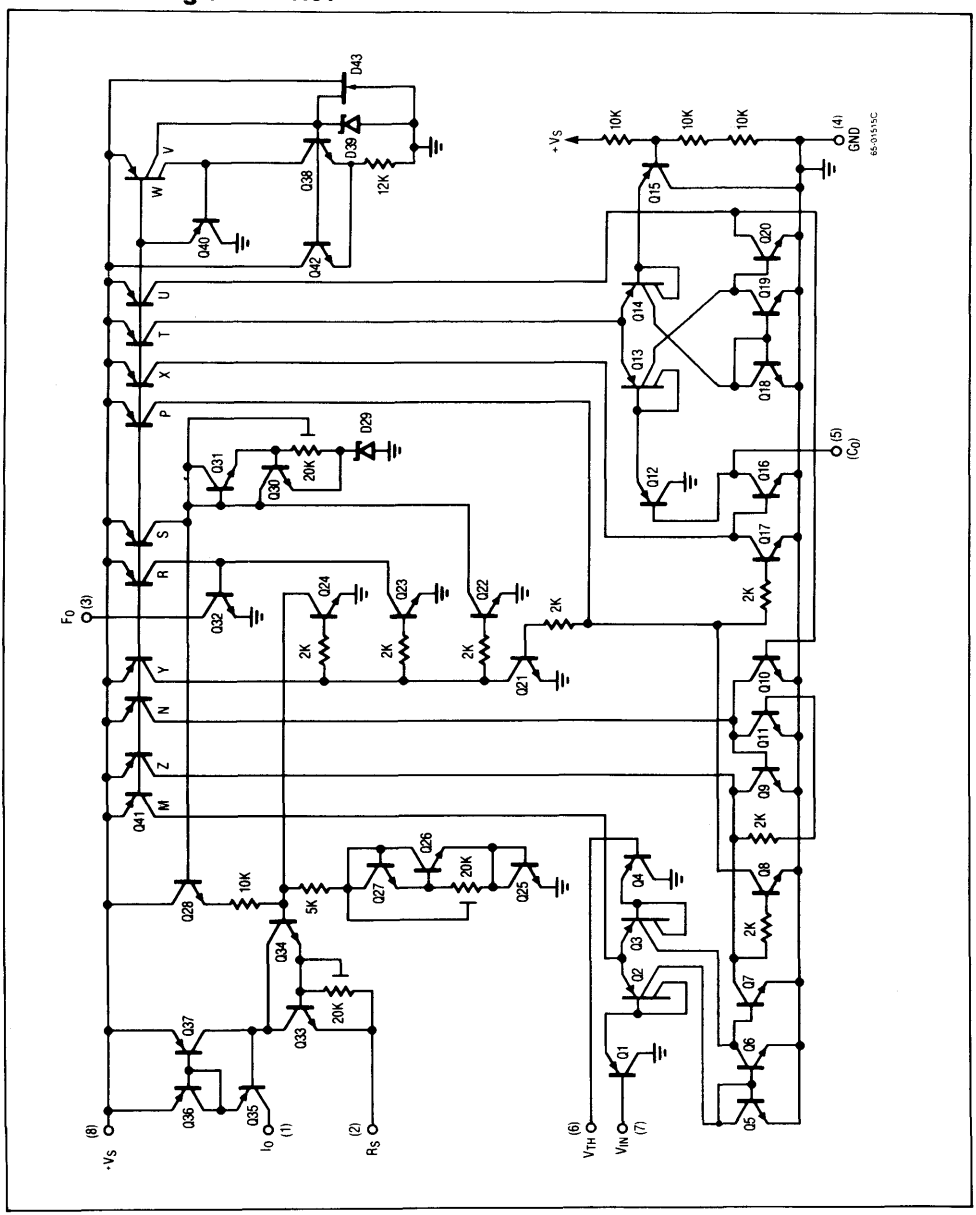
Die Size: 45 x 61 mils
Min. Pad Dimension: 4 x 4 mils

4152

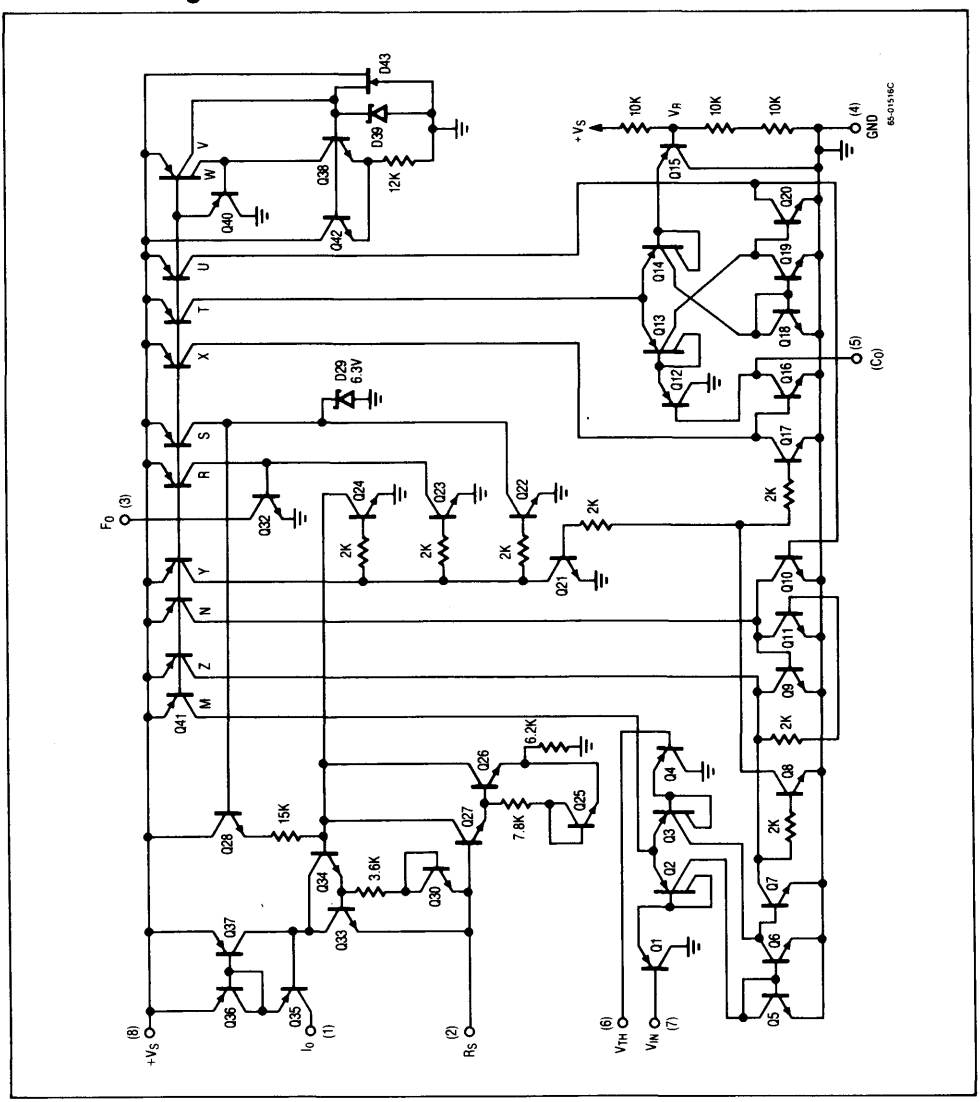


Die Size: 47 x 68 mils
Min. Pad Dimension: 4 x 4 mils

Schematic Diagram — 4151

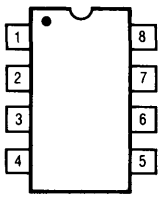


Schematic Diagram — 4152



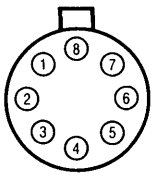
Connection Information

DE and NB
Dual In-Line Packages



65-01529A

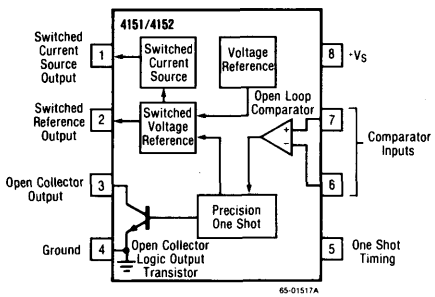
T
(TO-99) Metal Can



65-01530A

Pin	Function
1	Switched Current Source Output (I_O)
2	Switched Voltage Reference (R_S)
3	Logic Output (Open Collector) (F_O)
4	Ground (GND)
5	One-Shot R, C Timing (C_O)
6	Threshold (V_{TH})
7	Input Voltage (V_{IN})
8	$+V_S$

Functional Block Diagram



65-01517A

Absolute Maximum Ratings

Supply Voltage ..... +22V
Internal Power Dissipation 500mW
Input Voltage ..... -0.2V to $+V_S$
Output Sink Current
(Frequency Output) 20mA
Output Short Circuit to Ground .. Continuous
Storage Temperature Range
RM4151, 4152 ..... -65°C to +150°C
RV4151, 4152 ..... -55°C to +125°C
RC4151, 4152 ..... -55°C to +125°C
Operating Temperature Range
RM4151, 4152 ..... -55°C to +125°C
RV4151, 4152 ..... -40°C to +85°C
RC4151, 4152 ..... 0°C to +75°C

Thermal Characteristics

	8-Lead Plastic DIP	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can
Max. Junction Temp.	125°C	175°C	175°C
Max. P_D $T_A > 50°C$	468mW	833mW	658mW
Therm. Res. θ_{JC}	—	45°C/W	50°C/W
Therm. Res. θ_{JA}	160°C/W	150°C/W	190°C/W
For $T_A > 50°C$ Derate at	6.25mW per °C	8.33mW per °C	5.26mW per °C

Ordering Information

Part Number	Package	Operating Temperature Range
RC4151DE	Ceramic	0°C to +70°C
RC4151NB	Plastic	0°C to +70°C
RC4151T	TO-99	0°C to +70°C
RC4152DE	Ceramic	0°C to +70°C
RC4152NB	Plastic	0°C to +70°C
RC4152T	TO-99	0°C to +70°C
RV4151DE	Ceramic	-40°C to +85°C
RV4151NB	Plastic	-40°C to +85°C
RV4152DE	Ceramic	-40°C to +85°C
RV4152DE	Ceramic	-40°C to +85°C
RM4151DE	Ceramic	-55°C to +125°C
RM4151DE/883B*	Ceramic	-55°C to +125°C
RM4151T	TO-99	-55°C to +125°C
RM4151T/883B*	TO-99	-55°C to +125°C
RM4152DE	Ceramic	-55°C to +125°C
RM4152DE/883B*	Ceramic	-55°C to +125°C
RM4152T	TO-99	-55°C to +125°C
RM4152T/883B*	TO-99	-55°C to +125°C

*MIL-STD-883, Level B Processing

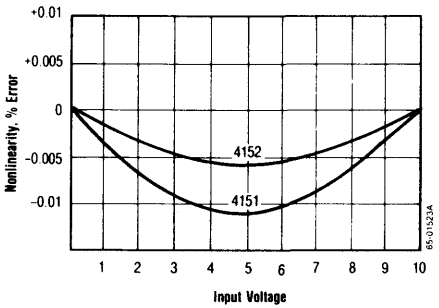
Electrical Characteristics (V_S = +15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	4151			4152			Units
		Min	Typ	Max	Min	Typ	Max	
Power Supply Requirements (Pin 8) Supply Current	V_S = +15V		4.5	7.5		2.5	6.0	mA
Supply Voltage		+8.0	+15	+22	+7.0	+15	+18	V
Input Comparator (Pins 6 and 7) V_{OS}			±2.0	±10		±2.0	±10	mV
Input Bias Current			-100	-300		-50	-300	nA
Input Offset Current			±50	±100		±30	±100	nA
Input Voltage Range		0	V_S-2	V_S-3	0	V_S-2	V_S-3	V
One Shot (Pin 5) Threshold Voltage		0.63	0.67	0.70	0.65	0.67	0.69	XV_S
Input Bias Current			-100	-500		-50	-500	nA
Saturation Voltage	I = 2.2mA		0.15	0.5		0.1	0.5	V
Drift of Timing vs. Temperature	T = 75μS 0°C to +70°C		±35			±30	±50	ppm/°C
Drift of Timing vs. Supply			±150			±100		ppm/V
Switched Current Source[1] (Pin 1) Output Current	4151-R_S = 14.0K/ 4152-R_S = 16.7K		+138			+138		μA
Drift vs. Temperature	0°C to +70°C		±75			±50	±100	ppm/°C
Drift vs. Supply Voltage			0.15			0.10		%/V
Leakage Current	Off State		1.0	50		1.0	50	nA
Compliance	Pin 1 = 0V to +10V	1.0	2.5		1.0	2.5		μA
Reference Voltage (Pin 2) V_{REF}		1.7	1.9	2.08	2.0	2.25	2.5	V
Drift vs. Temperature	0°C to +70°C		±50			±50	±100	ppm/°C
Logic Output (Pin 3) Saturation Voltage	I_{SINK} = 3.0mA		0.1	0.5		0.1	0.5	V
Saturation Voltage	I_{SINK} = 10mA		0.8			0.8		V
Leakage Current	Off State		0.2	1.0		0.1	1.0	μA
Nonlinearity % Error Voltage Sourced Circuit of Figure 3	1.0Hz to 10kHz		0.013			0.007	0.05	%
Temperature Drift Voltage Sourced Circuit of Figure 3	F_O = 10kHz		±100			±75	±150	ppm/°C

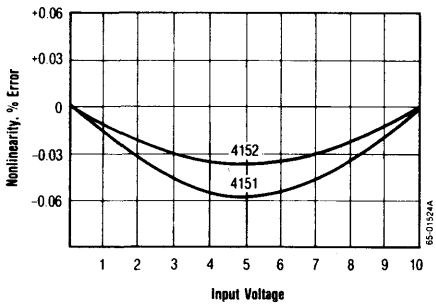
Note 1. Temperature coefficient of output current source (pin 1 output) exclusive of reference voltage drift.

Typical Performance Characteristics

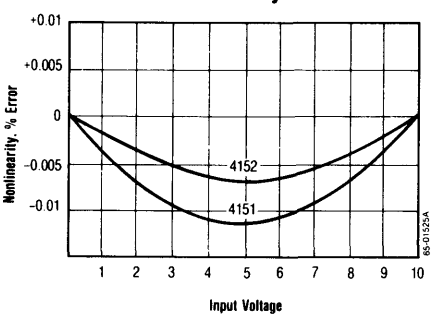
10kHz Current-Sourced VFC Nonlinearity



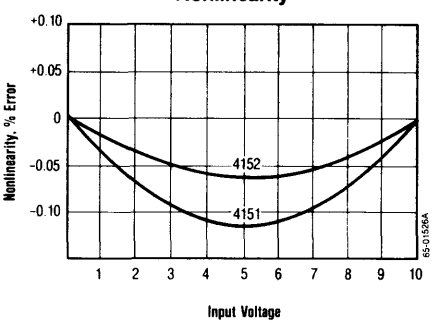
100kHz Current-Sourced VFC Nonlinearity



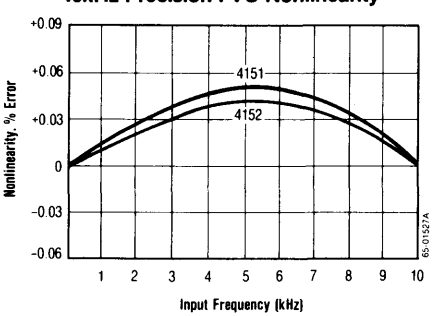
10kHz Voltage-Sourced VFC Nonlinearity



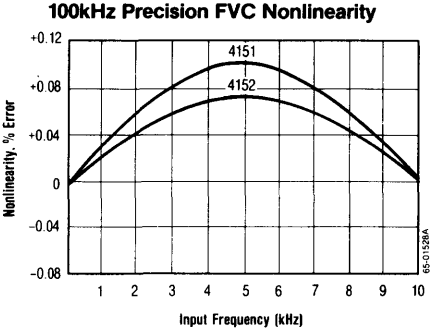
100kHz Voltage-Sourced VFC Nonlinearity



10kHz Precision FVC Nonlinearity



100kHz Precision FVC Nonlinearity



Principles of Operation

The 4151 and the 4152 contain the following components: an open loop comparator, a precision one-shot timer, a switched voltage reference, a switched current source, and an open collector logic output transistor. These functional blocks are internally interconnected in a special way. By adding some external resistors and capacitors, a designer can create a complete voltage-to-frequency converter.

The comparator's output controls the one-shot (monostable timer). The one-shot in turn controls the switched current source, the switched reference, and the open collector output transistor. The block diagram shows the components and their interconnection.

To detail, if the voltage at pin 7 is greater than the voltage at pin 6, the comparator switches and triggers the one-shot. When the one-shot is triggered, two things happen. First, the one-shot begins its timing period. Second, the one-shot's output turns on the switched current source, the switched voltage reference, and the open collector output transistor.

The one-shot creates its timing period much like the popular 555 timer does, by charging a capacitor from a resistor tied to $+V_S$. The one-shot senses the voltage on the capacitor (pin 5) and ends the timing period when the voltage reaches 2/3 of the supply voltage. At the end of the timing period the capacitor is discharged by a transistor similar to the open collector output transistor.

Meanwhile, during the timing period of the one-shot, the switched current source, the switched reference, and the open collector output transistor all will be switched on. The switched current source (pin 1) will deliver a current proportional to both the reference voltage and an external resistor, R_S. The switched reference (pin 2) will supply an output voltage equal to the internal reference voltage (4151 = 1.9V, 4152 = 2.25V). The open collector output transistor will be turned on, forcing the logic output (pin 3) to a low state. At the end of the timing period all of these outputs will turn off. The switched voltage reference has produced an off-on-off voltage pulse, the switched current source has emitted a quanta of charge, and the open collector output has transmitted a logic pulse.

To summarize, the purpose of the circuit is to produce a current pulse, well-defined in amplitude and duration, and to simultaneously produce an output pulse which is compatible with most logic families. The circuit's outputs show a pulse waveform in response to a voltage difference between the comparator's inputs.

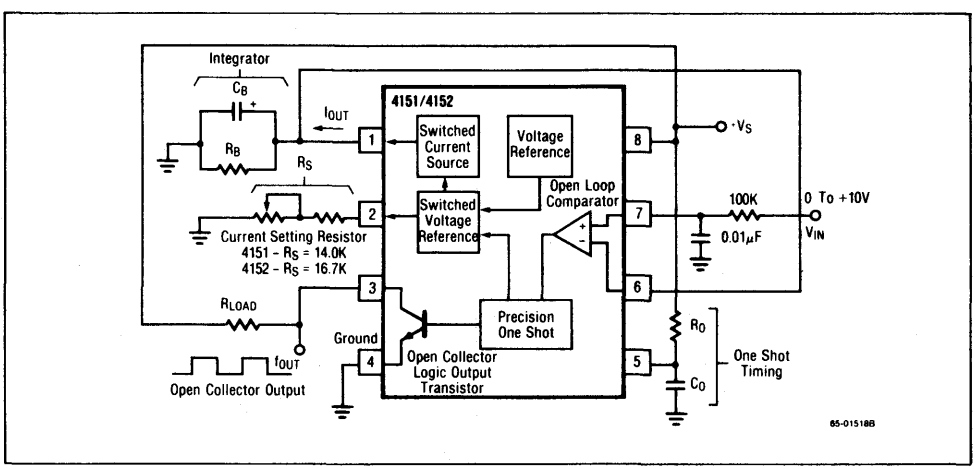


Figure 1. Single Supply VFC

Applications

Single Supply VFC

The stand-alone voltage-to-frequency converter is one of the simplest applications for the 4151 or 4152. This application uses only passive external components to create the least expensive VFC circuit.

The positive input voltage V_{IN} is applied to the input comparator through a low pass filter. The one-shot will fire repetitively and the switched current source will pump out current pulses of amplitude V_{REF}/R_S and duration 1.1 R_OC_O into the integrator. Because the integrator is tied back to the inverting comparator input, a feedback loop is created. The pulse repetition rate will increase until the average voltage on the integrator is equal to the DC input voltage at pin 7. The average voltage at pin 6 is proportional to the output frequency because the amount of charge in each current pulse is precisely controlled.

Because the one-shot firing frequency is the same as the open collector output frequency, the output frequency is directly proportional to V_{IN}.

The external passive components set the scale factor. For best linearity, R_S should be limited to a range of 12kΩ to 20kΩ.

The reference voltage is nominally 1.9V for the 4151 and 2.25V for the 4152. Recommended values for different operating frequencies are shown in the table below.

Operating Range	R_O	C_O	R_B	C_B
DC to 1.0kHz	6.8kΩ	0.1μF	100kΩ	10μF
DC to 10kHz	6.8kΩ	0.01μF	100kΩ	1.0μF
DC to 100kHz	6.8kΩ	0.001μF	100kΩ	0.1μF

The single supply VFC is recommended for uses where the dynamic range of the input is limited, and the input does not reach 0V. With 10kHz values, nonlinearity will be less than 1.0% for a 10mV to 10V input range, and response tme will be about 135mS.

Precision Current-Sourced VFC

This circuit operates similarly to the single supply VFC, except that the passive R-C integrator has been replaced by an active op amp integrator. This increases the dynamic range down to 0V, improves the response time, and eliminates the nonlinearity error introduced by the limited compliance of the switched current source output.

The integrator algebraically sums the positive current pulses from the switched current source with the current V_{IN}/R_B. To operate correctly, the input voltage must be negative, so that when the circuit is balanced, the two currents cancel.

$$T = \frac{1}{F_{OUT}}$$

$$\frac{|V_{IN}|}{R_B} = I_{OUT}\left[\frac{T_P}{T}\right] \text{ where } T_P = 1.1\ R_OC_O$$

$$I_{OUT} = \frac{V_{REF}}{R_S}$$

By rearranging and substituting,

$$F_{OUT} = \frac{1}{T}\left[\frac{R_S}{1.1\ R_OC_OR_B}\right]\left[\frac{V_{IN}}{V_{REF}}\right]$$

Recommended component values for different operating frequencies are shown in the table below.

Range		Scale Factor	R_0	C_0	C_1	R_B
Input V_{IN}	Output F_0					
0 to -10V	0 to 1.0kHz	0.1kHz/V	6.8kΩ	0.1μF	0.05μF	100kΩ
0 to -10V	0 to 10kHz	1.0kHz/V	6.8kΩ	0.01μF	0.005μF	100kΩ
0 to -10V	0 to 100kHz	10kHz/V	6.8kΩ	1000pF	500pF	100kΩ

The graphs shown under Typical Performance Characteristics show nonlinearity versus input voltage for the precision current-sourced VFC. The 4152s improved circuitry reduces nonlinearity error when compared to the 4151. The best linearity is achieved by using an op amp having greater than 1.0V/μS slew rate, but any op amp can be used.

Precision Voltage-Sourced VFC

This circuit is identical to the current-sourced VFC, except that the current pulses into the integrator are derived directly from the switched voltage reference. This improves temperature drift at the expense of high frequency linearity.

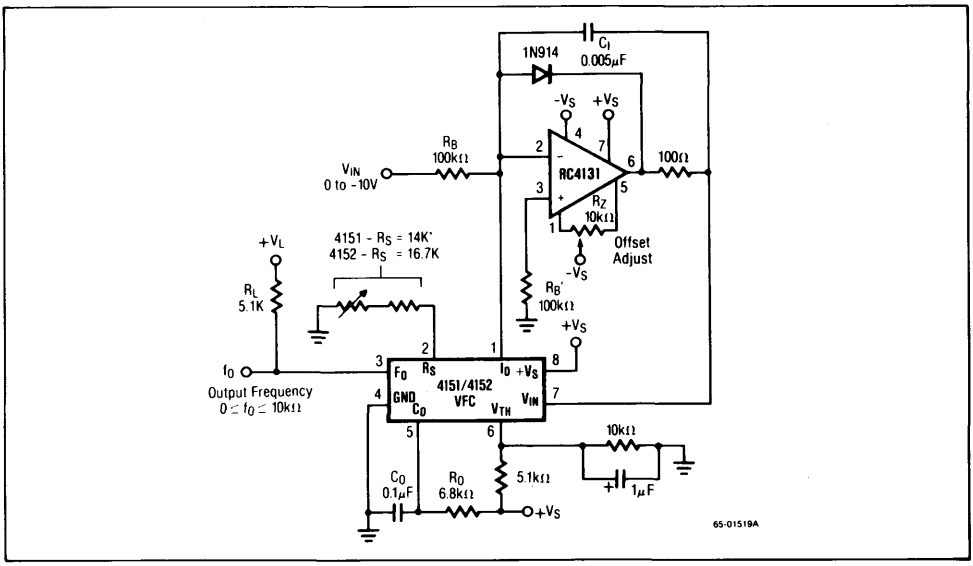


Figure 2. Precision Current — Sourced VFC

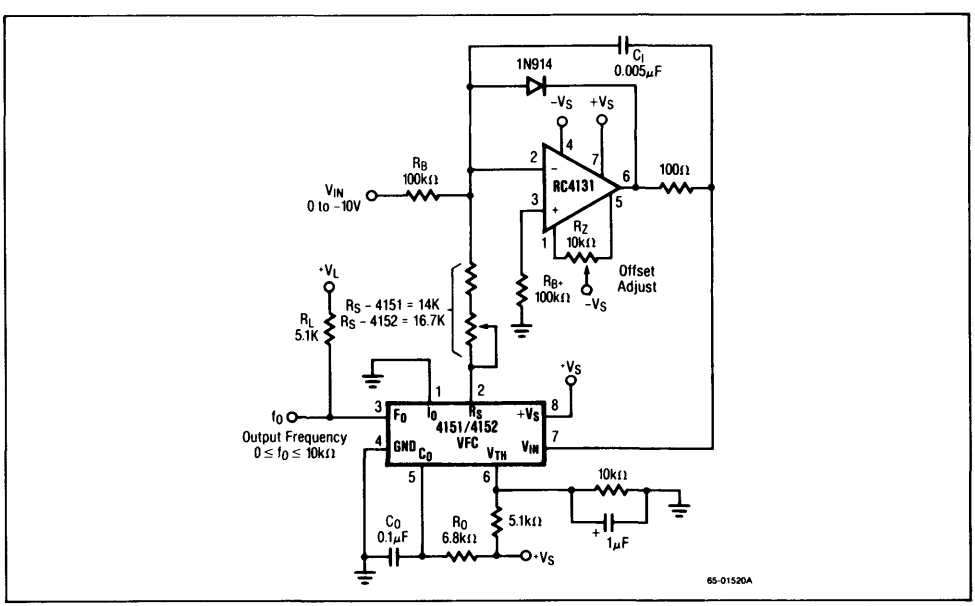


Figure 3. Precision Voltage — Sourced VFC

The switched current source (pin 1) output has been tied to ground, and R_S has been put in series between the switched voltage reference (pin 2) and the summing node of the op amp. This eliminates temperature drift associated with the switched current source. The graphs under the Typical Performance Characteristics show that the nonlinearity error is worse at high frequency, when compared with the current-sourced circuit.

Single Supply FVC

A frequency-to-voltage converter performs the exact opposite of the VFCs function; it converts an input pulse train into an average output voltage. Incoming pulses trigger the input comparator and fire the one-shot. The one-shot then dumps a charge into the output integrator. The voltage on the integrator becomes a varying DC voltage proportional to the frequency of the input signal. Figure 4 shows a complete single supply FVC.

The input waveform must have fast slewing edges, and the differentiated input signal must be less than the timing period of the one-shot, 1.1 R_OC_O. A differentiator and divider are used to shape and bias the trigger input; a negative going pulse at pin 6 will cause the comparator to fire the one-shot. The input pulse amplitude must be large enough to trip the comparator, but not so large as to exceed the ICs input voltage ratings.

The output voltage is directly proportional to the input frequency:

$$V_O = \left[\frac{1.1\ R_O C_O\ R_B\ V_{REF}}{R_S} \right] f_{IN}\ (Hz)$$

Output ripple can be minimized by increasing C_B, but this will limit the response time. Recommended values for various operating ranges are shown in the table below.

Input Operating Range	C_{IN}	R_O	C_O	R_B	C_B	Ripple
0 to 1.0kHz	0.02μF	6.8kΩ	0.1μF	100kΩ	100μF	1.0mV
0 to 10kHz	0.002μF	6.8kΩ	0.01μF	100kΩ	10μF	1.0mV
0 to 100kHz	200pF	6.8kΩ	0.001μF	100kΩ	1.0μF	1.0mV

Precision FVC

Linearity, offset, and response time can be improved by adding one or more op amps to form an active lowpass filter at the output. A circuit using a single pole active integrator is shown in Figure 5.

The positive output current pulses are averaged by the inverting integrator, causing the output voltage to be negative. Response time can be further improved by adding a double pole filter to replace the single pole filter. Refer to the graphs under Typical Performance Characteristics that show nonlinearity error versus input frequency for the precision FVC circuit.

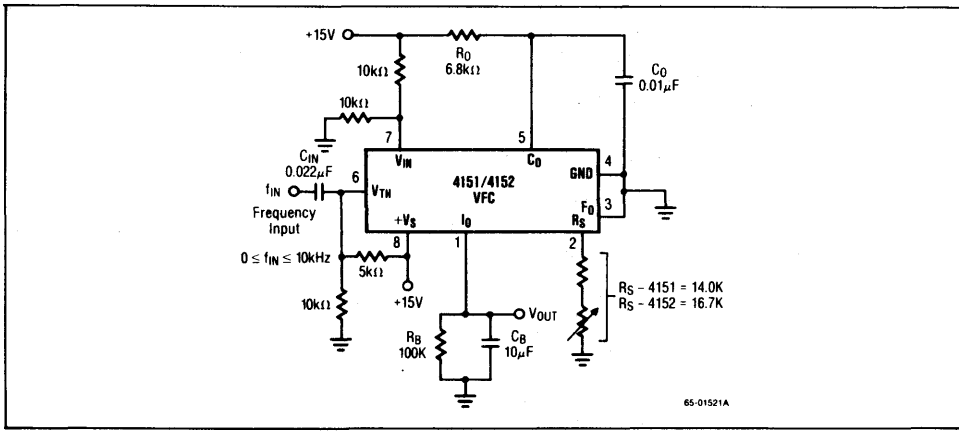


Figure 4. Single Supply FVC

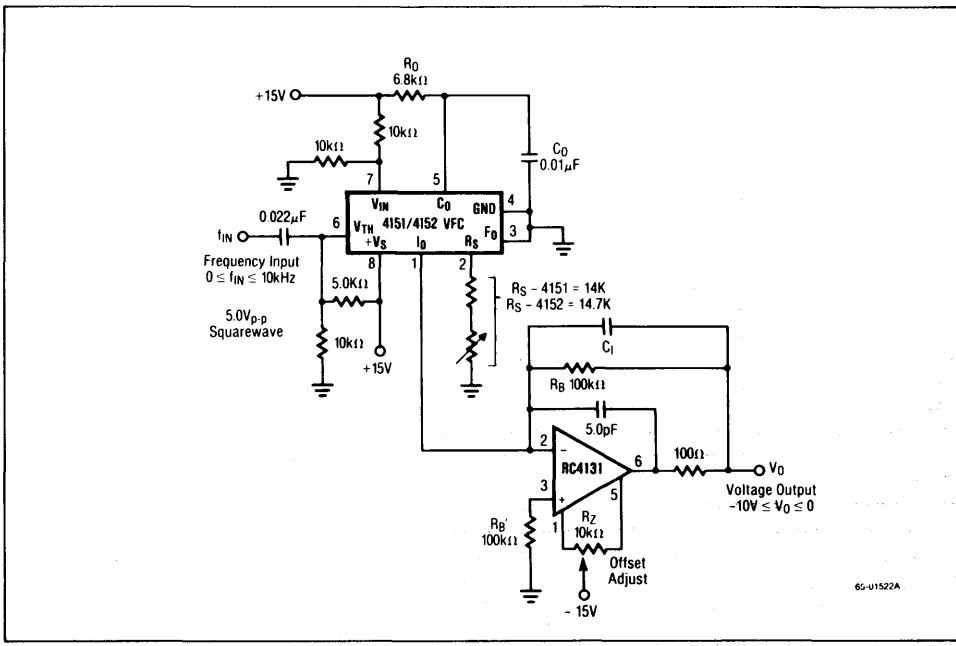


Figure 5. Precision FVC

Raytheon

Voltage-to-Frequency Converter

RC4153, 4153A

Features

- 0.1Hz to 250kHz dynamic range
- 0.01% F.S. maximum nonlinearity error — 0.1Hz to 10kHz
- 50ppm/°C maximum gain temperature coefficient (external reference)
- Few external components required

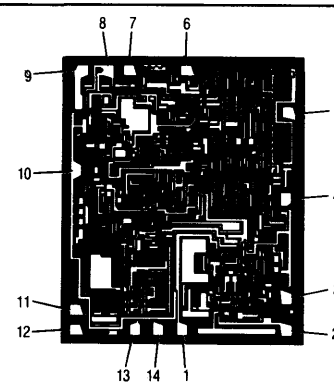
Applications

- Precision voltage-to-frequency converters
- Serial transmission of analog information
- Pulse width modulators
- Frequency-to-voltage converters
- A/D converters and long term integrators
- Signal isolation
- FSK modulation/demodulation
- Frequency scaling
- Motor speed controls
- Phase lock loop stabilization

Description

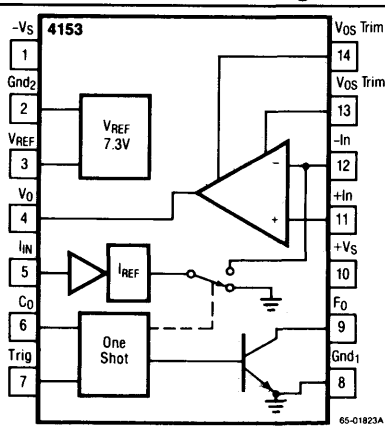
The 4153 sets a new standard for ease of application and high frequency performance in monolithic voltage-to-frequency converters. This voltage-to-frequency requires only four passive external components for precision operation, making it ideal for many low cost applications such as A/D conversion, frequency-to-voltage conversion, and serial data transmission. The improved linearity at high frequency makes it comparable to many dual slope A/D converters both in conversion time and accuracy, while retaining the benefits of voltage-to-frequency conversion, i.e., serial output, cost and size. The speed, accuracy, and temperature performance of the 4153 is achieved by incorporating high speed ECL logic, a high gain, wide bandwidth op amp, and a buried zener reference on a single monolithic chip.

Mask Pattern



Die Size: 90 x 108 mils
Min. Pad Dimensions: 4 x 4mils

4153 Functional Block Diagram



14 Lead
Dual In-Line Package
(Top View)

Pin	Function	Pin	Function
1	$-V_S$	8	Circuit Gnd
2	REF Gnd	9	Frequency Output (Open Collector)
3	V_{REF} Output	10	$+V_S$
4	V_{OUT} (Op Amp)	11	(+) Op Amp Input
5	I_{IN} (REF Input)	12	(-) Op Amp Input
6	C_O (Pulse Width)	13	V_{OS} Trim
7	Trigger Input	14	V_{OS} Trim

Absolute Maximum Ratings

Supply Voltage ..... ±18V
RA4153 ..... ±16V
Internal Power Dissipation 500mW
Input Voltage Range ..... $-V_S$ to $+V_S$
Output Sink Current (Freq. Output) 20mA
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range
RM4153 ..... -55°C to +125°C
RV4153, RV4153A ..... -40°C to +85°C
RC4153, RC4153A, RA4153 .... 0°C to +70°C

Thermal Characteristics

	14-Lead Ceramic DIP
Max. Junction Temp.	175°C
Max. P_D T_A < 50°C	1042mW
Therm. Res. θ_{JC}	60°C/W
Therm. Res. θ_{JA}	120°C/W
For T_A > 50°C Derate at	8.33mW per °C

Ordering Information

Part Number	Package	Operating Temperature Range
RC4153ADC	Ceramic	0°C to +70°C
RC4153DC	Ceramic	0°C to +70°C
RA4153DC	Ceramic	0°C to +70°C
RV4153DC	Ceramic	-40°C to +85°C
RM4153DC	Ceramic	-55°C to +125°C
RM4153DE/883B*	Ceramic	-55°C to +125°C

*MIL-STD-883, Level B Processing

Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise noted)

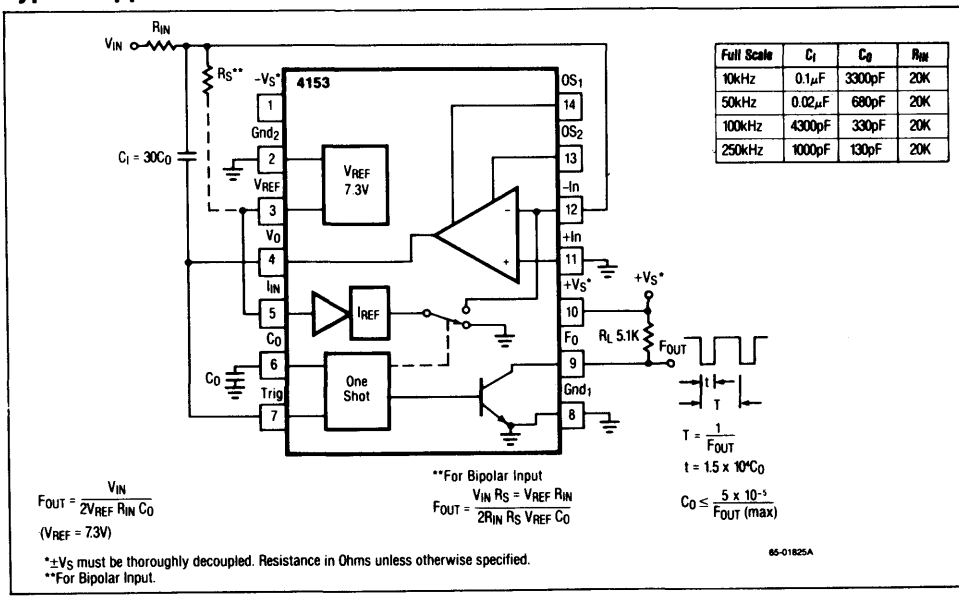
	4153A			4153			RA4153			
Parameters	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
Power Supply Requirements Supply Voltage	±12	±15	±18	±12	±15	±18	±12	±15	±16	V
Supply Current (I_O = 0, Pos) (I_O = 0, Neg)		+4.2 -7	+7.5 -10		+4.2 -7	+7.5 -10		+4.2 -7	+10 -15	mA
Full Scale Frequency	250	500		250	500			500		kHz
Transfer Characteristics Nonlinearity Error Voltage-to-Frequency[1] 0.1Hz ≤ F_{OUT} ≤ 10kHz		0.002	0.01		0.002	0.01		0.002	0.02	%FS
1.0Hz ≤ F_{OUT} 100kHz		0.025	0.05		0.025	0.05		0.025		%FS
5.0Hz ≤ F_{OUT} ≤ 250kHz		0.06	0.1		0.06	0.1		0.06		%FS
Nonlinearity Error Frequency-to-Voltage[1] 0.1Hz ≤ F_{IN} ≤ 10kHz		0.002	0.01		0.002	0.01		0.002	0.02	%FS
1.0Hz ≤ F_{IN} ≤ 100kHz		0.05	0.1		0.05	0.1		0.05		%FS
5.0Hz ≤ F_{IN} ≤ 250kHz		0.07	0.12		0.07	0.12		0.07		%FS

Electrical Characteristics (Continued)

Parameters	4153A			4153			RA4153			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Scale Factor Tolerance, F = 10kHz $K = \frac{1}{2V_{REF} R_{IN} C_O}$		±0.5			±0.5		-10	±0.5	+10	%
Change of Scale Factor With Supply		0.008			0.008			0.008		%/V
Reference Voltage (V_{REF})		7.3			7.3			7.3		V
Temperature Stability (0°C to +70°C)[1,2]										
Scale Factor		±50	±100		±75	±150		±75		ppm/°C
Reference Voltage		±25	±50		±50	±100		±50		ppm/°C
Scale Factor (External Ref) 10kHz FS		±25	±50		±25	±50		±25		ppm/°C
Scale Factor (External Ref) 100kHz FS		±50	±100		±50	±100		±50		ppm/°C
Scale Factor (External Ref) 250kHz FS		±100	±150		±100	±150		±100		ppm/°C
Op Amp										
Open Loop Output Resistance		230			230			230		Ω
Short Circuit Current		25			25			25		mA
Gain Bandwidth Product	2.5	3.0		2.5	3.0			3.0		MHz
Slew Rate	0.5	2.0		0.5	2.0			2.0		V/μS
Output Voltage Swing ($R_L \geq 2K$)	0 to +10	-0.5 to +14.3		0 to +10	-0.5 to +14.3		0 to +10	-0.5 to +14.3		V
Input Bias Current		70	400		70	400		70	800	nA
Input Offset Voltage (Adjustable to 0)		0.5	5.0		0.5	5.0		0.5	5.0	mV
Input Offset Current		30	60		30	60		30	300	nA
Input Resistance (Differential Mode)		1.0			1.0			1.0		MΩ
Common Mode Rejection Ratio	75	100		75	100			100		dB
Power Supply Rejection Ratio	70	106		70	106		62	106		dB
Large Signal Voltage Gain	25	350		25	350			350		V/mV
Switched Current Source										
Reference Current (Ext Ref)		1.0			1.0			1.0		mA
Digital Input (Frequency-to-Voltage, Pin 7)										
Logic "0"			0.5			0.5			0.4	V
Logic "1"	2.0			2.0			2.2			V
Trigger Current		-50			-50			-50		μA
Logic Output (Open Collector)										
Saturation Voltage (Pin 9)										
I_{SINK} = 4mA		0.15	0.4		0.15	0.4		0.15		V
I_{SINK} = 10mA		0.4	1.0		0.4	1.0		0.4		V
Leakage Current (Off State)		150			150			150		nA

Notes: 1. Guaranteed but not tested. 2. V_{REF} Range 6.6V ≤ VR ≤ 8.0V.

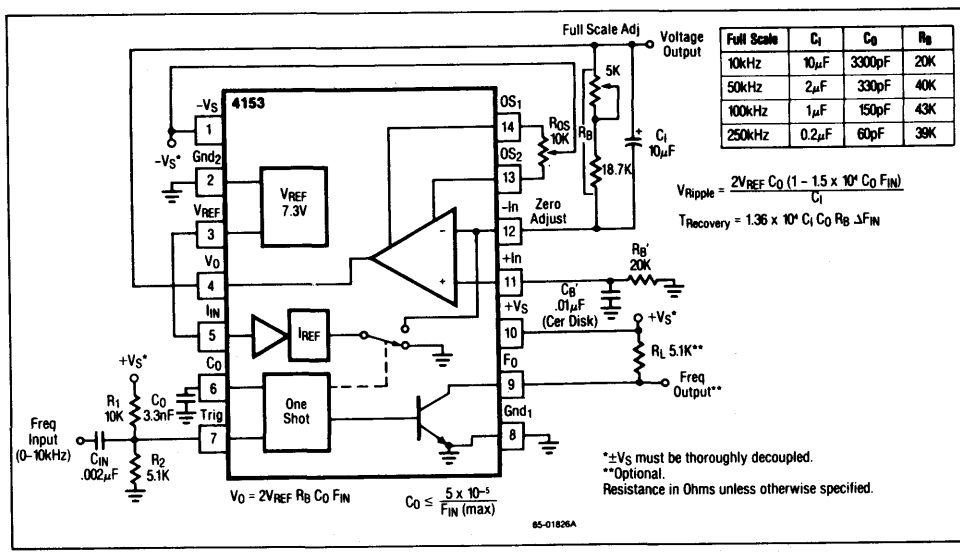
Typical Application Circuits



Full Scale	CI	CO	RIN
10kHz	0.1μF	3300pF	20K
50kHz	0.02μF	680pF	20K
100kHz	4300pF	330pF	20K
250kHz	1000pF	130pF	20K

*±VS must be thoroughly decoupled. Resistance in Ohms unless otherwise specified.
**For Bipolar Input.

Figure 1. Voltage-to-Frequency Converter Minimum Circuit

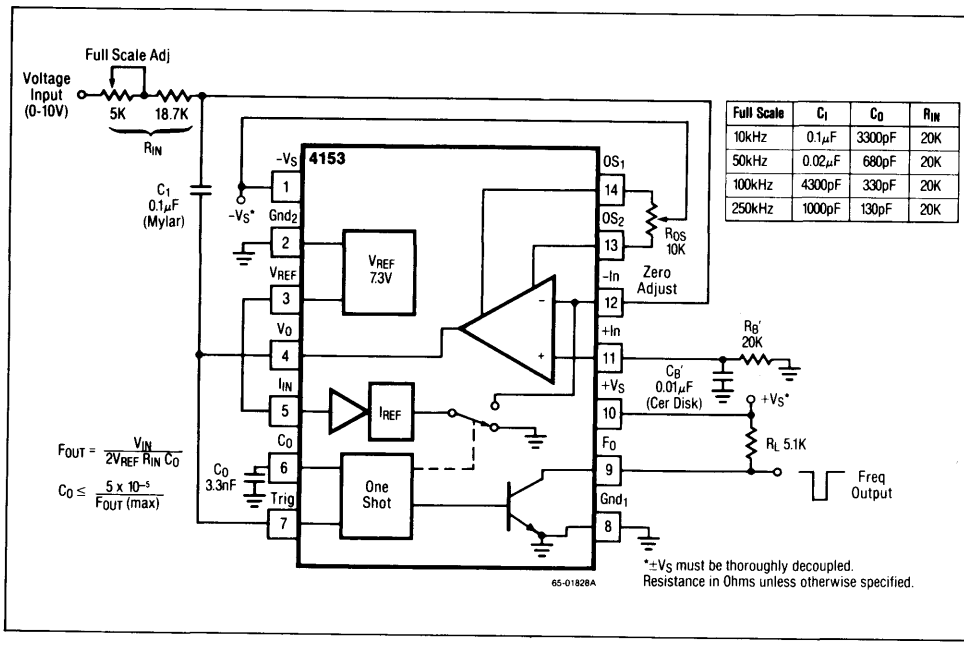


Full Scale	CI	CO	RB
10kHz	10μF	3300pF	20K
50kHz	2μF	330pF	40K
100kHz	1μF	150pF	43K
250kHz	0.2μF	60pF	39K

*±VS must be thoroughly decoupled.
**Optional.
Resistance in Ohms unless otherwise specified.

Figure 2. Frequency-to-Voltage Converter — V_O (Volts) = F_{IN} (kHz) — 100kHz Max

Typical Application Circuits (Continued)



Full Scale	C_I	C_O	R_{IN}
10kHz	0.1μF	3300pF	20K
50kHz	0.02μF	680pF	20K
100kHz	4300pF	330pF	20K
250kHz	1000pF	130pF	20K

Figure 3. Voltage-to-Frequency Converter With Offset and Gain Adjusts

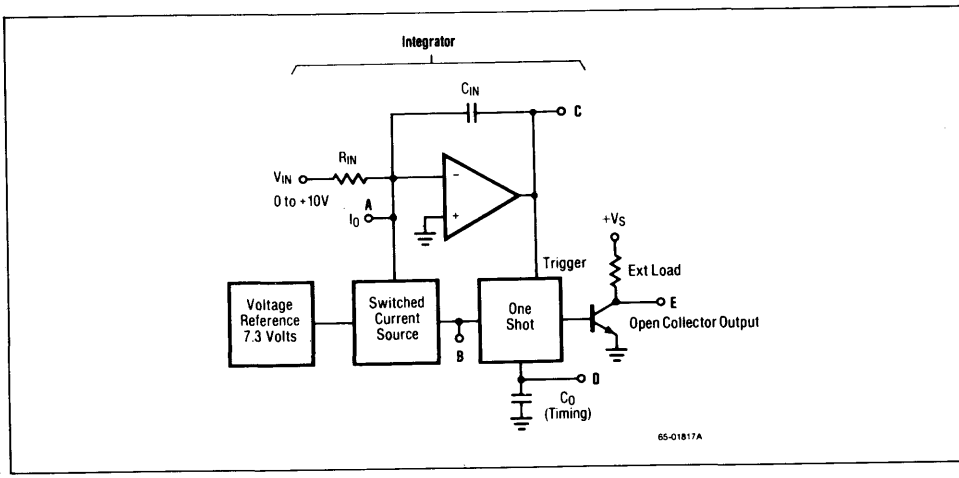


Figure 4. VFC Block Diagram

Principles of Operation

The 4153 consists of several functional blocks which provide either voltage-to-frequency or frequency-to-voltage conversion, depending on how they are connected. The operation is best understood by examining the block diagram as it is powered in a voltage-to-frequency mode.

When power is first applied, all capacitors are discharged. The input current, V_{IN}/R_{IN}, causes C_{IN} to charge, and point **C** will try to ramp down. The trigger threshold of the one-shot is approximately +1.3V, and if the integrator output is less than +1.3V, the one-shot will fire and pulse the open collector output **E** and the switched current source **A** (see Figures 4 and 5). Because the point **C** is less than +1.3V, the one-shot fires, and the switched current source delivers a negative current pulse to the integrator. This causes C_{IN} to charge in the opposite direction, and point **C** will ramp up until the end of the one-shot pulse. At that time, the positive current V_{IN}/R_{IN} will again make point **C** ramp down until the trigger threshold is reached.

When power is applied, the one-shot will continuously fire until the integrator output exceeds the trigger threshold. Once this is reached, the

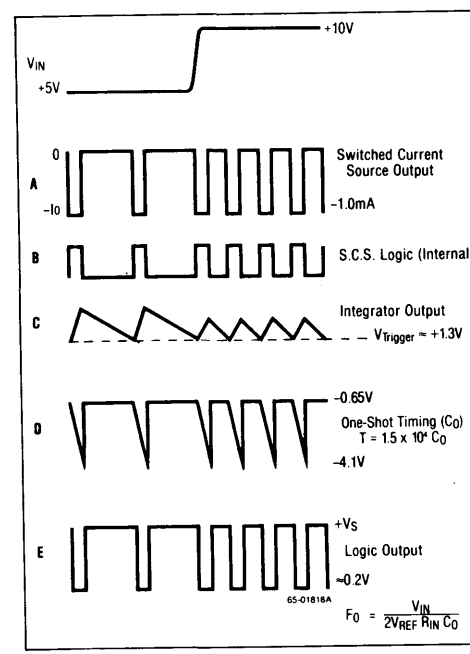


Figure 5. 4153 Voltage-to-Frequency Timing Waveforms

one-shot will fire as needed to keep the integrator output above the trigger threshold. If V_{IN} is increased, the slope of the downward ramp increases, and the one-shot will fire more often in order to keep the integrator output high. Since the one-shot firing frequency is the same as the open collector output frequency, any increase in V_{IN} will cause an increase in F_{OUT}. This relationship is very linear because the amount of charge in each I_{OUT} pulse is carefully defined, both in magnitude and duration. The duration of the pulse is set by the timing capacitor C_O (point **D**). This feedback system is called a charge balanced loop.

The scale factor (the number of pulses per second for a specified V_{IN}) is adjusted by changing either R_{IN} and therefore I_{IN}, or by changing the amount of charge in each I_O pulse. Since the magnitude of I_O is fixed at 1 milliamp, the way to change the amount of charge is by adjusting the one-shot duration set by C_O. (I_O may be adjusted by changing V_{REF}.) The accuracy of the relationship between V_{IN} and F_{OUT} is affected by three major sources of error: temperature drift, nonlinearity, and offset.

The total temperature drift is the sum of the individual drift of the components that make up the system. The greatest source of drift in a typical application is in the timing capacitor, C_O. Low temperature coefficient capacitors, such as silver mica and polystyrene, should be measured for drift, using a capacitance meter. Experimentation has shown that the lowest tempco's are achieved by wiring a parallel capacitor composed of 70% silver mica and 30% polystyrene.

The reference on the chip can be replaced by an external reference with much tighter drift specifications, such as an LM199. The 199s 6.9V output is close to the 4153s 7.3V output, and has less than 10 ppm/°C drift.

Nonlinearity is primarily caused by changes in the precise amount of charge in each I_{OUT} pulse. As frequency increases, internal stray capacitances and switching problems change the width and amplitude of the I_{OUT} pulses, causing a nonlinear relationship between V_{IN} and F_{OUT}. For this reason, the scale factor you choose should be below 1kHz/V or as low as the acquisition time of your system will allow.

Nonlinearity is also affected by the ratio of C_I to C_O. Less error can be achieved by increasing the value of C_I, but this affects response time and temperature drift. Optimum values for C_I and C_O are shown in the tables in Figures 1, 2, and 3. These values represent the best compromise of nonlinearity and temperature drift. Polypropylene, mylar or polystyrene capacitors should be used for C_I.

The accuracy at low input voltages is limited by the offset and V_{OS} drift of the op amp. To improve this condition, an offset adjust is provided.

Once your system is running, it may be calibrated as follows: apply a measured full scale input voltage and adjust R_{IN} until the scale factor is correct. For precise applications, trimming by soldering metal film resistors in parallel is recommended instead of trimpots, which have bad tempco's and are easily taken out of adjustment by mechanical shock. After the scale factor is calibrated, apply a known small input voltage (approximately 10mV) and adjust the op amp offset until the output frequency equals the input multiplied by the scale factor.

The output **E** consists of a series of negative going pulses with a pulse width equal to the one-shot time. The open collector pull up resistor may be connected to a different supply (such as +5V for TTL) as long as it does not exceed the value of $+V_S$ applied to pin 10. The load current should be kept below 10mA in order to minimize strain on the device. Pins 2 and 8 must be grounded in all applications, even if the open collector transistor is not used.

Figure 6 shows the complete circuit for a precision frequency-to-voltage converter. This circuit converts an input frequency to a proportional voltage by integrating the switched current source output. As the input frequency increases, the number of I_{OUT} pulses delivered to the integrator increases, thus increasing the average output voltage. Depending on the time constant of the

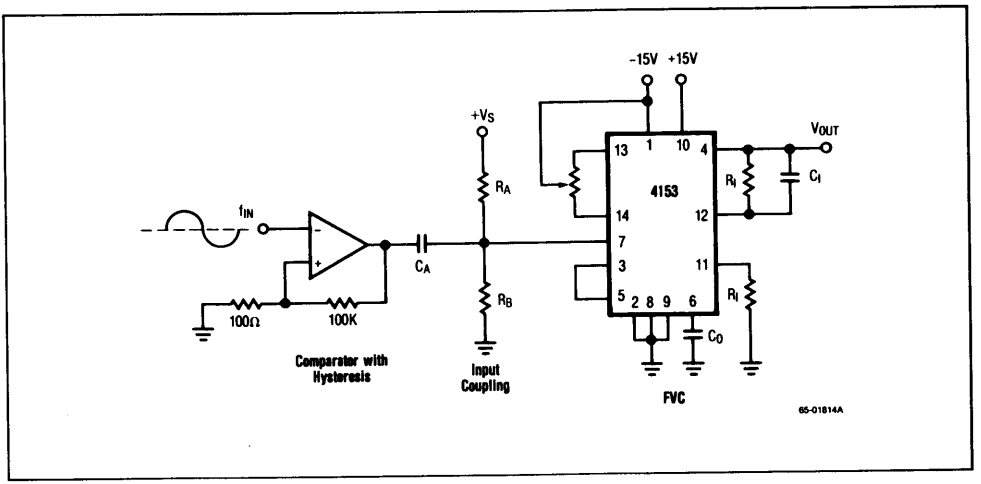


Figure 6. FVC Input Conditioning

integrator, there will be some ripple on the output. The output may be further filtered, but this will reduce the response time. A second order filter will decrease ripple and improve response time.

The output waveform must meet three conditions for proper frequency-to-voltage operation. First, it must have sufficient amplitude and offset to swing above and below the 1.3V trigger threshold. (See Figure 6 for an example of AC coupling and offset bias.) Second, it must be a fast slewing waveform having a quick rise time. A comparator may be used to square it up. Finally, the input pulse width must not exceed the one-shot time, in order to avoid retriggering the one-shot (AC couple the input).

Capacitive coupling between the trigger input and the timing capacitor pin may occur if the input waveform is a squarewave or the input has a short period. This can cause gross nonlinearity due to changes in the one-shot timing waveform (see Figure 7). This problem can be avoided by keeping the value of C_O small, and thereby keeping the timing period less than the input waveform period.

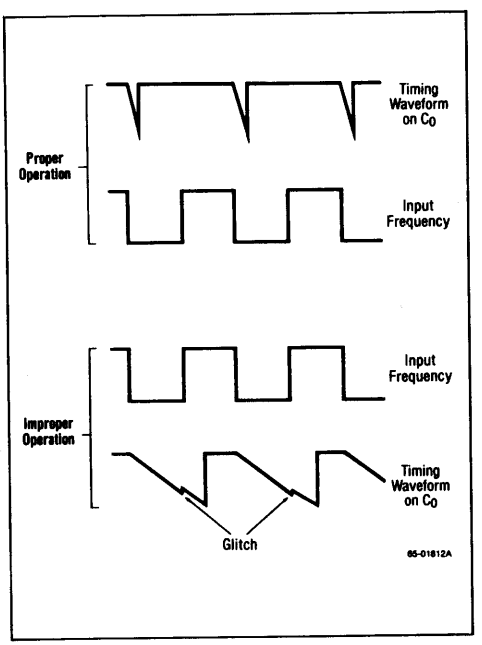


Figure 7. FVC Timing Waveform

Detailed Circuit Operation

The circuit consists of a buried zener reference (breakdown occurs below the surface of the die, reducing noise and contamination), a high speed one-shot, a high speed switched precision voltage-to-current converter, and an open collector output transistor.

Figure 8 shows a block diagram of the high speed one-shot and Figure 9 shows the monolithic implementation. A trigger pulse sets the R-S latch, which lets C_O charge from I_T. When the voltage on C_O exceeds V_{TH}, the comparator resets the latch and discharges C_O. Looking at the detailed schematic, a positive trigger voltage turns on Q5, turns off Q4, and turns on Q3. Q3 provides more drive to Q5 keeping it on and latching the base of Q11 low. This turns on the switched current source and turns off Q1, allowing C_O to charge in a negative direction. When the voltage on C_O exceeds V_{TH}, Q13's collector pulls Q3's base down, resetting the latch, turning off the switched current source and discharging C_O through Q1. Note that all of the transistors in the signal path are NPNs and that the voltage swings are minimized ECL fashion to reduce delays. Minimum delay means minimum drift of the resultant VFC scale factor at high frequency.

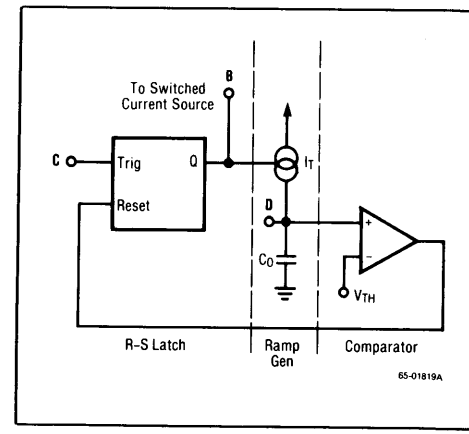


Figure 8. One-Shot Block Diagram

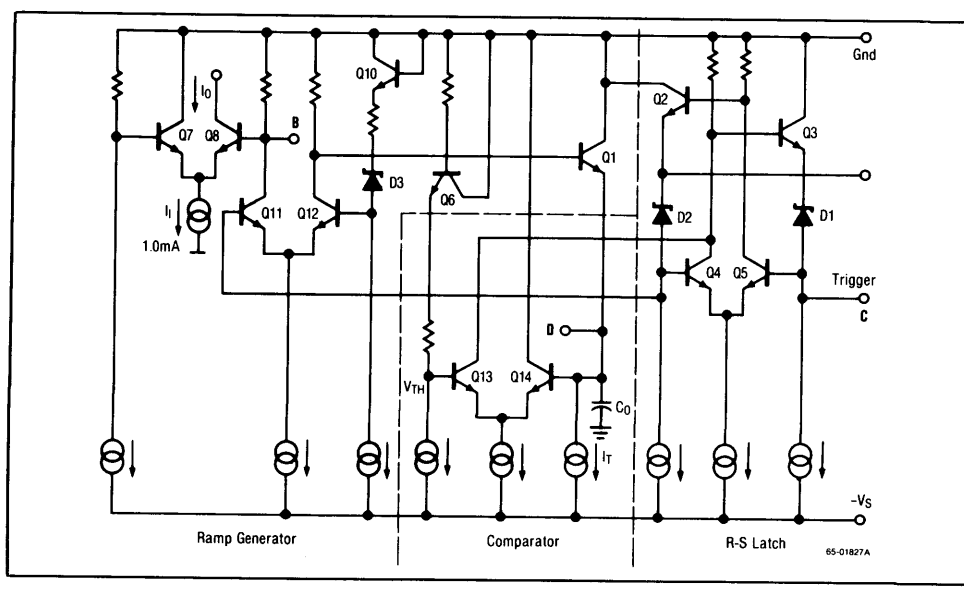


Figure 9. One-Shot Detail

The switched current source is shown as a block diagram in Figure 10 and detailed in Figure 11. The summing node (+ input of op amp) is held at 0V by the amplifier feedback, causing V_{REF} to be applied across R60. This current (V_{REF}/R60), minus the small amplifier bias current, flows through Q35. Q35 develops a V_{BE} dependent on that current. This V_{BE} is developed across Q36. Since Q35 and Q36 are equal in area, their currents are equal. This mirrored current is switched by the one-shot output.

The detail schematic shows the amplifier and load (Q21 through Q34), the mirror transistors (Q35, Q36) and the differential switching transistors (Q7, Q8). The amplifier uses a complementary paraphase input composed of Q21 through Q26 with a current mirror formed by Q27 through Q30, which converts from differential to single ended output. Level shift diodes

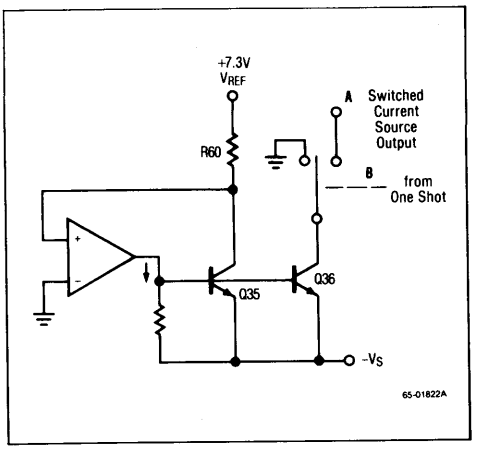


Figure 10. Switched Current Source Simplified Diagram

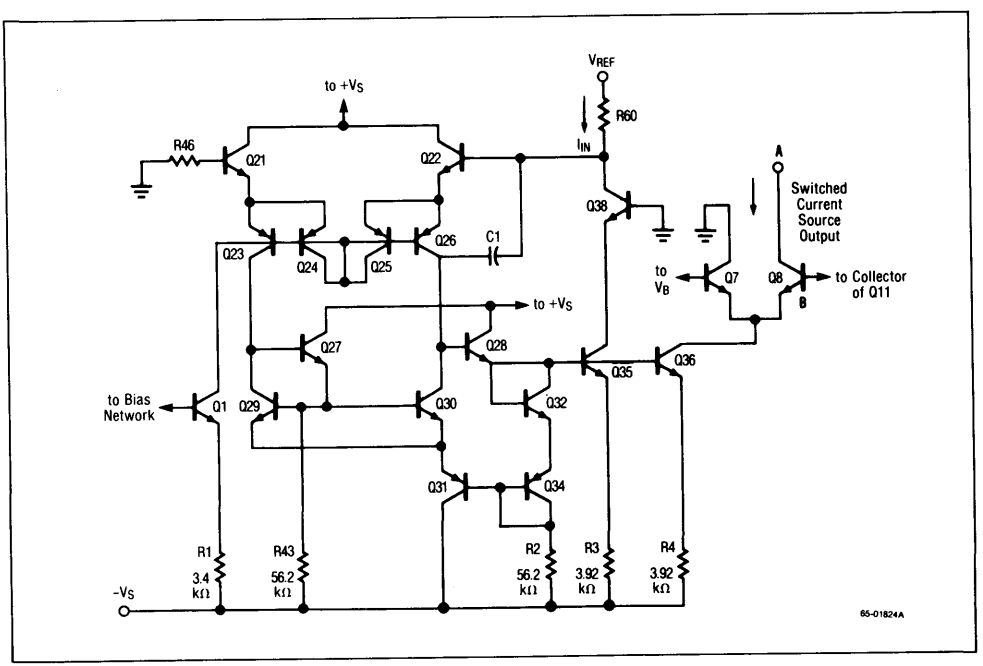
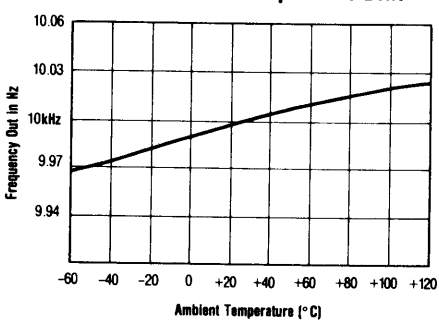


Figure 11. Switched Current Source (Detail)

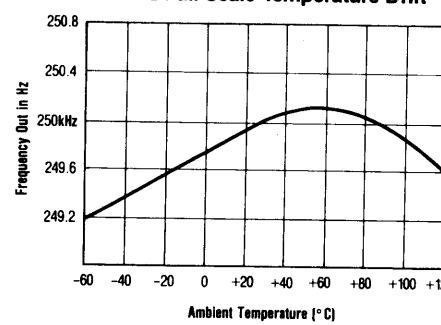
Q32 and Q34 and emitter follower Q31 bootstrap the emitters of the mirror devices Q29 and Q30 to increase gain and lower input offsets, which would otherwise be caused by unbalanced collector voltages on Q23 and Q26. Matching emitter currents in Q35 and Q36 are assured by degeneration resistors R3 and R4. The differential switch allows the current source to remain active continuously, shunting to ground in the off state. This helps stabilize the output, and again, NPNs reduce switching time, timing errors, and most important, drift of timing errors over temperature.

Typical Performance Characteristics

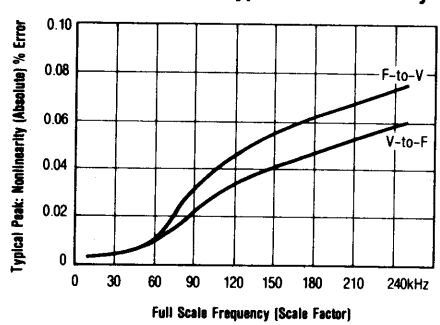
4153 10kHz Full Scale Temperature Drift



4153 250kHz Full Scale Temperature Drift

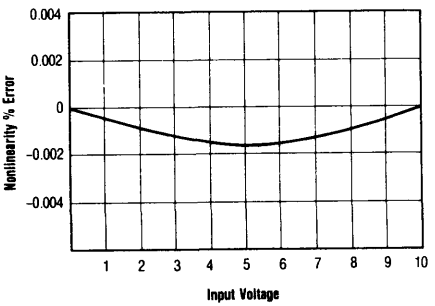


4153 Scale Factor vs. Typical Peak Linearity

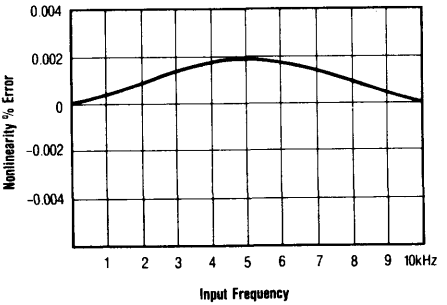


Typical Performance Characteristics (Continued)

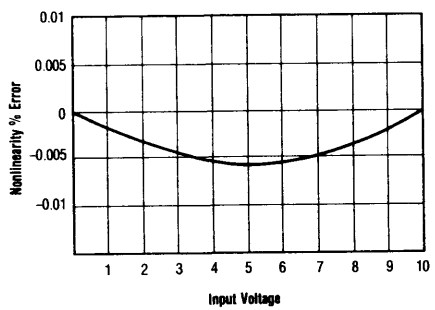
4153 10kHz Voltage-to-Frequency Nonlinearity



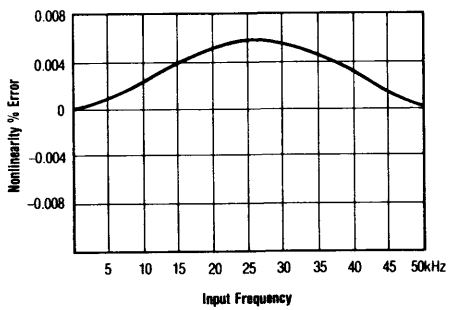
4153 10kHz Frequency-to-Voltage Nonlinearity



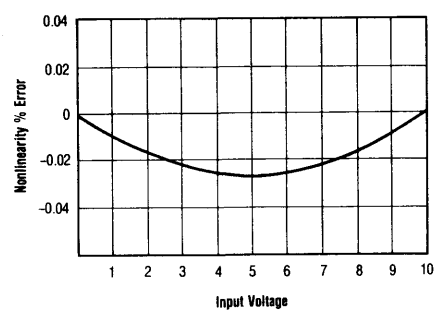
4153 50kHz Voltage-to-Frequency Nonlinearity



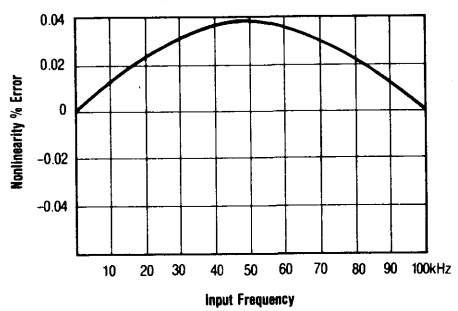
4153 50kHz Frequency-to-Voltage Nonlinearity



4153 100kHz Voltage-to-Frequency Nonlinearity

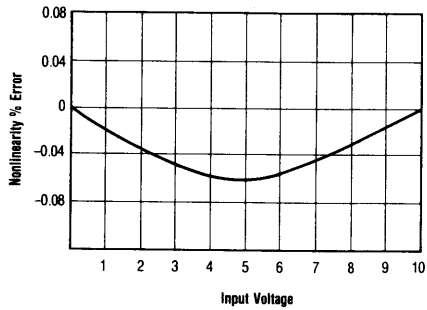


4153 100kHz Frequency-to-Voltage Nonlinearity

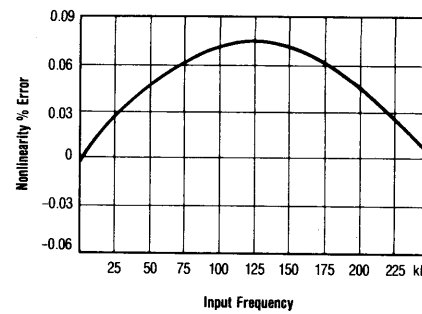


Typical Performance Characteristics (Continued)

4153 250kHz Frequency-to-Voltage Nonlinearity



4153 250kHz Voltage-to-Frequency Nonlinearity



Section 10
Voltage References

Raytheon's REF series of precision voltage references are functionally similar to ordinary three terminal fixed voltage regulators, as opposed to zener type references which require external components and often need output buffering. The REF series accept positive supply voltages and regulate to a lower output voltage, just like a three terminal regulator, but have much better temperature drift, line and load regulation, and initial accuracy specifications.

The REF series is grouped by nominal output voltage:

REF-01	+10V output
REF-02	+5V output
REF-03	+2.5V output

The REF-03 will accept a +5V TTL power supply as its supply voltage.

DEFINITIONS

Line Regulation
The ratio of change in output voltage to the change in supply (line) voltage effecting it, expressed as a percentage of the output voltage per volt change in supply voltage (%/V).

Load Regulation
The ratio of change in output voltage to the change in load (output) current effecting it, measured in percent of output voltage per milliamp change in load current (%/mA).

Output Voltage Noise
Output voltage noise is the broadband noise over a specified range of frequencies, measured in microvolts peak-to-peak (μV_{p-p}).

Short Circuit Current
The maximum output current available from the regulator with the output shorted to ground, expressed in milliamps (mA).

Sink Current
The amount of current that can be forced into the output with the reference still within ±3% regulation, expressed in milliamps (mA).

Supply Current (I_S)
The current required from the power supply to operate the regulator under quiescent no-load conditions, expressed in milliamps (mA).

Supply Voltage (V_S)
The range of power supply voltages over which the regulator will operate, expressed in volts (V).

Raytheon

+10V Precision Voltage References

REF-01

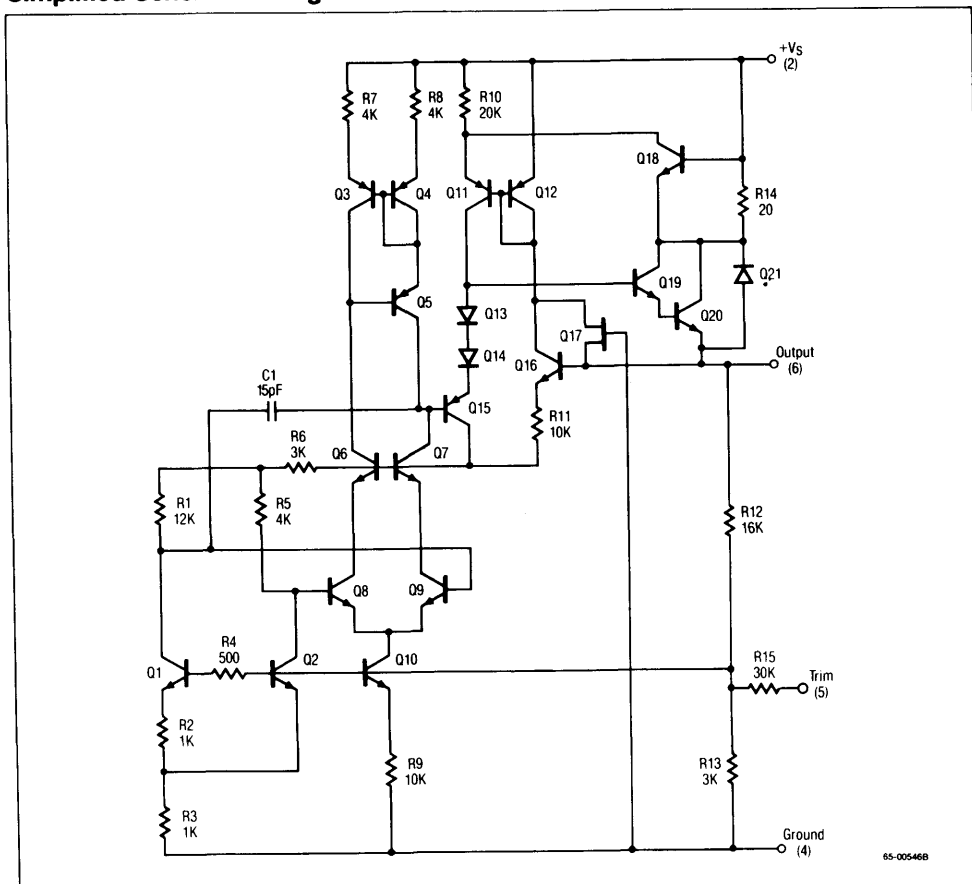
Features

- +10 Volt output — ±0.3%
- Adjustable — ±3%
- Excellent temperature stability — 3ppm/°C
- Low noise — $20\mu V_{p-p}$
- Wide input voltage range — +12V to +40V
- No external components
- Short circuit proof
- Low power consumption — 15mW

Description

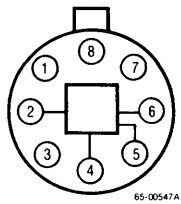
The REF-01 Precision Voltage Reference contains a bandgap reference using thin film resistors, a step-up amplifier, short circuit protection, and a zener trim network. The REF-01's +10V output shows excellent stability for large changes of temperature, load current, and input voltage. An adjust pin is provided that can change the output voltage by at least 3% with little effect on temperature coefficient.

Simplified Schematic Diagram



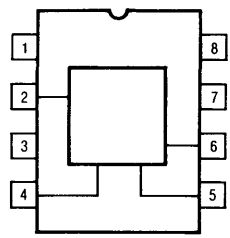
Connection Information

8-Lead TO-99 Metal Can (Top View)



65-00547A

8-Lead Ceramic Dual In-Line (Top View)



65-00548A

Pin	Function
1	No Connection
2	$+V_S$
3	No Connection
4	Ground
5	Adjust
6	Output
7	No Connection
8	No Connection

Ordering Information

Part Number	Package	Operating Temperature Range
REF-01EDE	Ceramic	0°C to +70°C
REF-01HDE	Ceramic	0°C to +70°C
REF-01CDE	Ceramic	0°C to +70°C
REF-01DDE	Ceramic	0°C to +70°C
REF-01ET	TO-99	0°C to +70°C
REF-01HT	TO-99	0°C to +70°C
REF-01CT	TO-99	0°C to +70°C
REF-01DT	TO-99	0°C to +70°C
REF-01ADE	Ceramic	-55°C to +125°C
REF-01ADE/883B*	Ceramic	-55°C to +125°C
REF-01DE	Ceramic	-55°C to +125°C
REF-01DE/883B*	Ceramic	-55°C to +125°C
REF-01AT	TO-99	-55°C to +125°C
REF-01AT/883B*	TO-99	-55°C to +125°C
REF-01T	TO-99	-55°C to +125°C
REF-01T/883B*	TO-99	-55°C to +125°C

*MIL-STD-883, Level B Processing

Thermal Characteristics

	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can
Max. Junction Temp.	175°C	175°C
Max. P_D $T_A < 50°C$	833mW	658mW
Therm. Res. θ_{JC}	45°C/W	50°C/W
Therm. Res. θ_{JA}	150°C/W	190°C/W
For $T_A > 50°C$ Derate at	8.33mW per °C	5.26mW per °C

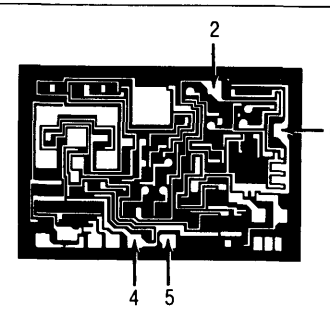
Absolute Maximum Ratings

Supply Voltage
- REF-01, A, E, H Grades ..... +40V
- REF-01C, D Grades ..... +30V

Internal Power Dissipation 500mW
Output Short Circuit Duration ..... Indefinite
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range
- REF-01A, -01 ..... -55°C to +125°C
- REF-01E, H, C, D ..... 0°C to +70°C

Lead Soldering Temperature (60 Sec) ..... +300°C

Mask Pattern



Die Size: 78 x 54 mils
Min. Pad Dimensions: 4 x 4 mils

Electrical Characteristics (V_S = +15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	REF-01A/E			REF-01/H			Units
		Min	Typ	Max	Min	Typ	Max	
Output Voltage	I_L = 0mA	9.97	10.00	10.03	9.95	10.00	10.05	V
Output Adjustment Range	R_P = 10kΩ	±3.0	±3.3		±3.0	±3.3		%
Output Voltage Noise[1]	0.1Hz to 10Hz		20	30		20	30	μV_{p-p}
Supply Voltage		12		40	12		40	V
Line Regulation[2]	V_S = +13V to +33V		0.006	0.010		0.006	0.010	%/V
Load Regulation[2]	I_L = 0mA to 10mA		0.005	0.008		0.006	0.010	%/mA
Turn-on Settling Time	To ±0.1% of Final Value		5.0			5.0		μS
Supply Current	No Load		1.0	1.4		1.0	1.4	mA
Load Current		10	21		10	21		mA
Sink Current		-0.3	-0.5		-0.3	-0.5		mA
Short Circuit Current	V_O = 0		30			30		mA

Electrical Characteristics (V_S = +15V and -55°C ≤ T_A ≤ +125°C unless otherwise noted)

Parameters	Test Conditions	REF-01A			REF-01			Units
		Min	Typ	Max	Min	Typ	Max	
Output Voltage Change With Temperature[3,4]	Over Temp. Range		0.06	0.15		0.18	0.45	%
Output Voltage Temperature Coefficient[5]	Over Temp. Range		3.0	8.5		10	25	ppm/°C
Change in V_{OUT} Temperature Coefficient With Output Adjustment	R_P = 10kΩ		0.7			0.7		ppm/%
Line Regulation[2]	V_S = +13V to +33V		0.009	0.015		0.009	0.015	%/V
Load Regulation[2]	I_O = 0mA to 8mA		0.007	0.012		0.007	0.012	%/mA

Notes:
1. Guaranteed by design.
2. Line and load regulation specifications include the effects of self heating.
3. Output voltage change with temperature = $\frac{V_{MAX} - V_{MIN}}{10V} \times 100\%$
4. Output voltage change with temperature specification applies untrimmed, or trimmed to +10V.
5. Output voltage temperature coefficient = $\frac{\text{Output voltage change with temperature}}{180°C}$

Electrical Characteristics (V_S = +15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	REF-01C			REF-01D			Units
		Min	Typ	Max	Min	Typ	Max	
Output Voltage	I_L = 0mA	9.90	10.00	10.10	9.850	10.00	10.150	V
Output Adjustment Range	R_P = 10kΩ	±2.7	±3.3		±2.0	±3.3		%
Output Voltage Noise[1]	0.1Hz to 10Hz		25	35		25		μV_{p-p}
Supply Voltage		12		30	12		30	V
Line Regulation[2]	V_S = +13V to +33V		0.009	0.015		0.012	0.04	%/V
Load Regulation[2]	I_L = 0mA to 8mA		0.006	0.015				%/mA
	I_L = 0mA to 4mA		0.006	0.015		0.009	0.04	
Turn-on Settling Time	To ±0.1% of Final Value		5.0			5.0		μS
Supply Current	No Load		1.0	1.6		1.0	2.0	mA
Load Current		8.0	21		8.0	21		mA
Sink Current		-0.2	-0.5		-0.2	-0.5		mA
Short Circuit Current	V_O = 0		30			30		mA

Electrical Characteristics (V_S = +15V, 0°C ≤ T_A ≤ +70°C, and I_O = 0 unless otherwise noted)

Parameters	Test Conditions	REF-01E			REF-01H			Units
		Min	Typ	Max	Min	Typ	Max	
Output Voltage Change With Temperature[3,4]	Over Temp. Range		0.02	0.06		0.07	0.17	%
Output Voltage Temperature Coefficient[5]	Over Temp. Range		3.0	8.5		10	25	ppm/°C
Change in V_{OUT} Temperature Coefficient With Output Adjustment	R_P = 10kΩ		0.7			0.7		ppm/%
Line Regulation[2]	V_S = +13V to +33V		0.007	0.012		0.007	0.012	%/V
Load Regulation[2]	I_L = 0mA to 8mA		0.006	0.010		0.007	0.012	%/mA

Notes: 1. Guaranteed by design.
2. Line and load regulation specifications include the effects of self heating.
3. Output voltage change with temperature = $\frac{V_{MAX} - V_{MIN}}{10V} \times 100\%$
4. Output voltage change with temperature specification applies untrimmed, or trimmed to +10V.
5. Output voltage temperature coefficient = $\frac{\text{Output voltage change with temperature}}{70°C}$

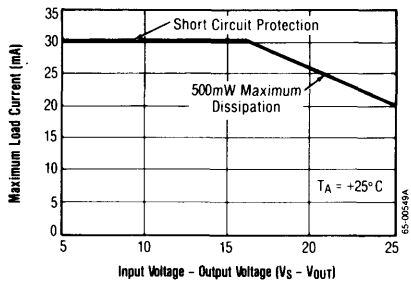
Electrical Characteristics (V_S = +15V, 0°C ≤ T_A ≤ +70°C, and I_O = 0 unless otherwise noted)

Parameters	Test Conditions	REF-01C			REF-01D			Units
		Min	Typ	Max	Min	Typ	Max	
Output Voltage Change With Temperature[3,4]	Over Temp. Range		0.14	0.45		0.49	1.7	%
Output Voltage Temperature Coefficient[5]	Over Temp. Range		20	65		70	250	ppm/°C
Change in V_{OUT} Temperature Coefficient With Output Adjustment	R_P = 10kΩ		0.7			0.7		ppm/%
Line Regulation[2]	V_S = +13V to +30V		0.011	0.018		0.020	0.025	%/V
Load Regulation[2]	I_O = 0mA to 5mA		0.008	0.018		0.020	0.025	%/mA

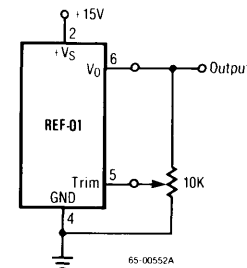
Notes: 1. Guaranteed by design.
2. Line and load regulation specifications include the effects of self heating.
3. Output voltage change with temperature = $\frac{V_{MAX} - V_{MIN}}{10V} \times 100\%$
4. Output voltage change with temperature specification applies untrimmed, or trimmed to +10V.
5. Output voltage temperature coefficient = $\frac{\text{Output voltage change with temperature}}{70°C}$

Typical Performance Characteristics

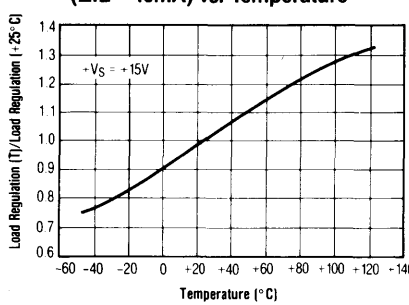
Maximum Load Current vs. Differential Input Voltage



Output Adjustment

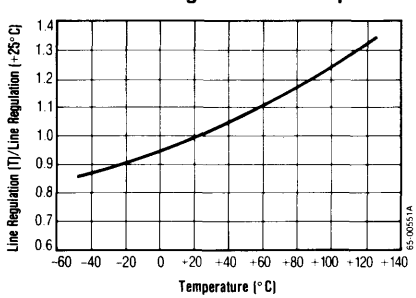


Normalized Load Regulation (ΔIL = 10mA) vs. Temperature

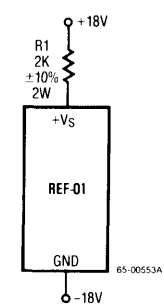


The REF-01 trim terminal can be used to adjust the output voltage over a 10V ±300mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 10V. Of course, the output can also be set to exactly 10.000V or to 10.240V for binary operation. Adjustment of the output does not significantly affect the temperature performance of the device. Typically the temperature coefficient change is 0.7ppm/°C for 100mV of output adjustment.

Normalized Line Regulation vs. Temperature

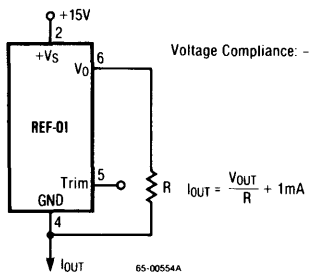


Burn-In Circuit

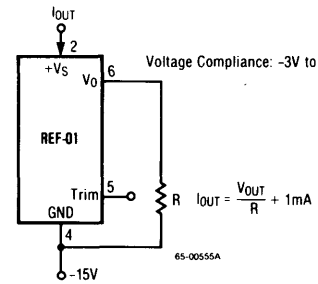


Typical Applications

Current Source



Current Sink



Raytheon

+5V Precision Voltage References

REF-02

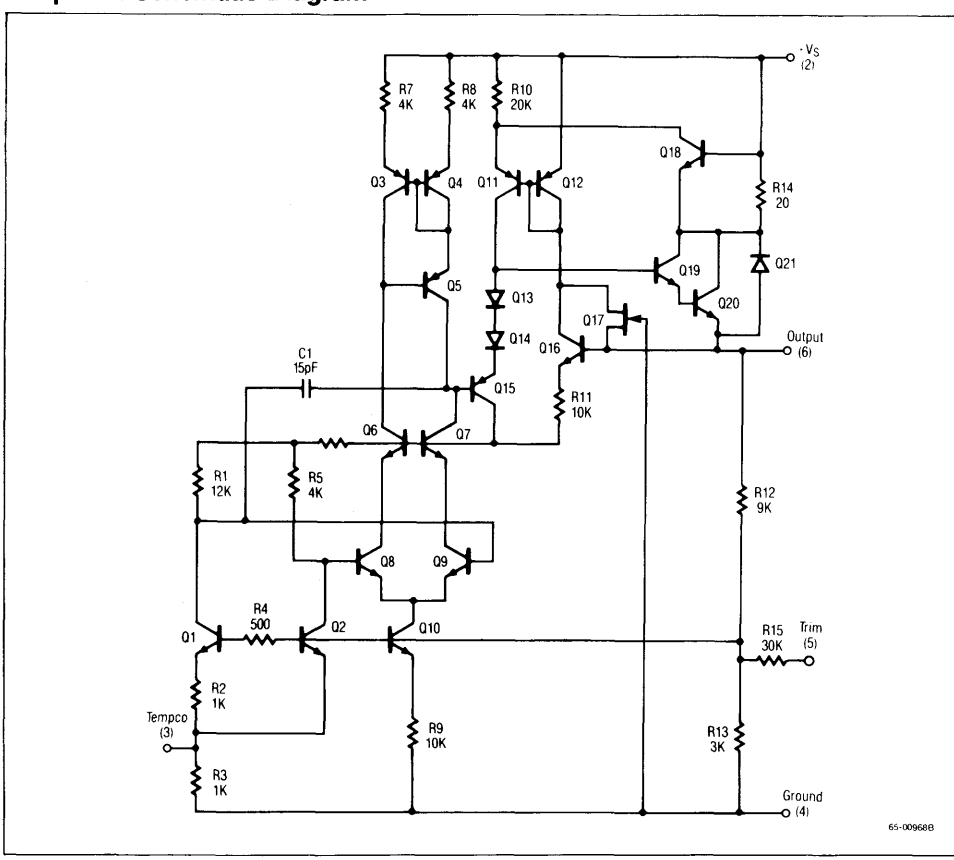
Features

- +5 Volt output — ±0.3%
- Adjustable — ±3%
- Excellent temperature stability — 3ppm/°C
- Low noise — $10\mu V_{p-p}$
- Wide input voltage range — +7V to +40V
- No external components
- Short circuit proof
- Low power consumption — 10mW

Description

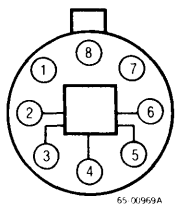
The REF-02 Precision Voltage Reference contains a bandgap reference using thin-film resistors, a step-up amplifier, short circuit protection, and a zener trim network. The REF-02's +5V output shows excellent stability for large changes of temperature, load current, and input voltage. An adjust pin is provided that can change the output voltage by at least 3% with little effect on temperature coefficient. A tempco pin also provides a voltage that varies linearly with temperature, typically from +470mV to +830mV over the military temperature range.

Simplified Schematic Diagram



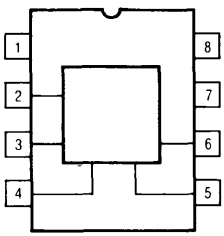
Connection Information

8-Lead TO-99 Metal Can (Top View)



65-00969A

8-Lead Ceramic Dual In-Line Package (Top View)



65-00970A

Pin	Function
1	No Connection
2	$+V_S$
3	Tempco
4	Ground
5	Adjust
6	Output
7	No Connection
8	No Connection

Ordering Information

Part Number	Package	Operating Temperature Range
REF-02EDE	Ceramic	0°C to +70°C
REF-02HDE	Ceramic	0°C to +70°C
REF-02CDE	Ceramic	0°C to +70°C
REF-02DDE	Ceramic	0°C to +70°C
REF-02ET	TO-99	0°C to +70°C
REF-02HT	TO-99	0°C to +70°C
REF-02CT	TO-99	0°C to +70°C
REF-02DT	TO-99	0°C to +70°C
REF-02ADE	Ceramic	-55°C to +125°C
REF-02ADE/883B*	Ceramic	-55°C to +125°C
REF-02DE	Ceramic	-55°C to +125°C
REF-02DE/883B*	Ceramic	-55°C to +125°C
REF-02AT	TO-99	-55°C to +125°C
REF-02AT/883B*	TO-99	-55°C to +125°C
REF-02T	TO-99	-55°C to +125°C
REF-02T/883B*	TO-99	-55°C to +125°C

*MIL-STD-883, Level B Processing

Thermal Characteristics

	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can
Max. Junction Temp.	175°C	175°C
Max. P_D $T_A < 50°C$	833mW	658mW
Therm. Res. θ_{JC}	45°C/W	50°C/W
Therm. Res. θ_{JA}	150°C/W	190°C/W
For $T_A > 50°C$ Derate at	8.33mW per °C	5.26mW per °C

Absolute Maximum Ratings

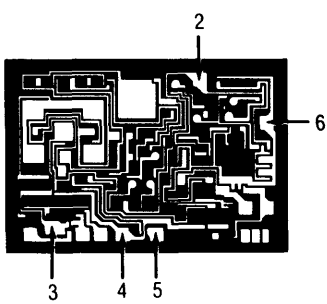
Supply Voltage
- REF-02, A, E, H Grades ..... +40V
- REF-02C, D Grades ..... +30V

Internal Power Dissipation 500mW
Output Short Circuit Duration ..... Indefinite
Storage Temperature
- Range ..... -65°C to +150°C

Operating Temperature Range
- REF-02A, -02 ..... -55°C to +125°C
- REF-02E, H, C, D ..... 0°C to +70°C

Lead Soldering Temperature
- (60 Sec) ..... +300°C

Mask Pattern



Die Size: 78 x 54 mils
Min. Pad Dimensions: 4 x 4 mils

Electrical Characteristics (V_S = +15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	REF-02A/E			REF-02/H			Units
		Min	Typ	Max	Min	Typ	Max	
Output Voltage	I_L = 0mA	4.985	5.000	5.015	4.975	5.000	5.025	V
Output Adjustment Range	R_P = 10kΩ	±3.0	±6.0		±3.0	±6.0		%
Output Voltage Noise[1]	0.1Hz to 10Hz		10	15		10	15	μV_{p-p}
Supply Voltage		7		40	7		40	V
Line Regulation[2]	V_S = +8V to +33V		0.006	0.010		0.006	0.010	%/V
Load Regulation[2]	I_L = 0mA to 10mA		0.005	0.010		0.006	0.010	%/mA
Turn-on Settling Time	To ±0.1% of Final Value		5.0			5.0		μS
Supply Current	No Load		1.0	1.4		1.0	1.4	mA
Load Current		10	21		10	21		mA
Sink Current		-0.3	-0.5		-0.3	-0.5		mA
Short Circuit Current	V_O = 0		30			30		mA
Tempco Voltage Output[6]			630			630		mV

Electrical Characteristics (V_S = +15V and -55°C ≤ T_A ≤ +125°C unless otherwise noted)

Parameters	Test Conditions	REF-02A			REF-02			Units
		Min	Typ	Max	Min	Typ	Max	
Output Voltage Change With Temperature[3,4]	Over Temp. Range		0.06	0.15		0.18	0.45	%
Output Voltage Temperature Coefficient[5]	Over Temp. Range		3.0	8.5		10	25	ppm/°C
Change in V_{OUT} Temperature Coefficient With Output Adjustment	R_P = 10kΩ		0.7			0.7		ppm/%
Line Regulation[2]	V_S = +8V to +33V		0.009	0.015		0.009	0.015	%/V
Load Regulation[2]	I_O = 0mA to 8mA		0.007	0.012		0.007	0.012	%/mA
Tempco Voltage Output Temperature Coefficient[6]			2.1			2.1		mV/°C

Notes:
1. *Guaranteed by design.*
2. Line and load regulation specifications include the effects of self heating.
3. Output voltage change with temperature = $\frac{V_{MAX} - V_{MIN}}{5V}$ x 100%
4. Output voltage change with temperature specification applies untrimmed, or trimmed to +5V.
5. *Output voltage temperature coefficient* = $\frac{\text{Output voltage change with temperature}}{180°C}$
6. Limit current in or out of pin 3 to 50nA and limit capacitance on pin 3 to 30pF.

Electrical Characteristics (V_S = +15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	REF-02C			REF-02D			Units
		Min	Typ	Max	Min	Typ	Max	
Output Voltage	I_L = 0mA	4.950	5.000	5.050	4.900	5.000	5.100	V
Output Adjustment Range	R_P = 10kΩ	±2.7	±6.0		±2.0	±6.0		%
Output Voltage Noise[1]	0.1Hz to 10Hz		12	18		12		μV_{p-p}
Supply Voltage		7.0		30	7.0		30	V
Line Regulation[2]	V_S = +8V to +33V		0.009	0.015		0.012	0.04	%/V
Load Regulation[2]	I_L = 0mA to 8mA I_L = 0mA to 4mA		0.006	0.015		0.009	0.04	%/mA
Turn-on Settling Time	To ±0.1% of Final Value		5.0			5.0		μS
Supply Current	No Load		1.0	1.6		1.0	2.0	mA
Load Current		8.0	21		8.0	21		mA
Sink Current		-0.2	-0.5		-0.2	-0.5		mA
Short Circuit Current	V_O = 0		30			30		mA
Tempco Voltage Output[6]			630			630		mV

Electrical Characteristics (V_S = +15V, 0°C ≤ T_A ≤ +70°C and I_O = 0 unless otherwise noted)

Parameters	Test Conditions	REF-02E			REF-02H			Units
		Min	Typ	Max	Min	Typ	Max	
Output Voltage Change With Temperature[3,4]	Over Temp. Range		0.02	0.06		0.07	0.17	%
Output Voltage Temperature Coefficient[5]	Over Temp. Range		3.0	8.5		10	25	ppm/°C
Change in V_{OUT} Temperature Coefficient With Output Adjustment	R_P = 10kΩ		0.7			0.7		ppm/%
Line Regulation[2]	V_S = +8V to +33V		0.007	0.012		0.007	0.012	%/V
Load Regulation[2]	I_L = 0mA to 8mA		0.006	0.010		0.007	0.012	%/mA
Tempco Voltage Output Temperature Coefficient[6]			2.1			2.1		mV/°C

Notes: 1. Guaranteed by design.
2. Line and load regulation specifications include the effects of self heating.
3. Output voltage change with temperature = $\frac{V_{MAX} - V_{MIN}}{5V} \times 100\%$
4. Output voltage change with temperature specification applies untrimmed, or trimmed to +10V.
5. Output voltage temperature coefficient = $\frac{\text{Output voltage change with temperature}}{70°C}$
6. Limit current in or out of pin 3 to 50nA and limit capacitance on pin 3 to 30pF.

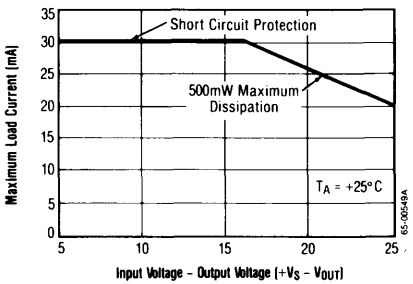
Electrical Characteristics (V_S = +15V, 0°C ≤ T_A ≤ +70°C and I_O = 0 unless otherwise noted)

Parameters	Test Conditions	REF-02C			REF-02D			Units
		Min	Typ	Max	Min	Typ	Max	
Output Voltage Change With Temperature[3,4]	Over Temp. Range		0.14	0.45		0.49	1.7	%
Output Voltage Temperature Coefficient[5]	Over Temp. Range		20	65		70	250	ppm/°C
Change in V_{OUT} Temperature Coefficient With Output Adjustment	R_P = 10kΩ		0.7			0.7		ppm/%
Line Regulation[2]	V_S = +8V to +33V		0.011	0.018		0.020	0.025	%/V
Load Regulation[2]	I_O = 0mA to 5mA		0.008	0.018		0.020	0.025	%/mA
Tempco Voltage Output Temperature Coefficient[6]			2.1			2.1		mV/°C

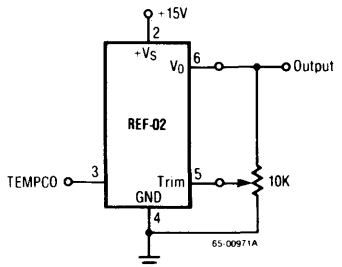
Notes:
1. Guaranteed by design.
2. Line and load regulation specifications include the effects of self heating.
3. Output voltage change with temperature = $\frac{V_{MAX} - V_{MIN}}{5V} \times 100\%$
4. Output voltage change with temperature specification applies untrimmed, or trimmed to +5V.
5. Output voltage temperature coefficient = $\frac{\text{Output voltage change with temperature}}{70°C}$
6. Limit current in or out of pin 3 to 50nA and limit capacitance on pin 3 to 30pF.

Typical Performance Characteristics

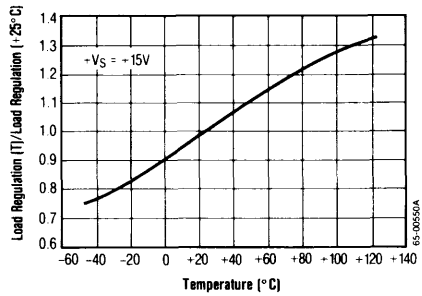
Maximum Load Current vs. Differential Input Voltage



Output Adjustment

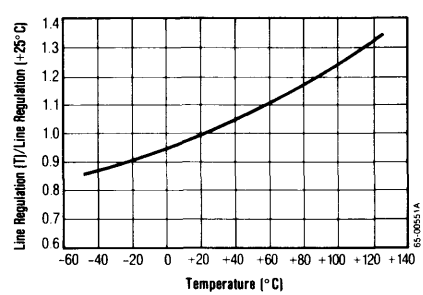


Normalized Load Regulation (ΔIL = 10mA) vs. Temperature

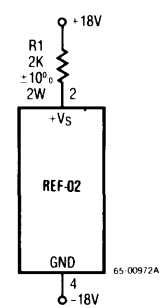


The REF-02 trim terminal can be used to adjust the output voltage over a 5V ±300mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 5V. Of course, the output can also be set to exactly 5.000V or to 5.12V for binary operation. Adjustment of the output does not significantly affect the temperature performance of the device. Typically the temperature coefficient change is 0.7ppm/°C for 100mV of output adjustment.

Normalized Line Regulation vs. Temperature



Burn-In Circuit



Typical Applications

Figure 3 shows how the REF-02 can be connected with an OP-07 to create an electronic thermometer. The circuit uses the +5V reference output and the op amp to level shift and amplify the 2.1mV/°C Tempco output into a voltage signal dependent on the ambient temperature. Different scaling can be obtained by selecting appropriate resistors from the table in Figure 3, giving output slopes calibrated in degrees Celsius or degrees Fahrenheit.

To calibrate, first measure the voltage on the Tempco pin (V_{TEMPCO}) and the ambient room temperature (T_A in °C). Put those values into the following equation:

$$X = \frac{V_{TEMPCO} \text{ (in millivolts)}}{(S)\ (T_A + 273)}$$

Where S = Scale factor for your circuit selected from the table in Figure 3 (in millivolts).

Then turn the circuit power off, short V_{OUT} (pin 6) of the REF-02 to ground, and while applying exactly 100.00mV to the op amp output, adjust R_{B2} so that V_B = (x) (100mV). Now remove the short and the 100mV source, reapply circuit power and adjust R_P so that the op amp output voltage equals (T_A) (S). The system is now exactly calibrated.

For remote sensor applications a 1.5kΩ resistor (R_S) must be connected in series with the Tempco pin to isolate it from cable capacitances. Low temperature coefficient metal film resistors must be used for R_A, R_B and R_C.

Better grades of REF-02 will provide greater accuracy over a wider range of temperatures. To decrease op amp input errors, use an OP-27 instead of an OP-07. A system using a REF-02A and an OP-07C will provide a typical accuracy of ±0.5% over the military temperature range.

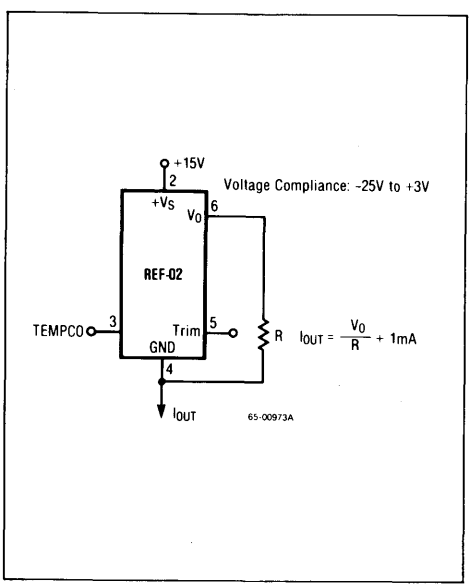


Figure 1. Current Source

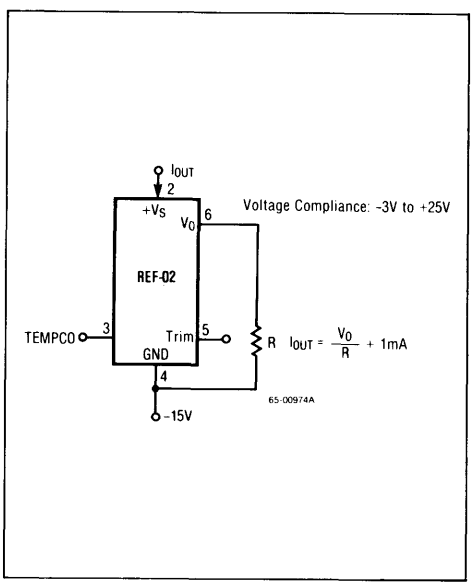
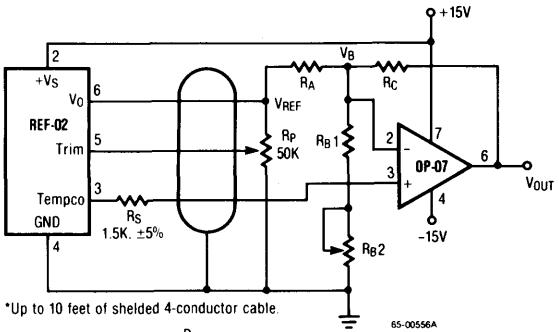


Figure 2. Current Sink



$$T_CV_{OUT} = (2.1mV/°C)\left(1 + \frac{R_C}{R_A \,||\, R_B}\right)$$

$$V_O = \left(H\,\frac{R_C}{R_A \,||\, R_B}\right)V_{Tempco} - \left(\frac{R_C}{R_A}\right)\,(V_O)$$

Resistor Values

TCV_{OUT} Slope(s)	10mV/°C	100mV/°C	10mV/°F
Temperature Range	-55°C to +125°C	-55°C to +125°C	-65°F to +257°F
Output Voltage Range	-0.55V to +1.25V	-5.5V to +12.5V	-0.67V to +2.57V
Zero Scale	0V at 0°C	0V at 0°C	0V at 0°F
R_A (±1% Resistor)	9.09KΩ	15KΩ	8.25KΩ
R_{B1} (±1% Resistor)	1.5KΩ	1.82KΩ	1.0KΩ
R_{B2} (Potentiometer)	200Ω	500Ω	200Ω
R_C (±1% Resistor)	5.11KΩ	84.5KΩ	7.5KΩ

Figure 3. Precision Electronic Thermometer

Raytheon

+2.5V Precision Voltage References

REF-03

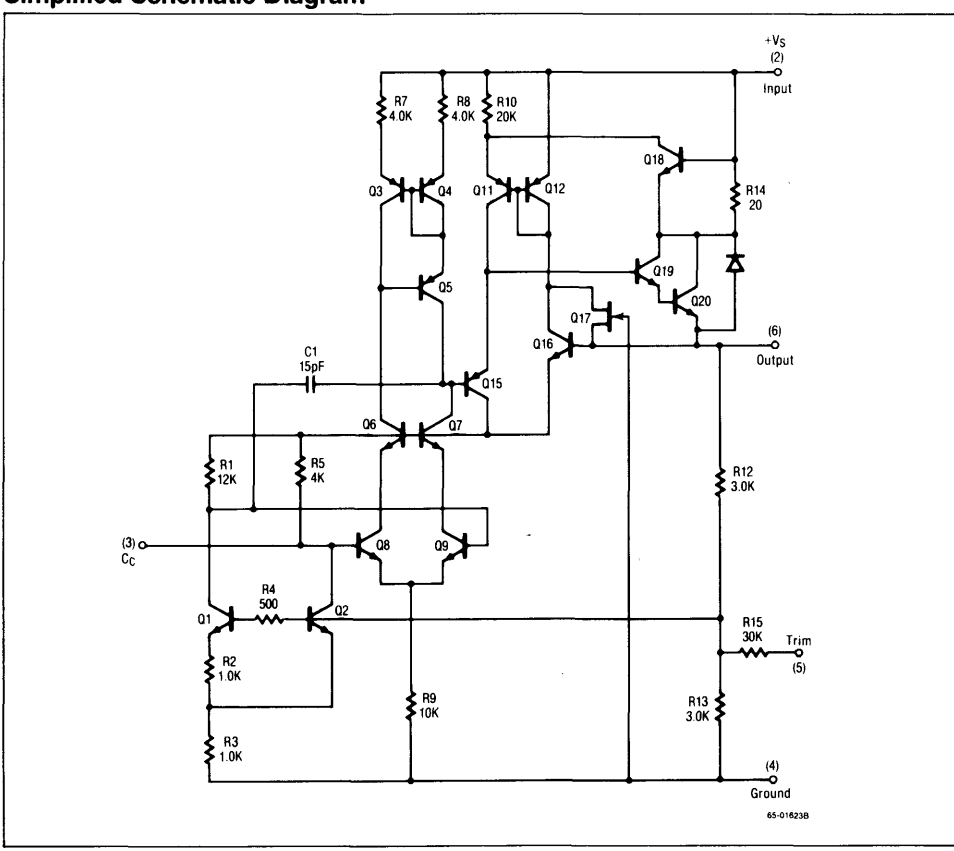
Features

- 2.5 Volt output — ±0.3%
- Adjustable — ±3%
- Excellent temperature stability — 10ppm/°C
- Low noise — 5.0μV_{p-p}
- Wide input voltage range — 4.5V to 30V
- No external components
- Short circuit proof
- Low power consumption — 5mW

Description

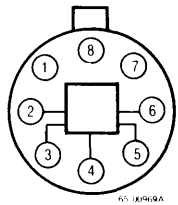
The REF-03 Precision Voltage Reference contains a band-gap reference using thin-film resistors, a step-up amplifier, short circuit protection, and a zener-trim network. The REF-03's 2.5V output shows excellent stability for large changes of temperature, load current, and input voltage. An adjust pin is provided that can change the output voltage by at least 3% with little effect on temperature coefficient.

Simplified Schematic Diagram



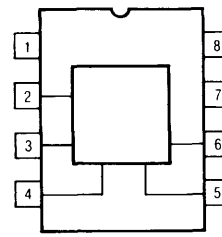
Connection Information

TO-99
Metal Can
(Top View)



65-00969A

8-Lead
Ceramic or Plastic
Dual In-Line Package
(Top View)



65-00970A

Pin	Function
1	No Connection
2	$+V_S$
3	Compensation
4	Ground
5	Adjust
6	V_{OUT}
7	No Connection
8	No Connection

Thermal Characteristics

	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can	8-Lead Plastic DIP
Max. Junction Temp.	175°C	175°C	125°C
Max. P_D $T_A < 50°C$	833mW	658mW	468mW
Therm. Res. θ_{JC}	45°C/W	50°C/W	—
Therm. Res. θ_{JA}	150°C/W	190°C/W	160°C/W
For $T_A > 50°C$ Derate at	8.33mW per °C	5.26mW per °C	6.25mW per °C

Ordering Information

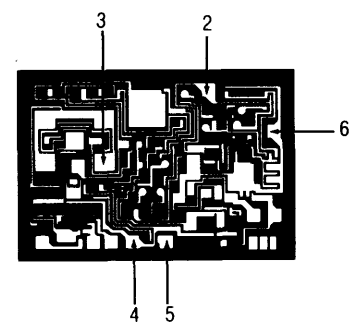
Part Number	Package	Operating Temperature Range
REF-03CT	TO-99	0°C to +70°C
REF-03DT	TO-99	0°C to +70°C
REF-03CNB	Plastic	0°C to +70°C
REF-03DNB	Plastic	0°C to +70°C
REF-03CDE	Ceramic	0°C to +70°C
REF-03DDE	Ceramic	0°C to +70°C
REF-03T	TO-99	-55°C to +125°C
REF-03T/883B*	TO-99	-55°C to +125°C
REF-03DE	Ceramic	-55°C to +125°C
REF-03DE/883B*	Ceramic	-55°C to +125°C

*MIL-STD-883, Level B Processing

Absolute Maximum Ratings

Supply Voltage ..... +30V
Internal Power Dissipation 500mW
Output Short Circuit Duration ..... Indefinite
Storate Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
REF-03 ..... -55°C to +125°C
REF-03C, D ..... 0°C to +70°C
Lead Soldering Temperature
(10 Sec) ..... +300°C

Mask Pattern



Die Size: 78 x 54 mils
Min. Pad Dimensions: 4 x 4 mils

Electrical Characteristics (V_S = +15V, T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	REF-03/REF-03C			REF-03D			Units
		Min	Typ	Max	Min	Typ	Max	
Output Voltage	I_L = 0mA	2.475	2.5	2.525	2.45	2.5	2.55	V
Output Adjust Range	R_P = 10kΩ	±3.0	±6.0		±2.0	±6.0		%
Output Voltage Noise[1]	0.1Hz to 10Hz		5.0	12		5.0		μV_{pp}
Input Voltage Range		4.5		30	4.5		30	V
Line Regulation[2]	V_S = +4.5V to +30V		0.001	0.005		0.001	0.005	%/V
Load Regulation[2]	I_L = 0mA to 8.0mA		0.01	0.02				%/mA
Load Regulation[2]	I_L = 0mA to 4.0mA					0.01	0.04	%/mA
Turn on Settling Time	To 0.1% of Final Value		5.0			5.0		μS
Quiescent Supply Current	I_L =0mA		1.0	1.4		1.0	2.0	mA
Load Current		10	20		5.0	20		mA
Sink Current		-0.2	-0.5		-0.2	-0.5		mA
Short Circuit Current	V_{OUT} = 0V		30			30		mA
The following specifications apply for V_S = +15V, over the specified operating temperature range, unless otherwise noted								
Output Voltage[3,4] Temperature Coefficient	Over Operating Temperature Range		10	25		20	65	ppm/°C
Change in V_{OUT} Temperature Coefficient with Output Adjustment	R_P = 10kΩ		0.7			0.7		ppm/°C
Line Regulation[2]	V_S = +4.5V to +30V		0.002	0.01		0.002	0.1	%/V
Load Regulation[2]	I_L = 0mA to 8.0mA		0.01	0.03				%/mA
Load Regulation[2]	I_L = 0mA to 4.0mA					0.02	0.04	%/mA

Notes: 1. Guaranteed by design.

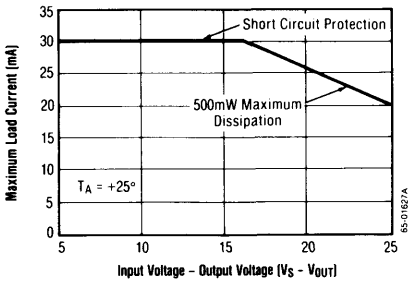
2. Line and load regulation specifications include the effects of self heating.

3. Output voltage temperature coefficient (ppm/°C) = $\frac{V_{max} - V_{min}}{(2.5)\,(T_A max - T_A min)} \times 10^6$

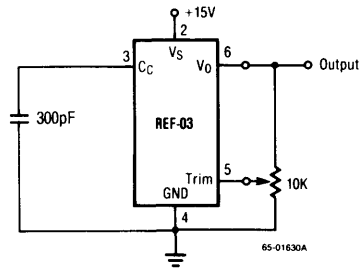
4. Output voltage temperature coefficient specification applies untrimmed or trimmed to +2.5V.

Typical Performance Characteristics

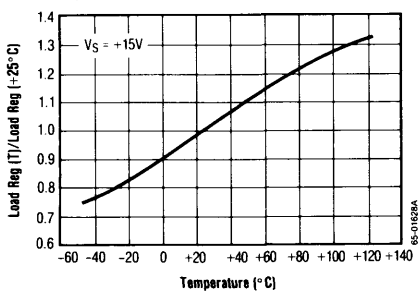
Maximum Load Current vs. Differential Input Voltage



Output Adjustment

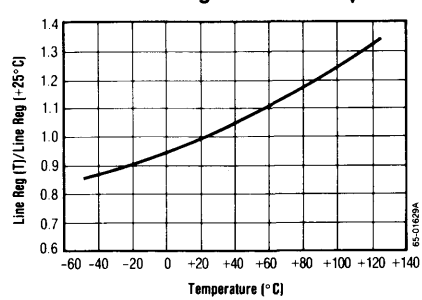


Normalized Load Regulation (ΔIL = 10mA) vs. Temperature

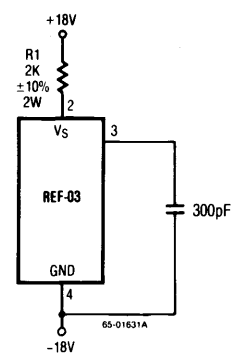


The REF-03 trim terminal can be used to adjust the output voltage over a 2.5V ±150mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 2.5V. Of course, the output can also be set to exactly 2.500V or to 2.56V for binary operation. Adjustment of the output does not significantly affect the temperature performance of the device. Typically the temperature coefficient change is 0.7ppm/°C for 100mV of output adjustment.

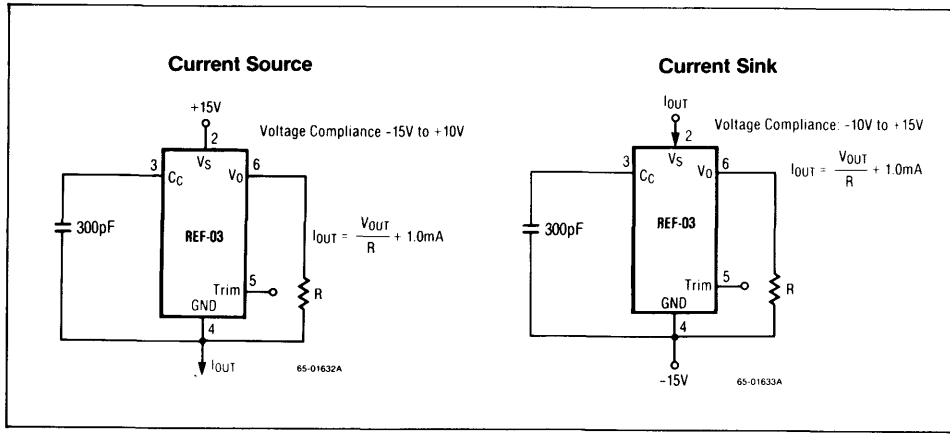
Normalized Line Regulation vs. Temperature



Burn-in Circuit



Typical Applications



Precision Current Source

A precision current source with an output impedance of 300MΩ can be made with two REF-03s, an OP-05, two resistors and two capacitors. The output voltage of U2 and R1 determine the output current (V02/R1). U1 is used to improve the output impedance of I_{OUT} by maintaining a constant 5.0V from V_S to Gnd of U2.

A high quality op amp such as the OP-05, OP-07 or OP-27 should be used as U3 because changes in the voltage at the current source output cause common mode errors in U3 which in turn degrade the output impedance. R1 should equal R2 to eliminate errors due to the I_{OS} of the op amp. C1 and C2 are used as compensation and should equal each other. A time constant of R1C2 = 10^{-5} should be used. With +20V and -15V supplies the output compliance will be ±13V. C3 and C4 are used for frequency compensation and may not be required.

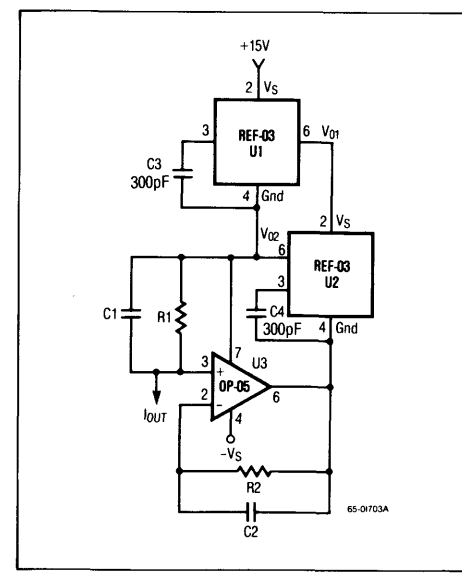


Figure 1. Precision Current Source

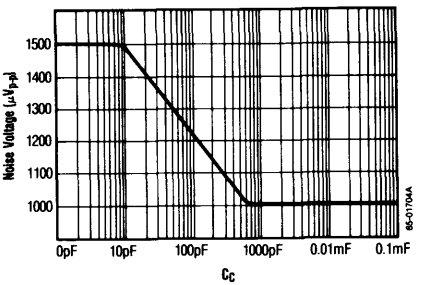


Figure 2. 0.1Hz ~ 1MHz Noise μV Peak-to-Peak Over 4 Second Scan

Section 11
Voltage Regulators

Raytheon's regulator products complement the products shown in other sections of this handbook. Positive and negative dual tracking regulators (RC4194 and RC4195) simplify power supplies for op amp circuits; their small size allows "on card" regulation adjacent to end use circuits. The RC4193 and RC4391 also will provide this positive and negative tracking supply on card, with the additional benefits of needing only a single unregulated input and being efficient enough to complement Raytheon's low power op amps and comparators in micropower circuits.

The main voltage regulator groups are as follows:

Linear Regulators —
- RC4194 Adjustable Dual Regulator
- RC4195 Fixed ±15V Dual Regulator

Micropower Switching Regulators —
- RC4193 Positive Input/Positive Output
- RC4391 Positive Input/Negative Output

DEFINITIONS

Efficiency
The ratio of load power to supply power, measured in percent.

$$\text{Efficiency} = \frac{(V_O)\,(I_O)}{(V_S)\,(I_S)} \times 100\%$$

Where V_O is the output voltage, I_O is the load current.

Input Output Voltage Differential
Guaranteed voltage difference needed to maintain output voltage specifications (dropout voltage) at a specified load current, measured in volts (V).

Internal Thermal Shutdown
The average junction temperature required to activate the thermal shutdown circuitry for disabling the output, measured in degrees C (°C).

Line Regulation
The ratio of change in output voltage to the change in supply (line) voltage effecting it, expressed as a percentage of the output voltage for a specified change in supply voltage.

Load Regulation
The ratio of change in output voltage to the change in load (output) current effecting it, measured in percent of output voltage per milliamp change in load current.

Operating Frequency Range
Guaranteed minimum range of achievable oscillation frequencies. Operating frequency range is expressed as a minimum and maximum value in Hertz (Hz).

Output Voltage Noise
The broadband noise over a specified range of frequencies, measured in microvolts peak-to-peak or rms (μV_{p-p} or V_{RMS}).

Output Voltage Tracking
The difference in absolute value of the two output voltages of a dual regulator, expressed as a percentage of the nominal output voltage.

Ripple Rejection
Similar to line regulation but specified at a particular frequency of supply voltage change, expressed in decibels (dB).

Short Circuit Current
The maximum output current available from the regulator with the output shorted to ground, expressed in milliamps (mA).

Supply Current (I_S)
The current required from the power supply to operate the regulator under quiescent no-load conditions, expressed in milliamps (mA).

Supply Voltage (V_S)
The range of power supply voltages over which the regulator will operate, expressed in volts (V).

Switch Current
The current flowing through the switch transistor, guaranteed at some minimum value with a specified collector to emitter voltage, expressed in milliamps (mA).

Switch Leakage Current
The collector to emitter leakage current of the internal switch transistor with the switch in an off condition. Switch leakage current is measured with a specified stress voltage and is expressed in microamps (μA).

Timing Pin Current
The charging current used to create a timing waveform at the C_X oscillator pin. The value of this current and the value of C_X determine the operating frequency. Timing pin current is measured in microamps (μA).

Raytheon

Micro-Power Switching Regulators

4191/2/3

Features

- High efficiency — 80% typical
- Low quiescent current — 135μA
- Adjustable output — 2.5V to 30V
- High switch current — 150mA
- Bandgap reference — 1.31V
- Remote shutdown capability
- Low battery detection circuitry
- Low component count

Description

Raytheon's micro-power switching regulators, 4191, 92 and 93, are the industry's first monolithic low power switching regulators available in an 8-lead mini-DIP, and designed specifically for battery operated instruments. They each contain a 1.3V temperature compensated bandgap reference, adjustable free running oscillator, voltage comparator, low battery detection circuitry, and a 150mA switch transistor with all of the functions required to make a complete low power switching regulator.

These regulators can achieve up to 80% efficiency in most applications while being able to operate over a wide input supply voltage range, 2.4V to 30V, at a very low quiescent drain of 135μA.

The 4191/92/93s have a free running oscillator which provides the drive signal for the on-chip 150mA switch transistor. The 100Hz to 75kHz oscillator frequency is determined by an external capacitor on pin 2.

These universal regulators can be used as a building block in three basic applications: step-up, step-down, and inverting.

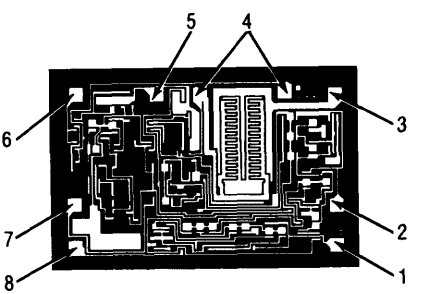
In their most popular configuration, step-up, these regulators will reduce the number of battery cells required for a given output voltage, and will maintain that voltage as the batteries decay, thus making available more board space and lengthening battery life.

A practical example of these advantages would be an instrument designed to operate from a nominal 9V supply voltage. If this instrument were powered with just 7 components (a steering diode, an inductor, two resistors, a capacitor, a 4191, 92 or 93 and a 9V battery), it would receive a continuous 9V until the battery had decayed to a terminal voltage of 2.4V. If board space is at a premium, then the designer could remove the 9V source and replace it with a single 3V Ni-Cad battery without making any other adjustment(s) to the circuitry or affecting the overall operation of the instrument.

The 4191/92/93 series of micro-power switching regulators consists of three devices each with slightly different specifications. The 4191 has a 1.5% maximum output voltage tolerance, 0.2% maximum line regulation, and operation to 30V. The 4192 has a 3.0% maximum output voltage tolerance, 0.5% maximum line regulation, and operation to 30V. The 4193 has a 5.0% maximum output voltage tolerance, 0.5% maximum line regulation, and operation to 24V. Other specifications are identical for the 4191, 4192 and 4193. Each type is available in commercial, industrial, and military temperature ranges, and in plastic and ceramic DIPs.

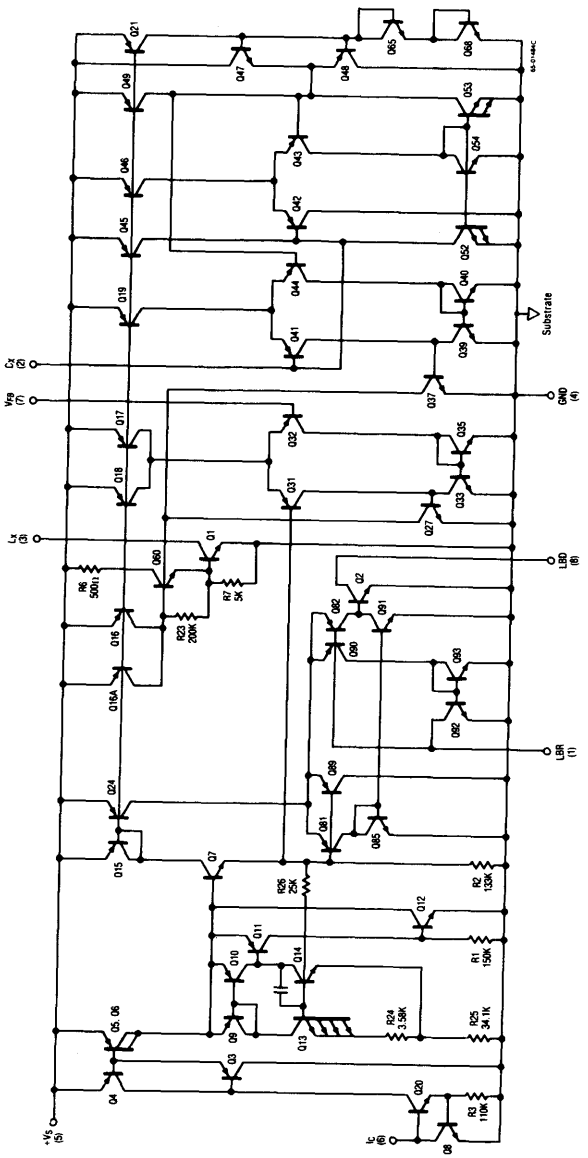
With some optional external components the application can be designed to signal a display when the battery has decayed below a predetermined level, or designed to signal a display at one level and then shut itself off after the battery decays to a second level. See the applications section for these and other unique circuits.

Mask Pattern



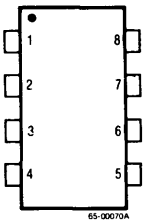
Die Size: 83 x 54 mils 65-01482A
Min. Pad Dimensions: 4 x 4 mils

Schematic Diagram



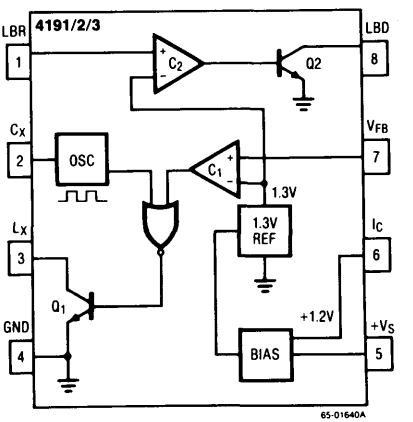
Connection Information

8-Lead
Dual In-Line Package
(Top View)



Pin	Function
1	Low Battery (Set) Resistor (LBR)
2	Timing Capacitor (C_X)
3	External Inductor (L_X)
4	Ground
5	+Supply Voltage ($+V_S$)
6	Reference Set Current (I_C)
7	Feedback Voltage (V_{FB})
8	Low Battery Detector Output (LBD)

Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage (Without External Series Pass Transistor)
- 4191, 4192 ..... +30V
- 4193 ..... +24V

Storage Temperature Range ..... -65° to +150°C

Operating Temperature Range
- RM4191/2/3 ..... -55°C to +125°C
- RV4191/2/3 ..... -40°C to +85°C
- RC4191/2/3 ..... 0°C to +70°C

Switch Current ..... 375mA Peak

Thermal Characteristics

	8-Lead Plastic DIP	8-Lead Ceramic DIP
Max. Junction Temp.	125°C	175°C
Max. P_D T_A < 50°C	468mW	833mW
Therm. Res. θ_{JC}	—	45°C/W
Therm. Res. θ_{JA}	160°C/W	150°C/W
For T_A > 50°C Derate at	6.25mW per °C	8.33mW per °C

Ordering Information

Part Number	Package	Operating Temperature Range
RC4191NB	Plastic	0°C to +70°C
RC4192NB	Plastic	0°C to +70°C
RC4193NB	Plastic	0°C to +70°C
RC4191DE	Ceramic	0°C to +70°C
RC4192DE	Ceramic	0°C to +70°C
RC4193DE	Ceramic	0°C to +70°C
RV4191NB	Plastic	-40°C to +85°C
RV4192NB	Plastic	-40°C to +85°C
RV4193NB	Plastic	-40°C to +85°C
RV4191DE	Ceramic	-40°C to +85°C
RV4192DE	Ceramic	-40°C to +85°C
RV4193DE	Ceramic	-40°C to +85°C
RM4191DE	Ceramic	-55°C to +125°C
RM4192DE	Ceramic	-55°C to +125°C
RM4193DE	Ceramic	-55°C to +125°C
RM4191DE/883B*	Ceramic	-55°C to +125°C
RM4192DE/883B*	Ceramic	-55°C to +125°C
RM4193DE/883B*	Ceramic	-55°C to +125°C

*MIL-STD-883, Level B Processing

Electrical Characteristics (V_S = +6.0V, I_C = 5.0μA, and T_A = +25°C unless otherwise noted)

Parameters	Symbol	Conditions	4191			4192			4193			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supply Voltage	$+V_S$		2.4		30	2.4		30	2.4		24	V
Reference Voltage (Internal)	V_{REF}		1.29	1.31	1.33	1.27	1.31	1.35	1.24	1.31	1.38	V
Switch Current	I_{SW}	V_3 = 400mV	75	150		75	150		75	150		mA
Supply Current	I_S	Measure at Pin 5 I_3 = 0		135	200		135	200		135	200	μA
Efficiency	ef			80			80			80		%
Line Regulation		$0.5V_O < V_S < V_O$		0.08	0.2		0.08	0.5		0.08	0.5	% V_O
Load Regulation	L_I	V_S = +0.5V_O, P_L = 150mW		0.2	0.5		0.2	0.5		0.2	0.5	% V_O
Operating Frequency Range	F_O		0.1	25	75	0.1	25	75	0.1	25	75	kHz
Reference Set Current	I_C		1.0	5.0	50	1.0	5.0	50	1.0	5.0	50	μA
Switch Current	V_3	V_3 = 1.0V	100			100			100			mA
Switch Leakage Current	I_{CO}	V_3 = 24V		0.01	5.0		0.01	5.0		0.01	5.0	μA
Supply Current (Disabled)	I_{SO}	I_C < 0.01μA		0.1	5.0		0.1	5.0		0.1	5.0	μA
Low Battery Bias Current	I_1	V_1 = 1.2V		0.7			0.7			0.7		μA
Capacitor Charging Current	I_{CX}			5.0			5.0			5.0		μA
Capacitor Threshold Voltage +	$+V_{THX}$			1.78			1.78			1.78		V
Capacitor Threshold Voltage –	$-V_{THX}$			0.62			0.62			0.62		V
Feedback Input Current	I_{FB}	V_7 = 1.3V		0.1			0.1			0.1		μA
Low Battery Output Current	I_{LBD}	V_8 = 0.4V, V_1 = 1.1V	250	600		250	600		250	600		μA

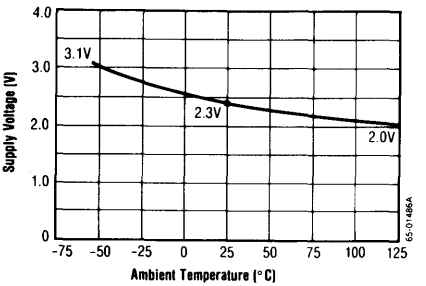
Electrical Characteristics

(V_S = +6.0V, I_C = 5.0μA, unless otherwise noted, over the full operating temperature range)

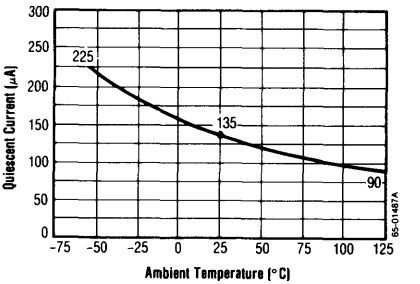
Parameters	Symbol	Conditions	4191			4192			4193			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supply Voltage	$+V_S$		3.5		24	3.5		24	3.5		24	V
Reference Voltage (Internal)	V_{REF}		1.25	1.31	1.37	1.23	1.31	1.39	1.20	1.31	1.42	V
Quiescent Current	I_S	Measure at Pin 5 $I_3 = 0$		225	300		225	300		225	300	μA
Line Regulation		$0.5V_O < +V_S < V_O$		0.2	0.5		0.5	1.0		0.5	1.0	% V_O
Load Regulation	L_I	$+V_S = 0.5V_O$, P_L = 150mW		0.5	1.0		0.5	1.0		0.5	1.0	% V_O
Reference Set Current	I_C		1.0	5.0	50	1.0	5.0	50	1.0	5.0	50	μA
Switch Leakage Current	I_{CO}	V_3 = 24V			30			30			30	μA
Supply Current (Disabled)	I_{SO}	$I_C < 0.01\mu A$			30			30			30	μA
Low Battery Output Current	I_{LBD}	V_8 = 0.4V, V_1 = 1.1V	250	600		250	600		250	600		μA

Typical Performance Characteristics

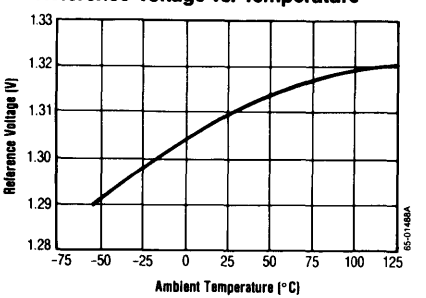
Minimum Supply Voltage vs. Temperature



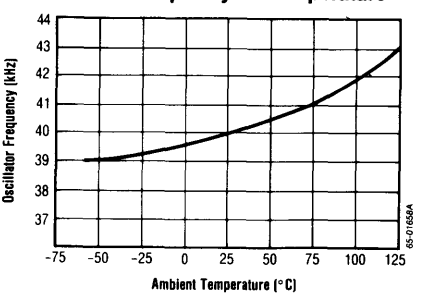
Quiescent Current vs. Temperature



Reference Voltage vs. Temperature



Oscillator Frequency vs. Temperature



Principles of Operation

Simple Step-Up Converter

The most common application, the step-up regulator, is derived from a simple step-up DC-to-DC converter (Figure 1).

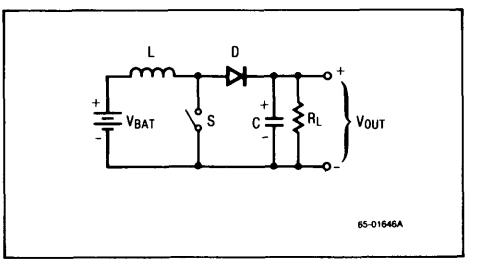


Figure 1. Simple Step-Up DC-to-DC Converter ($V_{OUT} > V_{BAT}$)

When switch S is closed the battery voltage is applied across the inductor L. Charging current flows through the inductor, building up a magnetic field, increasing as the switch is held closed. While the switch is closed, the diode D is reverse biased (open circuit) and current is supplied to the load by the capacitor C. Until the switch is opened the inductor current will increase linearly to a maximum value determined by the battery voltage, inductor value, and the amount of time the switch is held closed ($I_{PEAK} = V_{BAT}/L \times T_{ON}$). When the switch is opened, the magnetic field collapses, and the energy stored in the magnetic field is converted into a discharge current which flows through the inductor in the same direction as the charging current. Because there is no path for current to flow through the switch, the current must flow through the diode to supply the load and charge the output capacitor.

If the switch is opened and closed repeatedly, at a rate much greater than the time constant of the output RC, then a constant DC voltage will be produced at the output.

An output voltage higher than the input voltage is possible because of the high voltage produced by a rapid change of current in the inductor. When the switch is opened the inductor voltage will instantly rise high enough to forward bias the diode, to $V_{OUT} + V_D$.

In the complete 4193 regulator a feedback control system adjusts the on time of the switch, controlling the level of inductor current, so that the average inductor current equals the load current, thus regulating the output voltage.

Complete Step-Up Regulator

A complete schematic of the minimum step-up application is shown in Figure 2. The ideal switch in the DC-to-DC converter diagram is replaced by an open collector NPN transistor Q1. C1 functions as the output filter capacitor, and D1 and L_X replace D and L.

When power is first applied, the current in R1 supplies bias current to pin 6 (I_C). This current is stabilized by a unity gain current source amplifier and then used as bias current for the 1.31V bandgap reference. A very stable bias current generated by the bandgap is mirrored and used to bias the remainder of the chip. At the same time the 4193 is starting up, current will flow through the inductor and the diode to charge the output capacitor to $V_{BAT} - V_D$.

At this point the feedback (pin 7) senses that the output voltage is too low, by comparing a division of the output voltage (set by the ratio of R2 to R3) to the +1.31V reference. If the output voltage is too low then the comparator output changes to a logical zero. The NOR gate then effectively ANDs the oscillator square wave with the comparator signal; if the comparator output is zero AND the oscillator output is low, then the NOR gate output is high and the switch transistor will be forced on. When the oscillator goes high again the NOR gate output goes low and the switch transistor will turn off. This turning on and off of the switch transistor performs the same function that opening and closing the switch in the simple DC-to-DC converter does; i.e., it stores energy in the inductor during the on time and releases it into the capacitor during the off time.

The comparator will continue to allow the oscillator to turn the switch on and off until enough charge has been delivered to the capacitor to raise the feedback voltage above 1.31V.

Thereafter this feedback system will vary the duration of the on time in response to changes in

load current or battery voltage (see Figure 3). If the load current increases (waveform C), then the transistor will remain on (waveform D) for a longer portion of the oscillator cycle, thus allowing the inductor current (waveform E) to build up to a higher peak value. The duty cycle of the switch transistor varies in response to changes in load and line.

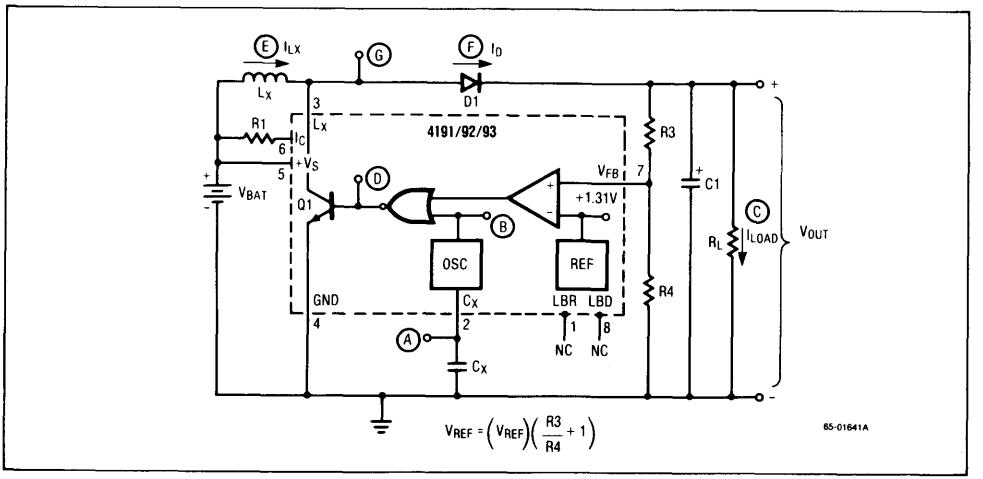


Figure 2. Minimum Step-Up Application

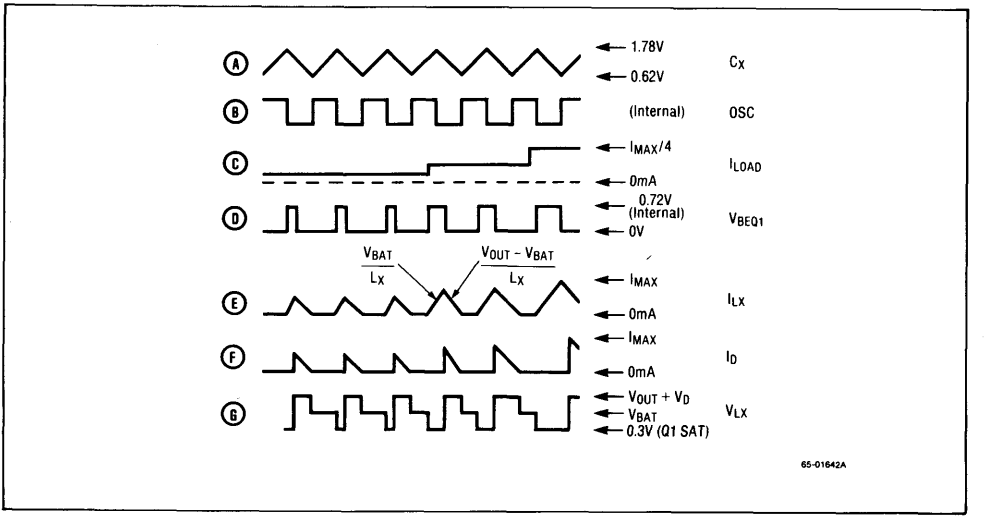


Figure 3. Step-Up Regulator Waveforms

The inductor value and oscillator frequency must be carefully tailored to the battery voltage, output current, and ripple requirements of the application (see Design Equations, Figure 11). If the inductor value is too high or the oscillator frequency is too high then the inductor current will never reach a value high enough to meet the load current and the output voltage will collapse. If the inductor value is too low or the oscillator frequency too low then the inductor current will build up too high, causing excessive output voltage ripple or possibly over stressing the switch transistor.

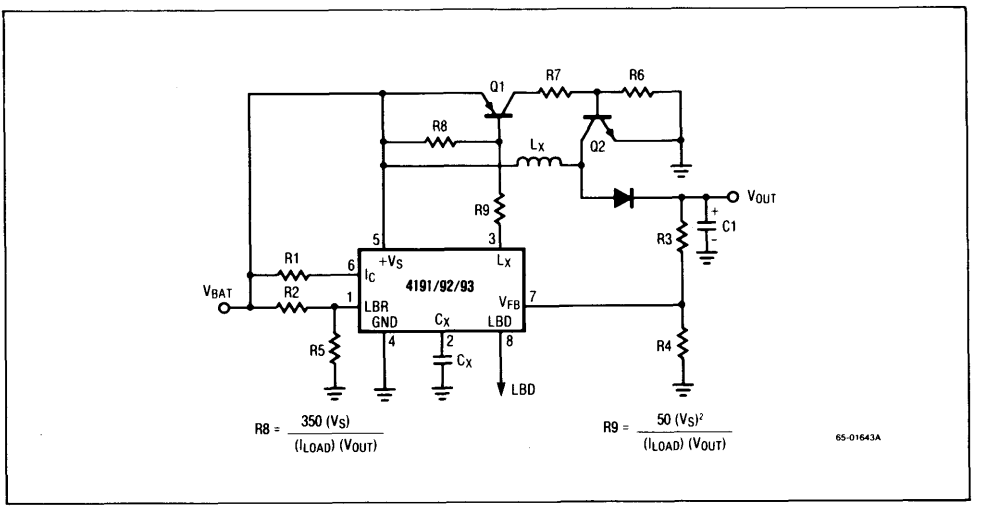


Figure 4. Step-Up Switching Regulator (High Current)

Simple Step-Down Converter

Figure 5 shows a simple step-down DC-to-DC converter with no feedback or control.

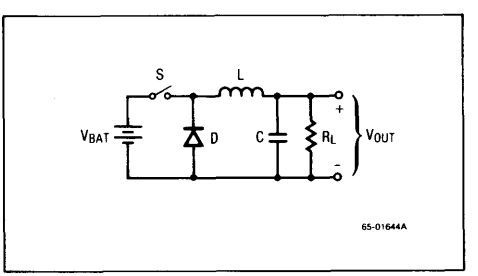


Figure 5. Simple Step-Down DC-to-DC Converter ($V_O \leq V_{BAT}$)

When S is closed the battery voltage minus the output voltage is applied across the inductor. All of the inductor current will flow into the load until the inductor current exceeds the load current. The excess current will then charge the capacitor and the output voltage will rise. When S is opened the voltage applied across the inductor will be reduced to V_{OUT} plus V_{DIODE}, and the inductor will discharge into the load. As in the step-up case, the average inductor current equals the load current. The maximum inductor current I_{MAX} will equal $(V_{BAT} - V_{OUT})/L_X$ times the maximum on time of the switch transistor. The maximum load current can be as high as $I_{MAX}/2$. At load currents less than $I_{MAX}/2$ the 4193 will reduce the switch on time until the average inductor current equals the load current.

Complete Step-Down Regulator

Since the switch transistor in the 4193 is in parallel with the load a method must be used to convert it to a series connection. The circuit of Figure 6 accomplishes this. The 2N2907 replaces S of Figure 5, and R6 and R7 are added to provide the base drive to the 2N2907 in the correct polarity to operate the circuit properly (refer to Figure 11 for determining the circuit values). Since the L_X pin is capable of sinking 150mA, high current switching transistors can be used in place of the 2N2907.

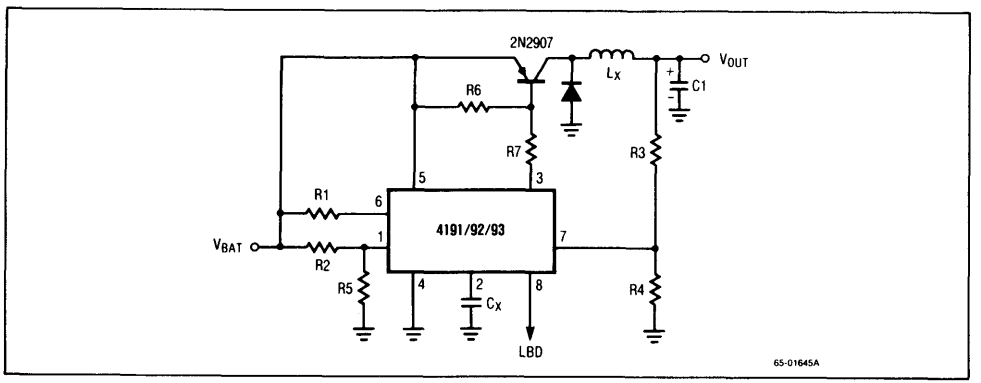


Figure 6. Complete Step-Down Regulator

An alternate method for providing base drive to the 2N2907 is to use the 4193 I_S current which alternates between 150μA and 2.5mA as the internal transistor (Q1 of Figure 2) turns off and on. This technique saves about 1.0mA of wasted current by connecting the base of the 2N2907 to the V_S pin as shown in Figure 7. The only requirement for this circuit is that the value of R6 must be low enough to insure turn off of the 2N2907. A value of 2.0kΩ is sufficient.

This technique is useful only for low load power applications, less than about 150mW.

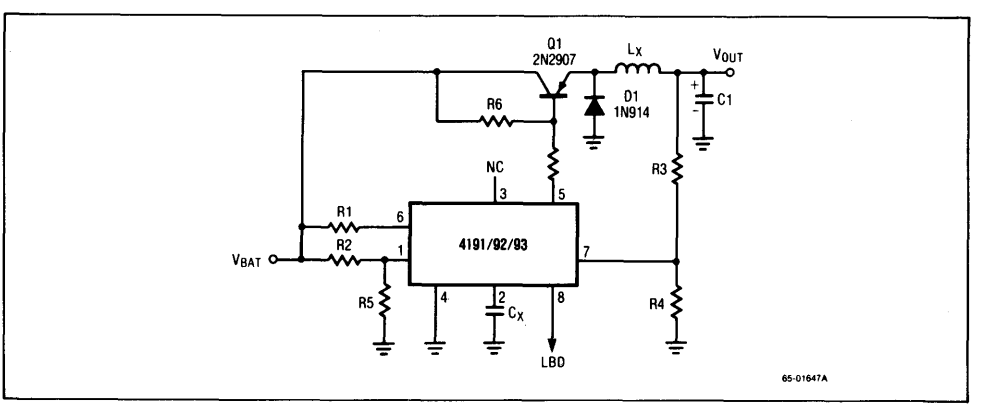


Figure 7. Step-Down Current Saver

Greater Than 30V Application

Adding a zener diode in series with the base of the 2N2907 allows the battery voltage to increase by the value of the zener, with only a slight decrease in efficiency. As an example, if a 24V zener is used, the maximum battery voltage can go to 48V when using a 4193. Refer to Figures 8 and 9.

Note, however, that the addition of the zener diode will not alter the maximum change of supply. With a 24V zener the circuit will stop operating when the battery voltage drops below 24V +2.4V = 26.4V.

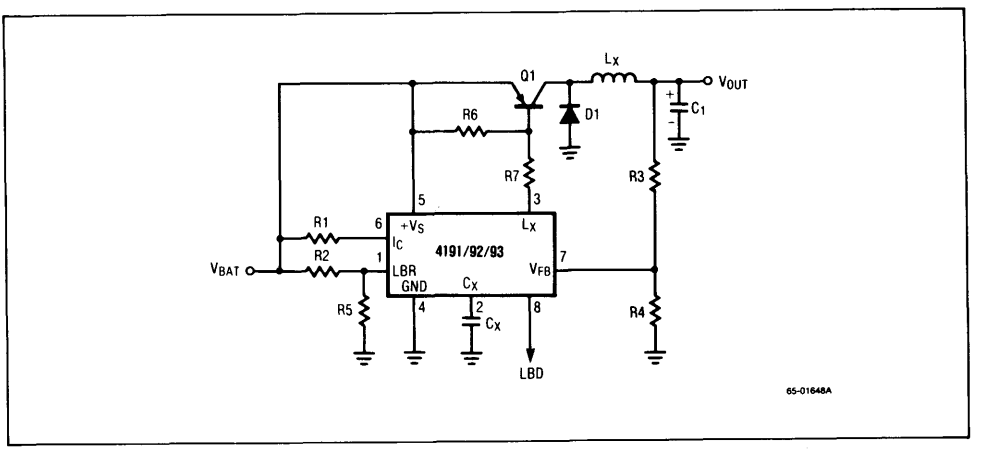


Figure 8. Stepping Down an Input Voltage Greater Than 30V

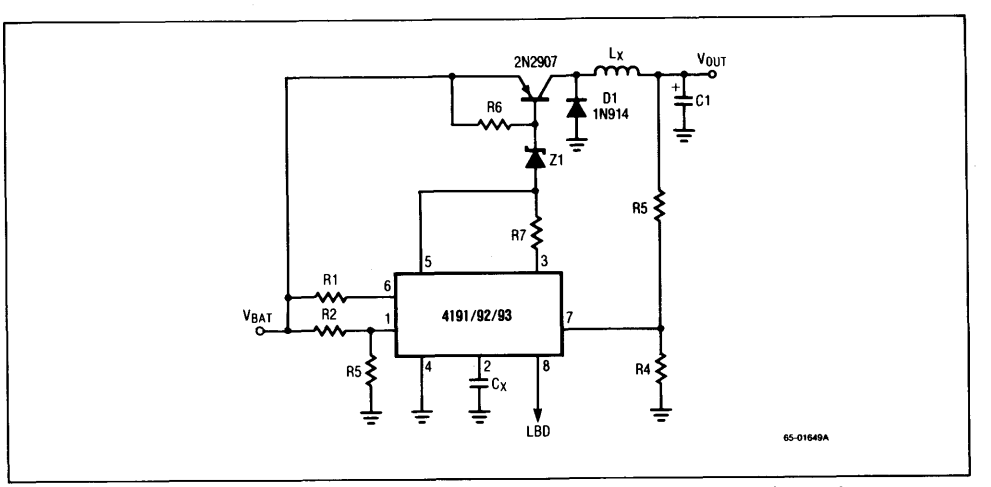


Figure 9. Stepping Down an Input Voltage Greater Than 30V (High Current)

Inverting Switching Regulator

Many single supply systems require an occasional negative voltage for a specific application. This circuit will meet those needs.

The circuit is similiar to the type used in Figure 6, except the location of L_X and the diode are reversed and a micro-power op amp RC3078 is added to provide inversion for the sense voltage. The output voltage is given by 1.31(R3)/R4.

The RC3078 operates at a closed loop gain of close to one in most applications. Therefore the value of C_C must be such to frequency compensate the RC3078 for unity gain conditions. The value for R_{SET} will determine the quiescent current in the 3078 and for micropower applications can be set to operate at approximately 10μA. Where a larger amount of amplifier quiescent current can be tolerated, a ground sensing op amp such as the LM324 or RC3403A can be used, eliminating the need for R_{SET} and C_C.

An important point is that pin 7 must be below 1.3V when $|V_{OUT}|$ is below the design output voltage or else the circuit will not start.

Due to their output stage design, op amp types similar in design to the 741 may cause the circuit to not start properly since they fail to keep pin 7 below 1.3V when power is first applied.

Note: Most inverting applications can be realized with less complexity and lower cost by using the RC4391 regulator, which is a dedicated inverting regulator I.C. Use of the 4391 will eliminate the extra op amp and external transistor (see Figure 23 for a 4391 application).

Design Equations

Figure 11 is a set of design equations which can be used to determine resistor, capacitor and inductor values for step-down, step-up, and voltage inverting applications. To use the equations, first determine the oscillator frequency (F_O), input voltage (V_{BAT}), output voltage (V_{OUT}), and maximum output load current (I_L), according to the application requirements. Then plug those numbers into the appropriate equations. These equations are based on an I_{MAX} of 150mA, so output voltage ripple may not be optimized. If ripple becomes a problem then increase F_O.

As an alternative to using the design equations, the following process can be used to optimize circuit performance.

1. Select an operating frequency based on efficiency and capacitor size requirements (frequencies from 10kHz to 50kHz are typical).
2. Build the circuit and apply the worst case conditions to it, i.e., the lowest battery voltage and the highest load current at the desired output voltage.

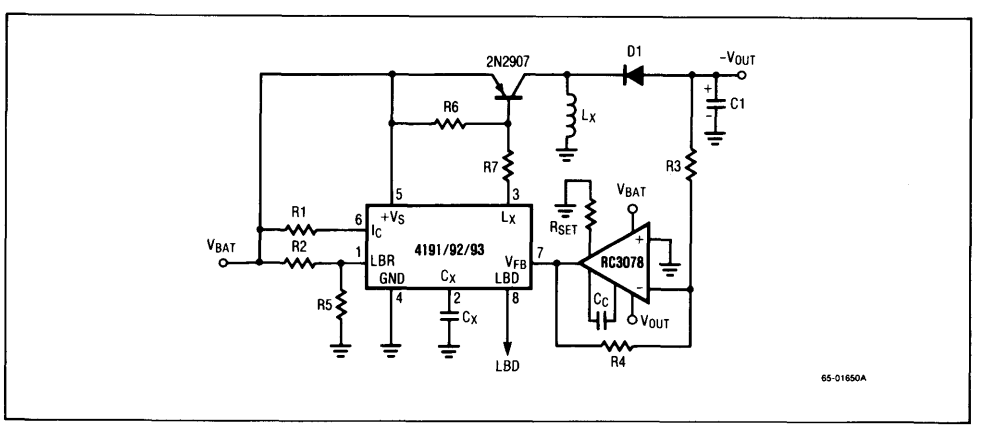


Figure 10. Inverting Switching Regulator Using 4191/92/93

Component	Step Up	Step Down	Inverting
R_1	$\frac{V_S - 1.2V}{5\mu A}$	$\frac{V_S - 1.2V}{5\mu A}$	$\frac{V_S - 1.2V}{5\mu A}$
R_2*	$\frac{V_S - 1.31V}{5\mu A}$	$\frac{V_S - 1.31V}{5\mu A}$	$\frac{V_S - 1.31V}{5\mu A}$
R_3**	$\frac{V_{OUT} - 1.31V}{I_A}$	$\frac{V_{OUT} - 1.31V}{I_A}$	$\frac{V_{OUT}}{I_A}$
R_4**	$\frac{1.31V}{I_A}$	$\frac{1.31V}{I_A}$	$\frac{1.31V}{I_A}$
R_5*	261kΩ	261kΩ	261kΩ
C_X(pF)	$\frac{2.14 \times 10^6}{F_O(Hz)}$	$\frac{2.14 \times 10^6}{F_O(Hz)}$	$\frac{2.14 \times 10^6}{F_O(Hz)}$
L_X	$\frac{0.3(V_S)(V_{OUT} - V_S)}{F_O(I_{LOAD})(V_{OUT})}$	$\frac{0.3(V_{OUT})}{F_O(I_{LOAD})}$	$\frac{0.3(V_S)(\lvert V_{OUT}\rvert)}{F_O(I_{LOAD})(V_S + \lvert V_{OUT}\rvert)}$
C_1	$\frac{2V_{OUT} - V_S}{4F_O(V_{OUT})V_{RIPPLE}}$**	$\frac{I_{LOAD}}{4F_O(V_{RIPPLE})}$	$\frac{0.15I_{LOAD}(V_S + 2\lvert V_{OUT}\rvert)^2}{F_O(V_S)(V_S + \lvert V_{OUT}\rvert)V_{RIPPLE}}$
R_6	$\frac{35\,V_S}{(I_{LOAD})(V_{OUT})}$	$\frac{35}{I_{LOAD}}$	$\frac{35(V_S)}{(I_{LOAD})(V_S + \lvert V_{OUT}\rvert)}$
R_7	$\frac{5(V_S)^2}{(I_{LOAD})(V_{OUT})}$	$\frac{5V_S}{I_{LOAD}}$	$\frac{5(V_S)^2}{(I_{LOAD})(V_S + \lvert V_{OUT}\rvert)}$

* = Optional ** Recommended I_A be set between 50μA and 100μA

Figure 11. 4191/92/93 Design Equations

3. Adjust the inductor value down until the desired output voltage is achieved, then go a little lower (approximately 15%) to cover manufacturing tolerances.
4. Check the output voltage with an oscilloscope for ripple, at high battery voltages, at as high of voltages as are expected. Also check for efficiency by monitoring battery and output voltages and currents (eff=$(V_{OUT})(I_{OUT})/(V_{BAT})(I_{IN})$ x 100%).
5. If the efficiency is poor, go back to (1) and start over. If the ripple is excessive, then increase the output filter capacitor value or start over.

Timing

The oscillator creates a square wave using a method similar to the 555 timer I.C., with a current steering flip-flop controlled by two voltage sensing comparators. The capacitor C_X is charged by a current source until its voltage reaches the 1.78V threshold (see Figure 3). The first comparator then sets the flip-flop and a negative current source discharges C_X. The second comparator trips at 0.62V, resetting the flip-flop, and the voltage ramps up again, starting another cycle. The output transistor cannot turn on unless the C_X voltage is ramping down.

The turn off delay of Q1 must be taken into account when operating at frequencies greater than 50kHz (Figure 2). The 4191/92/93 was designed for maximum efficiency at low input voltages commonly found in battery applications. Q1 was designed to saturate in order for the inductor to charge to the full input voltage. As a result, Q1 has a fixed 5.0μS turn off delay, which has the effect of increasing the On/Off duty cycle as the oscillator frequency is increased.

Another consideration is the frequency response of the feedback network. The output RC introduces a lag into the feedback signal which may cause excessive output ripple or erratic switching. If this problem occurs it can be cured by connecting a 100pF to 1000pF capacitor in parallel with the feedback resistor (R3 in Figure 2).

Inductors

Efficiency and load regulation will improve if a quality high Q inductor is used. A ferrite pot core is recommended; the wind-yourself type with an air gap adjustable by washers or spacers is very useful for bread boarding prototypes. Care must be taken to choose a permeable enough core to handle the magnetic flux produced at I_{MAX}; if the core saturates then efficiency and output current capability are severely degraded and excessive current will flow through the switch transistor. An isolated AC current probe for an oscilloscope is an excellent tool for saturation problems; with it the inductor current can be monitored for nonlinearity at the peaks (a sign of saturation).

Low Battery Detector

An open collector signal transistor Q2 with comparator C2 provide the designer with a method of signaling a display or computer whenever the battery voltage falls below a programmed level. This level is determined by the +1.31V reference level and by the selection of two external resistors according to the equation:

$$V_{TH} = V_{REF}\left(\frac{R2}{R5} + 1\right)$$

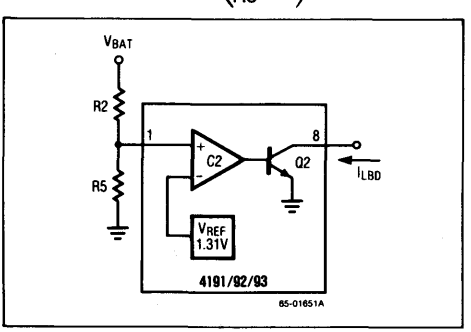


Figure 12. Low Battery Detector

When the battery voltage drops below this threshold Q2 will turn on and sink over 600μA typically. The low battery detector circuitry may also be used for other, less conventional applications (see Figures 18 and 19).

Bias Current Shutdown

The control current for the reference is externally set by a resistor from the I_C pin to the battery. This current can vary from 1.0μA to 50 μA without affecting the operation of the I.C. Interrupting this current will disable the entire circuit, causing the output voltage to go to zero volts for step down applications, and reducing the supply current to less than 1.0μA.

Automatic shutdown of the 4193 can be achieved using the circuit of Figure 13.

A resistor is placed from the I_C pin to ground, creating a voltage divider. When the voltage at the I_C pin is less than 1.2V, the 4193 will turn off. This scheme should only be used in limited temperature range applications since the "turn off" voltage at the I_C pin has a temperature coefficient of -4.0mV/°C. At 25°C, typically 250nA is the minimum current required by the I_C pin to sustain operation. A 5.0μA voltage divider works well taking into account the sustaining current of 250nA and a threshold voltage of 0.4V at turn off. As an example, if 3.0V is to be the turn off voltage, then R9 = 1.1/4.75μA and R1 = (3.0 - 1.1)5.0μA or about 240kΩ and 390kΩ respectively. The tempco at the top of the divider will be -4.0mV (R1 + R9)/R9 or -10.5mV/°C an acceptable number for many applications.

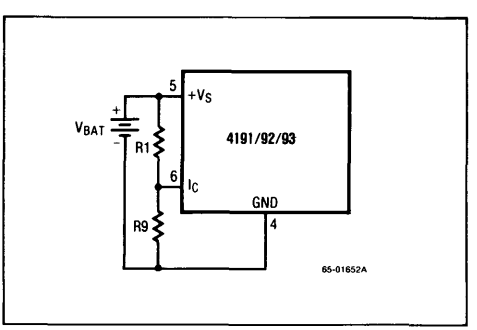


Figure 13. Simple Automatic Shutdown

Another method of automatic shutdown without temperature limitations is the use of a zener diode in series with the I_C pin and set resistor. When the battery voltage falls below $V_Z + 1.2V$ the circuit will start to shut down. With this connection and the low battery detector, the application can be designed to signal a display when the battery voltage has dropped to the first programmed level, then shut itself off as the battery reaches the zener threshold.

The set current can also be turned off by forcing the I_C pin to 0.4V or less using an external transistor or mechanical switch. An example of this is shown in Figure 14.

In this circuit an external control voltage is used to determine the operating state of the 4193. If the control voltage V_C is a logic 1 at the input of the 4025 (CMOS Triple NOR Gate), the voltage at the I_C pin will be less than 0.5V forcing the 4193 off ($< 0.1\mu A$ I_{CC}) both the 2N2222 and 2N2907 will be off insuring long shelf for the battery since less than $1.0\mu A$ is drawn by the circuit.

When V_C goes to a logic 0, $2.0\mu A$ is forced into the I_C pin thru the $2.2M\Omega$ resistor and the NOR gate, and at the same time the 2N2222 and 2N2907 turn on, connecting the battery to the load.

As long as V_C remains low the circuit will regulate the output to 5.0V. This type of circuit is used to back up the main supply voltage when line interruptions occur, a particularly useful feature when using volatile memory systems.

Typical Step-Up Application

Figure 15 shows a common application: a circuit to extend the lifetime of a 9.0V battery. The regulator remains in its quiescent state (drawing only $150\mu A$) until the battery voltage decays below 7.5V, at which time it will start to switch and regulate the output at 7.0V until the battery falls below 2.4V.

If this circuit operates at its typical efficiency of 80%, with an output current of 10mA, at 5.0V battery voltage, then the average input current will be $I_{IN} = (V_{OUT} \times I_L) \div (V_{BAT} \times e_f)$ or $(7.0V \times 10mA) \div (5.0V \times 0.8) = 17.5mA$

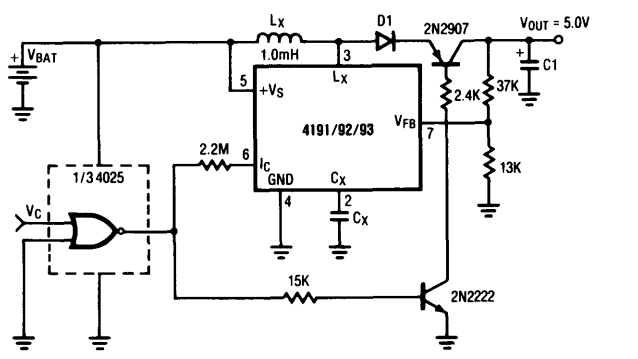


Figure 14. Battery Back-Up Circuit

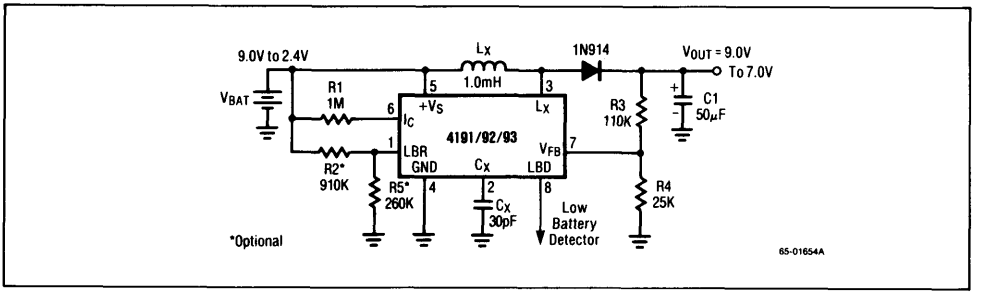


Figure 15. Typical Application: 9.0V Battery Life Extender

Bootstrapped Operation

In step-up applications, power to the 4193 can be derived from the output voltage by connecting the $+V_S$ pin and the top of R1 to the output voltage (Figure 16).

One requirement is that the battery voltage must be greater than 3.5V when the circuit is energized or else there is not enough voltage at pin 5 to start up the I.C. The big advantage of this circuit is the ability to operate down to a terminal battery voltage of 1.0V.

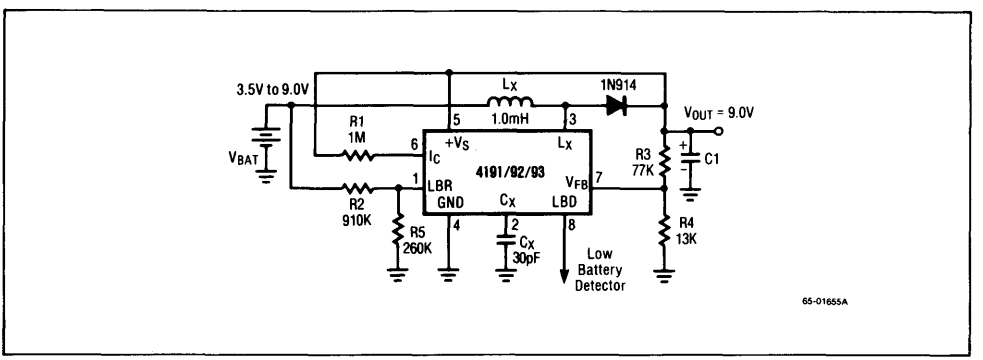


Figure 16. Bootstrapped Operation

Buck-Boost Application

A disadvantage of the standard step-up and step-down circuits is the limitation of the input voltage range; for a step-up circuit, the battery voltage must always be less than the programmed output voltage, and for a step-down circuit, the battery voltage must always be greater than the output voltage. The following circuit (Figure 17) eliminates this disadvantage, allowing a battery voltage above the programmed output voltage to decay to well below the output voltage.

The circuit operation is similar to the step-up circuit operation, except that both terminals of the inductor are connected to switch transistors. This switching method allows the inductor to be disconnected from the battery during the time the inductor is being discharged. A new discharge path is provided by D1, allowing the inductor to be referenced to ground and independent of the battery voltage. The efficiency of this circuit will be reduced to 55-60% by losses in the extra switch transistor and diode. Efficiency can be improved by choosing transistors with low saturation voltages and by using Schottky diodes..

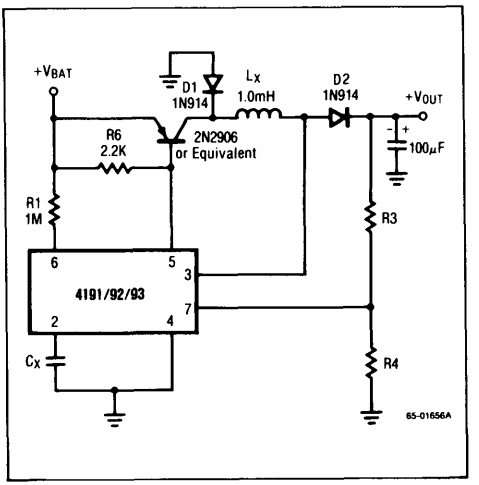


Figure 17. Buck Boost Circuit (V_{BAT} > or < V_{OUT})

Voltage Dependent Oscillator

The 4193's ability to supply load current at low battery voltages depends on the inductor value and the oscillator frequency. Low values of inductance or a low oscillator frequency will cause a higher peak inductor current and therefore increase the load current capability. A large inductor current is not necessarily best, however, because the large amount of energy delivered with each cycle will cause a large voltage ripple at the output, especially at high input voltages. This tradeoff between load current capability and output ripple can be improved with the circuit connection shown in Figure 18. This circuit uses the low battery detector to sense for a low battery voltage condition and will decrease the oscillator frequency after a pre-programmed threshold is reached.

The threshold is programmed exactly as the normal low battery detector connection:

$$V_{TH} = V_{REF}\left(\frac{R2}{R5} + 1\right)$$

When the battery voltage reaches this threshold the comparator will turn on the open collector transistor at pin 8, effectively putting C2 in parallel with C_X. This added capacitance will reduce the oscillator frequency according to the following equation:

$$F_O \approx \frac{2.14 \times 10^{-6}}{C_X + C2}$$

Where C is in pF and F_O is in Hz.

Component values for a typical application might be R2 = 330kΩ, R5 = 150kΩ, C_X = 50pF, and C2 = 100pF. These values would set the threshold voltage at 4.1V and change the operating frequency from 43kHz to 16kHz. Note that this technique may be used for step-up, step-down, or inverting applications.

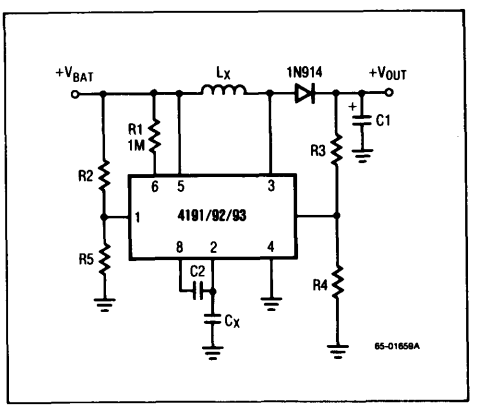


Figure 18. Step-Up Regulator With Voltage Dependent Oscillator

Short Circuit Protection

One disadvantage of the simple application circuits is their lack of short circuit protection, especially for the step-up circuit, which has a very low resistance path for current flow from the input to the output. A current limiting circuit which senses the output voltage and shuts down the 4193 if the output voltage drops too low can be built using the low battery detector circuitry. The low battery detector is connected to sense the output voltage and will shut off the oscillator by forcing pin 2 low if the output voltage drops. Figure 19 shows a schematic of a step-down regulator with this connection.

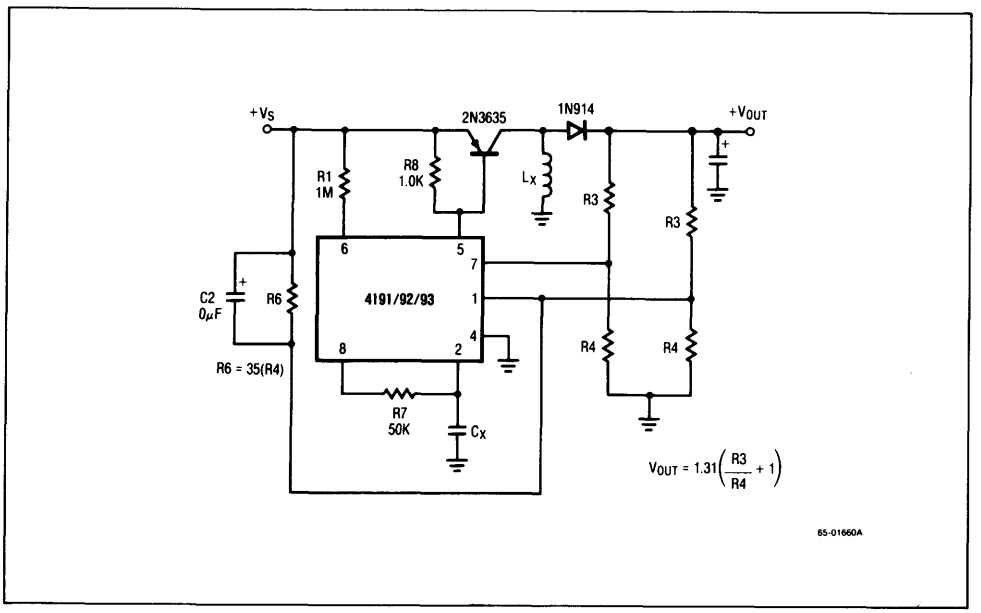


Figure 19. Step-Down Regulator With Short Circuit Protection

R3 and R4 set the output voltage, as in the circuit of Figure 3. Choose resistor values so R2 = R3 and R4 = R5, and make R6 25 to 35 times higher than R5. When the output is shorted, the open collector transistor at pin 8 will force pin 2 low and shut off the oscillator and therefore shut off the external switch transistor. The regulator will then remain in a low current off condition until power is removed and reapplied. C2 provides momentary current to ensure proper start up. This scheme will not work with the simple step-up regulator, but will work with the boost-buck converter, providing short circuit protection in both step-up and step-down modes.

Inductorless Inverter

The 4193 can be used as a low cost inverting power supply for applications where line and load regulation are not critical. The circuit, which is low cost because no external inductor is required, provides a simple inversion of the battery voltage; that is, $-V_{OUT} \approx +V_S$. Diode voltages and transistor V_{SAT}s will reduce the output voltage, however. The circuit (Figure 20) operates as follows: V_{FB} is tied low so the oscillator continuously switches the output transistors. When the internal transistor is on then Q1 is on, and C1 charges through D2. When the internal transistor is off Q1 is off and Q2 is on; Q2 discharges C1 into C2 through D1, effectively reversing the terminals of C1 and charging C2 to a voltage more negative than ground. Poor load regulation can be improved by adding a minimum load.

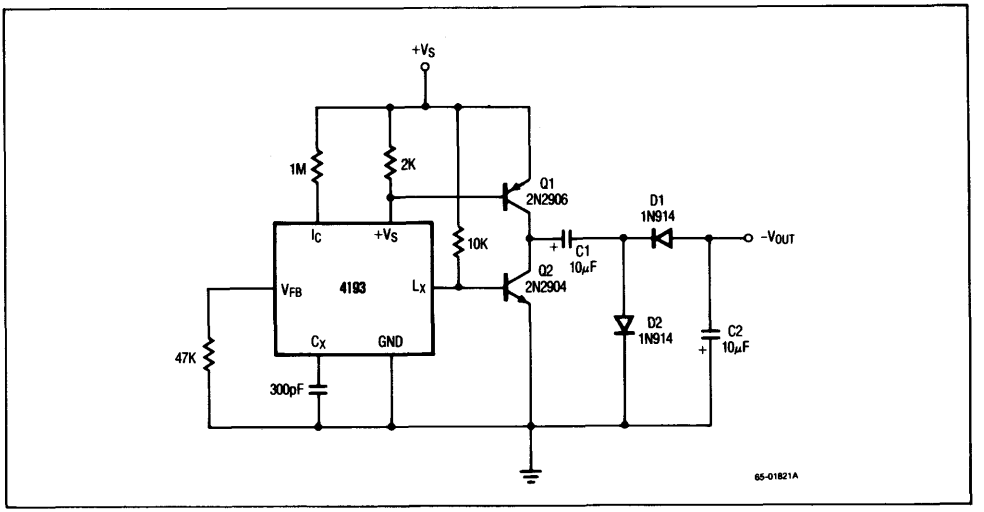


Figure 20. Inductorless Inverter

Transformer Coupled Regulator

One advantage of using a switching regulator to convert DC voltages is that a transformer may be used to transfer energy, providing complete electrical isolation from input to output. Figure 21 shows a simplified conceptual diagram of a push-pull circuit using two RC4193s. The feedback regulating portion of the circuit is not shown for simplicity.

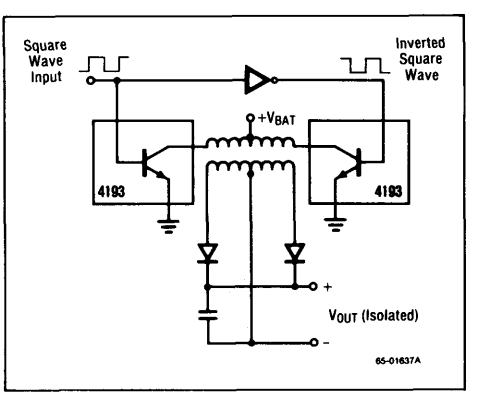


Figure 21. Transformer Coupled Regulator (Simplified Drawing)

The square wave input is inverted and the two signals turn on and off the switching transistors. The opposite phase of these signals ensures that one transistor is always off while the other is on. This on-off push-pull action draws current from the center tap of the transformer primary, converting the DC input voltage into an alternating magnetic field which is coupled over to the transformer secondary. Current induced in the secondary is converted back to DC by the full wave diode rectifier and is filtered by the large output capacitor. There is no connection from input to output through ground or the transformer, so the output is completely isolated electrically.

A complete schematic of the transformer application is shown in Figure 22. The feedback control circuitry, consisting of a zener diode, an optically isolated variable resistor, some resistors and a capacitor, and the gating circuitry internal to the 4193 provides a method of controlling and regulating the output voltage while keeping the output electrically isolated.

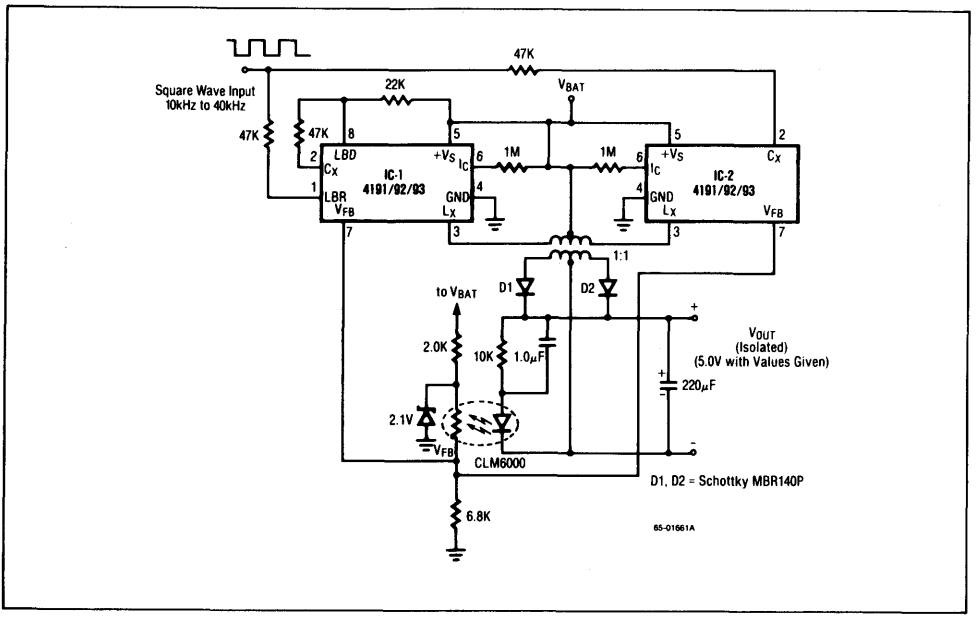


Figure 22. Isolated Push-Pull Transformer Coupled Regulator

The square wave input is applied to the timing pin (C_X) of IC-2, synchronizing the internal oscillator frequency with the square wave. The square wave is inverted by the low battery detection circuit of IC-1, and the inverted waveform synchronizes IC-1's oscillator. This out of phase synchronization ensures that the open collector switching transistors will never conduct simultaneously.

Schottky diodes are used in the rectifier to reduce efficiency losses caused by high diode voltage. Silicon diodes may also be used.

The CLM6000 optically isolated resistor uses light as a transfer medium, avoiding any electrical continuity in the feedback circuit. The feedback control works as follows: The 2.1V zener diode fixes the voltage at the top of a voltage divider. The voltage divider consists of a 6.8K resistor and the variable resistor in the CLM6000. The output of the voltage divider is connected to the feedback inputs of the two 4193s. If the output voltage decreases, then the LED in the CLM6000 emits less light, increasing the value of the variable resistor. As the value of the variable resistor increases, the output of the voltage divider decreases, reducing the voltage at the feedback inputs of the 4193s. The internal comparators sense that the feedback voltage is less than the internal 1.3V reference voltage and therefore increase the on time of the switch transistors. This increase in on time causes more energy to be delivered to the output, increasing the output voltage. The total effect is for the output voltage to remain at a value at which the feedback voltage equals 1.3V. The component values shown will regulate the output at 5.0V; other values of output voltage can be realized by adjusting the value of the 6.8K resistor.

The circuit will supply at least 50mA of output current with efficiency of up to 75%, and with ripple, load, and line regulation of less than 100mV. An RC555 may be used to supply the square wave input.

4391/4193 ± Power Supply

A positive and negative dual tracking power supply using a step up 4193 and an inverting 4391 is shown in Figure 23. The inductor and capacitor values were chosen to achieve the highest practical output currents from a +12V battery, as it decays, while keeping the output voltage ripple under 100mV$_{PP}$ at ±15V output. The circuit may be adapted to other voltages and currents, but note that the 4193 is step-up, so V_{OUT} must be greater than V_{BAT}.

The output voltages may simultaneously be trimmed by adjusting a single resistor value (R3 or R4), because the reference for the negative output is derived from $+V_{OUT}$. This connection also allows the output voltages to track each other with changes in temperature and line voltage.

The timing capacitors are set up exactly as in the voltage dependent oscillator application of Figure 18. The values of R2, R5, C6, and C4 that are given were chosen to optimize for the +12V battery conditions, setting the threshold for oscillator frequency change at V_{BAT} = +8.5V.

As given, this power supply is capable of delivering +45mA and -15mA with regulation, until the battery decays below 5.0V.

For information on adjusting the 4391 to meet a specific application refer to the Raytheon 4391 data sheet.

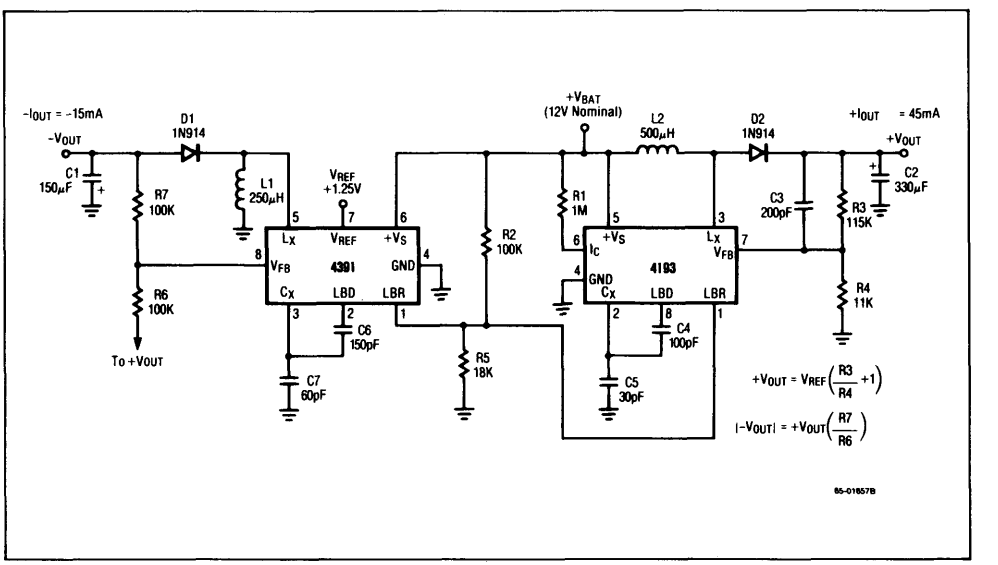


Figure 23. RC4391/RC4193 Power Supply (±15.0V With Values Given)

Definition of Terms

Switch Leakage Current (I_{CO}) The leakage current of the switching transistor in the off condition with 24V applied to pin 3. I_{CO} is measured into pin 3.

Low Battery Bias Current (I_1) The hysteresis current into pin 1 for proper low battery indicator operation (nominally 0.7μA).

Capacitor Charging Current (I_{CX}) The current into (or out of) pin 2. This is the C_X timing current (nominally 5.4μA).

Feedback Input Current (I_{FB}) The current drawn by the feedback input (pin 7). This current must be taken into account when designing the feedback network.

Capacitor Threshold Voltage (V_{THX}) The voltage applied to the C_X pin (pin 2) for which I_{CX} changes direction.

Supply Voltage ($+V_S$) The voltage applied to pin 5. This voltage may not be the same as battery voltage.

Peak Inductor Current (I_{MAX}) The maximum current through the inductor when switching at full duty cycle.

Reference Voltage (V_{REF}) The output of the bandgap reference. This voltage is internal and cannot be directly measured. Other chip references are not specified.

Supply Current (I_S) The current into pin 5. Switch currents and bias currents are specified separately.

Disabled Supply Current (I_{SO}) The current into pin 5 after reference set current (I_C) has been reduced to 10nA.

Switch Current (I_{SW}) The current into pin 3. In typical operation this is also the inductor current.

Efficiency (e_f) The ratio of load power to input power.

Load Regulation (L_I) The ratio of incremental change in output voltage (ΔV_O) to the output voltage design value (V_O) as output current is varied over its specified range.

Oscillator Frequency (F_O) The frequency of the internal oscillator. F_O is set by selection of timing capacitor C_X.

Reference Set Current (I_C) The input current to the reference (pin 6) which will result in normal operations.

Feedback Divider Current (I_A) the DC current flowing through R3 and R4.

Background Information

During the past several years there have been various switching regulator ICs introduced by many manufacturers, all of which attended to the same market, namely controllers for use in power supplies delivering greater than 10W of DC power. Raytheon felt there was another area which could use a switching regulator to even more advantage, the area of battery powered equipment. Battery powered systems have problems peculiar unto themselves: changes in supply voltage, space considerations, battery life and usually cost. The 4193 was designed with each of these in mind.

The 4193 was partitioned to work in an eight pin package, making it 48% smaller than other controllers which go into 14 and 16 pin packages. Battery powered applications require the load as seen by the battery to be as small as possible to extend battery life. To this end, the quiescent current of the 4193 is 15 to 100 times less than controllers designed for nonbattery applications. At the same time the switch transistor can sink 100mA to 0.4V, comparable to or better than higher powered controllers. As an example, the 4193 configured in the step-up mode can supply 5.0V at 40mA output with an input of 3.0V.

Cost is usually a primary consideration in battery powered systems. The 4193, guaranteed to work down to 2.4V, can save the designer and end user money as well because battery costs decrease as the number of cells needed goes down.

Raytheon

Dual Tracking Voltage Regulators

RC4194

Features

- Simultaneously adjustable outputs with one resistor to ±42V
- Load current — ±200mA with 0.04% load regulation
- Internal thermal shutdown at T_j = +175°C
- External balance for $\pm V_O$ unbalancing
- 3W power dissipation

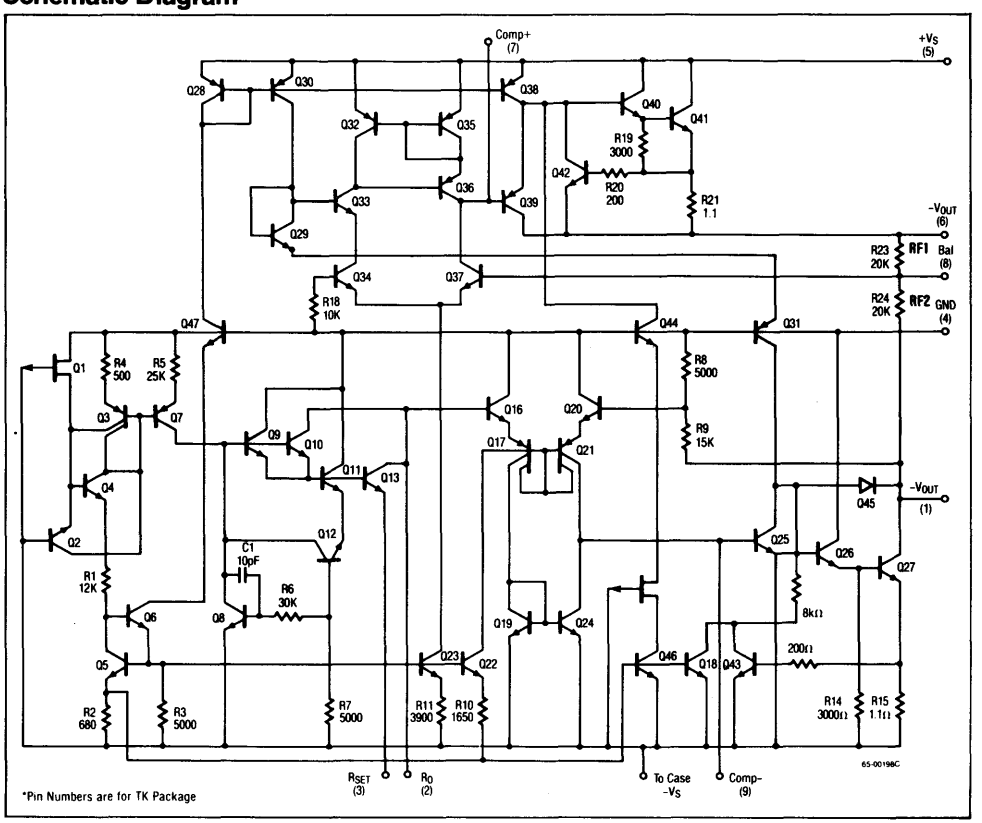
Description

The RM4194 and RC4194 are dual polarity tracking regulators designed to provide balanced or unbalanced positive and negative output voltages at currents to 200mA. A single external resistor adjustment can be used to change both outputs between the limits of ±50mV and ±42V.

These devices are designed for local "on-card" regulation, eliminating distribution problems associated with single-point regulation. To simplify application the regulators require a minimum number of external parts.

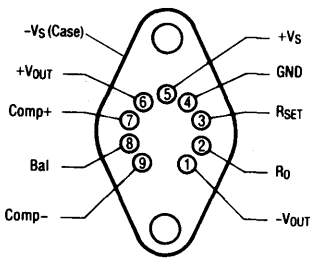
The device is available in three package types to accommodate various power requirements. The TK (TO-66) power package can dissipate up to 3W at T_A = +25°C. The DC 14-pin dual in-line will dissipate up to 1W and the DB 14-pin dual in-line will dissipate up to 625mW.

Schematic Diagram

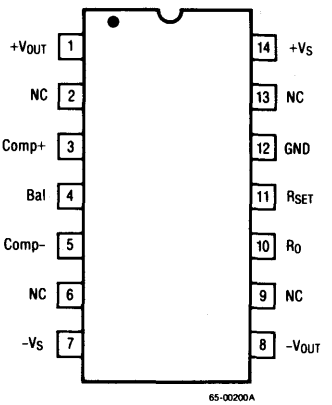


Connection Information

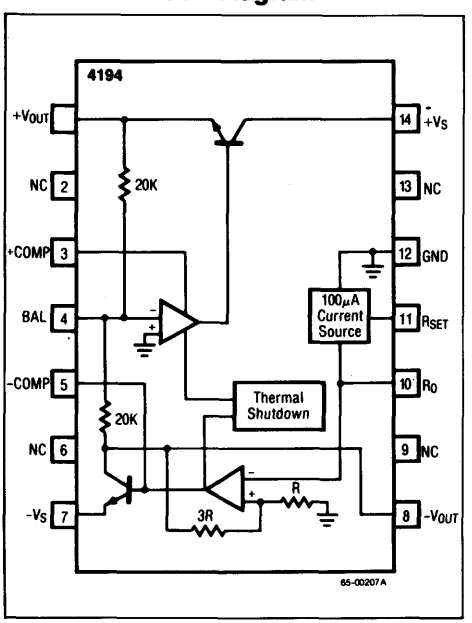
9-Lead
TK (TO-66) Package
(Top View)



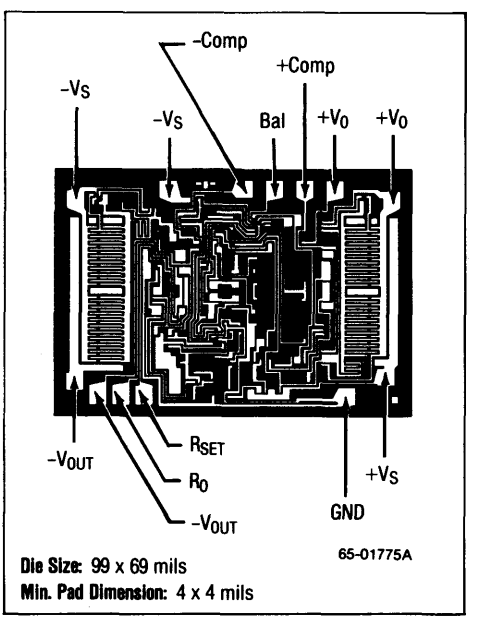
14-Lead
DB and DC Dual In-Line Package
(Top View)



Functional Block Diagram



Mask Pattern



Die Size: 99 x 69 mils
Min. Pad Dimension: 4 x 4 mils

Absolute Maximum Ratings

Supply Voltage (V_{MAX}) to Ground
- RC4194 ..... ±35V
- RM4194 ..... ±45V

Supply Input to Output Voltage Differential
- RC4194 ..... ±35V
- RM4194 ..... ±45V

Load Current
- DB Package 100mA
- DC Package 150mA
- TK Package 250mA

Operating Junction Temperature Range
- RC4194 ..... 0°C to +125°C
- RM4194 ..... -55°C to +150°C

Storage Temperature Range ..... -65°C to +150°C

Lead Soldering Temperature (10 Sec) ..... +300°C

Electrical Characteristics

($\pm 5 \le V_{OUT} \le V_{MAX}$; $I_L = \pm 1mA$; RM4194: $-55°C \le T_j \le +125°C$; RC4194: $0°C \le T_j \le +70°C$ unless otherwise specified)

Parameters	Test Conditions	RC/RM4194 Min	RC/RM4194 Typ	RC/RM4194 Max	Units
Line Regulation	$\Delta V_S = 0.1V_{IN}$		0.04	0.1	$\%V_{OUT}$
Load Regulation Output Voltage Drift With Temperature	4194TK: $I_L < 200mA$, 4194DC: $I_L < 100mA$ $\pm V_S = \pm(V_O + 5)V$		0.002	0.004	$\%V_O \times I_L$ (mA)
Positive Output			0.002	0.015	%/°C
Negative Output			0.003	0.015	%/°C
Supply Current[1] (Positive)	$V_S = \pm V_{MAX}$, $V_O = 0V$, $I_L = 0mA$		+0.8	+2.5	mA
Supply Current[1] (Negative)	$V_S = \pm V_{MAX}$, $V_O = 0V$, $I_L = 0mA$		-1.8	-4.0	mA
Supply Voltage	RM4194	±9.5		±45	V
	RC4194	±9.5		±35	
Output Voltage Scale Factor	$R_{SET} = 71.5k\Omega$, $T_j = +25°C$	2.38	2.5	2.62	kΩ/V
Output Voltage Range	RM4194: $R_{SET} = 71.5k\Omega$	0.05		±42	V
	RC4194: $R_{SET} = 71.5k\Omega$	0.05		±32	
Output Voltage Tracking			0.4	2.0	%
Ripple Rejection	f = 120Hz, $T_j = +25°C$		70		dB
Input-Output Voltage Differential	$I_L = 50mA$, $T_j = +25°C$	3.0			V
Short Circuit Current	$V_S = \pm 30V$, $T_j = +25°C$		300		mA
Output Noise Voltage	$C_L = 4.7\mu F$, $V_O = \pm 15V$ f = 10Hz to 100kHz		250		μV_{RMS}
Internal Thermal Shutdown			175		°C

Notes: 1. The current drain will increase by $50\mu A/V_{OUT}$ on positive side and $100\mu A/V_{OUT}$ on negative side.
2. The specifications above apply for the given junction temperatures since pulse test conditions are used.

Thermal Characteristics

	14-Lead Plastic DIP	14-Lead Ceramic DIP	9-Lead TO-66 Metal Can
Max. Junction Temp.	125°C	175°C	150°C
Max. P_D T_A < 50°C	468mW	1042mW	2381mW
Therm. Res. θ_{JC}	—	60°C/W	7°C/W
Therm. Res. θ_{JA}	160°C/W	120°C/W	42°C/W
For T_A > 50°C Derate at	6.25mW per °C	8.38mW per °C	23.81mW per °C

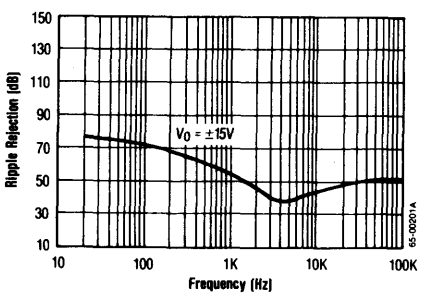
Ordering Information

Part Number	Package	Operating Temperature Range
RC4194DB	Plastic	0°C to +70°C
RC4194DC	Ceramic	0°C to +70°C
RC4194TK	TO-66	0°C to +70°C
RM4194DC	Ceramic	-55°C to +125°C
RM4194DC/883B*	Ceramic	-55°C to +125°C
RM4194TK	TO-66	-55°C to +125°C

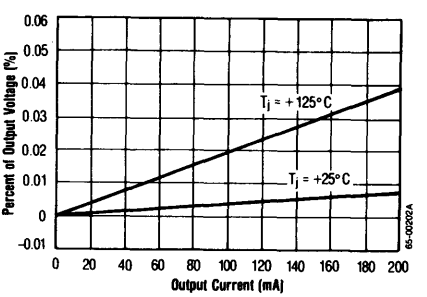
*MIL-STD-883, Level B Processing

Typical Electrical Data

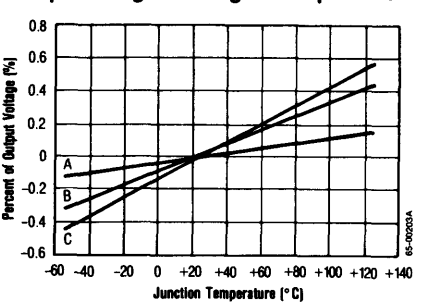
Ripple Rejection



Load Regulation vs. Output Current



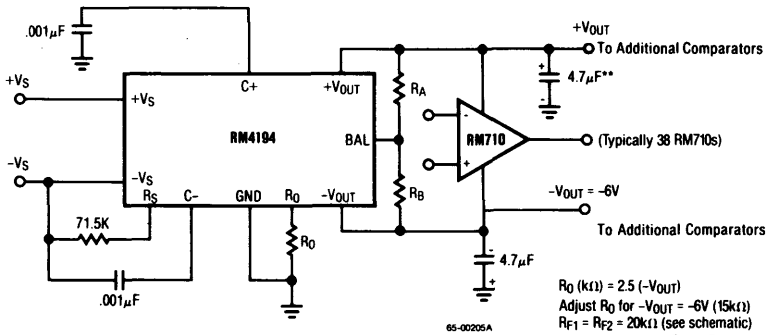
Output Voltage Tracking vs. Temperature



A = % Tracking of Output Voltage
B = T.C. for Positive Regulator
C = T.C. for Negative Regulator

Typical Applications

Unbalanced Output Voltage — Comparator Application

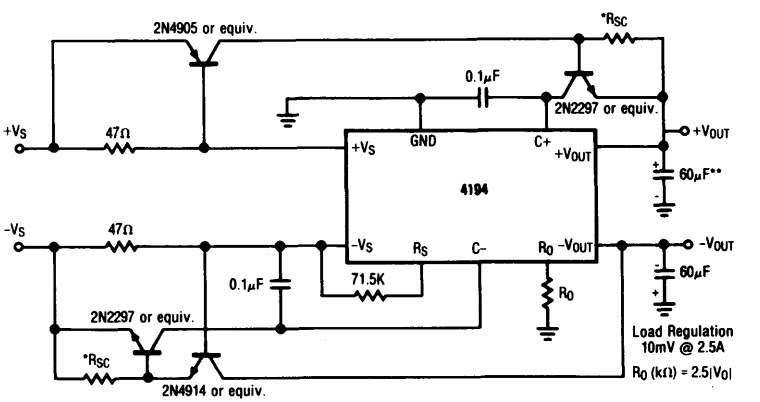


R_O (kΩ) = 2.5 ($-V_{OUT}$)
Adjust R_O for $-V_{OUT}$ = -6V (15kΩ)
$R_{F1} = R_{F2}$ = 20kΩ (see schematic)

$$|+V_{OUT}| = |-V_{OUT}| \frac{R_{F1} \,||\, R_A}{R_{F2} \,||\, R_B}$$

$R_A = \infty$ when $|+V_{OUT}| > |-V_{OUT}|$
$R_B = \infty$ when $|+V_{OUT}| < |-V_{OUT}|$
For $+V_{OUT}$ = 12 when $-V_{OUT}$ = 6V
$R_A = \infty$
R_B = 20kΩ

High Output Application



$$*R_{SC} = \frac{0.7}{I_{SC}}.$$

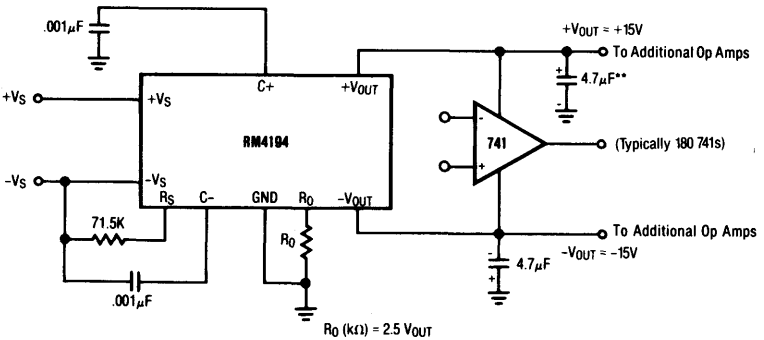
Note: Compensation and bypass capacitor connections should be close as possible to the 4194.

**Optional usage — not as critical as $-V_O$ bypass capacitors.

65-00206A

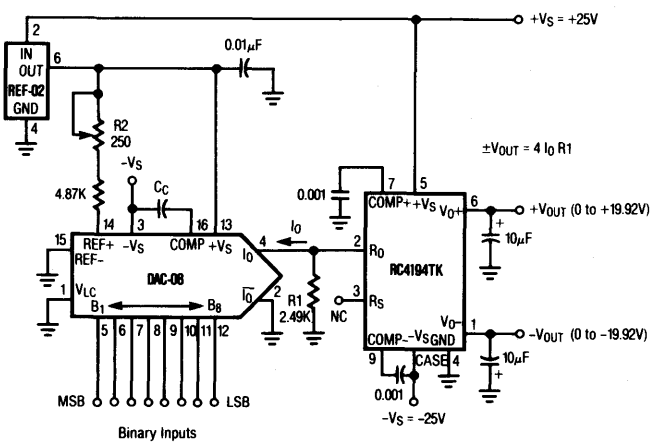
Typical Applications (Continued)

Balanced Output Voltage — Op Amp Application

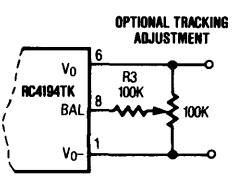


65-00204A

Digitally Controlled Dual 200mA Voltage Regulator



Adjust R2 for -19.92V at -VOUT with all "1s" at binary inputs, then optionally adjust R3 for +19.92V at +VOUT



65-01725A

Raytheon

Fixed ±15V Dual Tracking Voltage Regulator

RC4195

Features

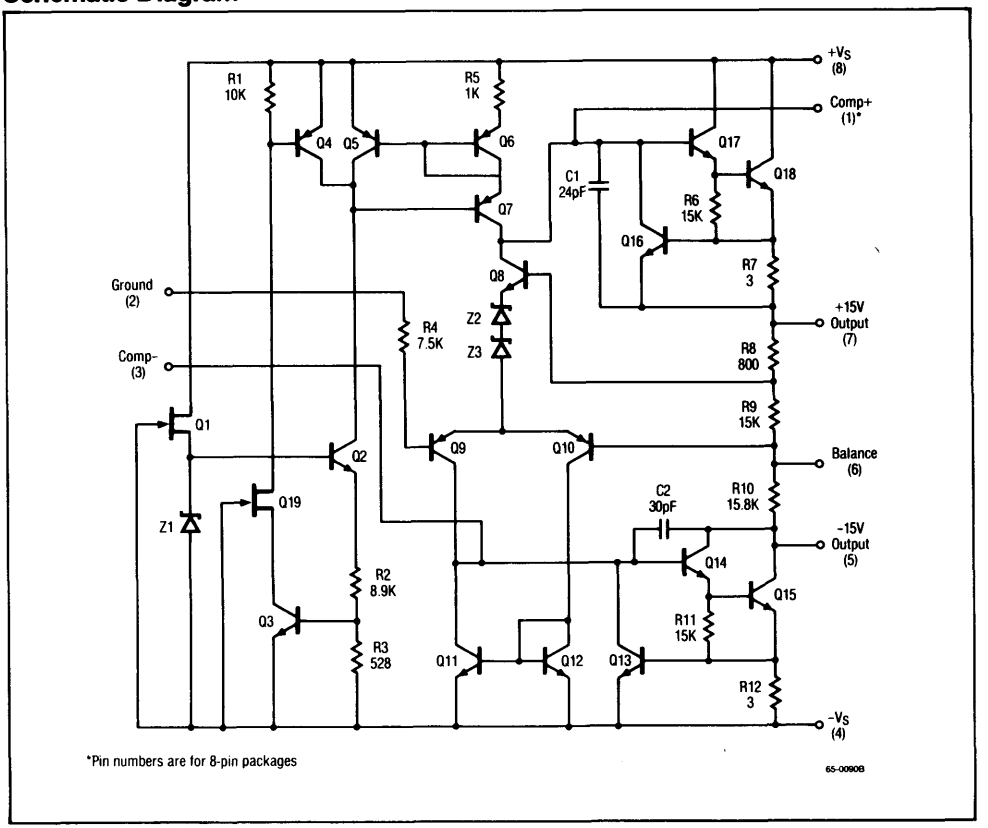
- ±15V operational amplifier power at reduced cost and component density
- Thermal shutdown at T_j = +175°C in addition to short circuit protection
- Output currents to 100mA
- May be used as single output regulator with up to +50V output
- Available in TO-66, TO-99 and 8-Pin Plastic Mini-DIP
- No external frequency compensation required

Description

The RC/RM4195 is a dual polarity tracking regulator designed to provide balanced positive and negative 15V output voltages at currents up to 100mA. This device is designed for local "on-card" regulation, eliminating distribution problems associated with single point regulation. The regulator is intended for ease of application. Only two external components are required for operation (two 10μF bypass capacitors).

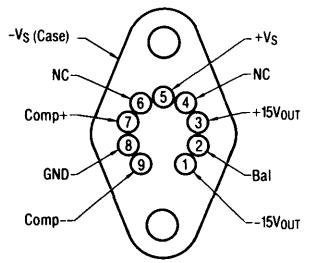
The device is available in three package types to accommodate various applications requiring economy, high power dissipation, and reduced component density.

Schematic Diagram

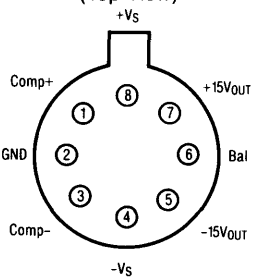


Connection Information

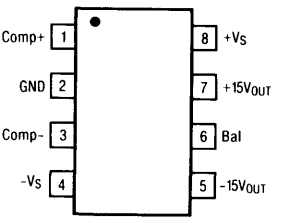
TO-66
Metal Can
(Top View)



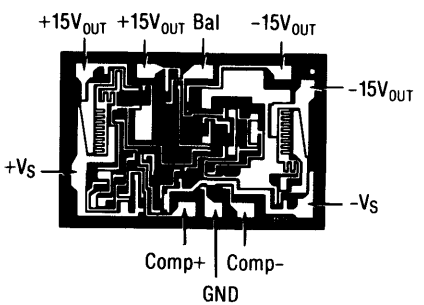
TO-99
Metal Can
(Top View)



8-Lead
Plastic Dual In-Line
(Top View)

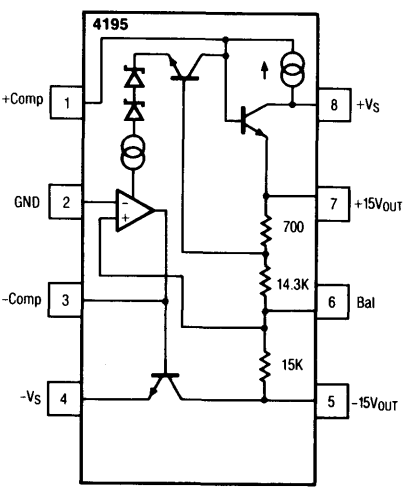


Mask Pattern



Die Size: 49 x 74 mils
Min. Pad Dimensions: 4 x 4 mils

Functional Block Diagram



Pin out for dual in-line package shown.

65-00089A

Ordering Information

Part Number	Package	Operating Temperature Range
RC4195NB	Plastic	0°C to +70°C
RC4195T	TO-99	0°C to +70°C
RC4195TK	TO-99	0°C to +70°C
RM4195T	TO-99	-55°C to +125°C
RM4195T/883B*	TO-99	-55°C to +125°C
RM4195TK	TO-66	-55°C to +125°C

*MIL-STD-883, Level B Processing

Absolute Maximum Ratings

Supply Voltage ($\pm V_S$) to Ground ..... ±30V
Load Current
TK Package 150mA
T and NB Package 100mA
Operating Junction Temperature Range
RC4195 ..... 0°C to +125°C
RM4195 ..... -55°C to +150°C
Storage Temperature
Range ..... -65°C to +150°C
Lead Soldering Temperature
(10 Sec) ..... +300°C

Thermal Characteristics

	8-Lead Plastic DIP	8-Lead TO-99 Metal Can	9-Lead TO-66 Metal Can
Max. Junction Temp.	125°C	175°C	150°C
Max. P_D $T_A < 50°C$	468mW	658mW	2381mW
Therm. Res. θ_{JC}	—	50°C/W	7°C/W
Therm. Res. θ_{JA}	160°C/W	190°C/W	42°C/W
For $T_A > 50°C$ Derate at	6.25mW per °C	5.26mW per °C	23.81mW per °C

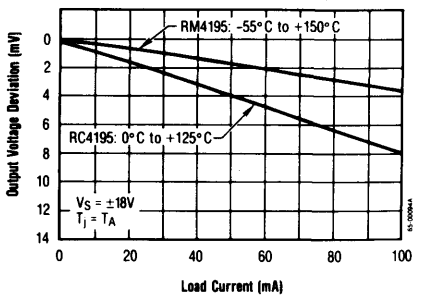
Electrical Characteristics (I_L = ±1mA, V_S = ±20V, C_L = 10μF RM4195: -55°C ≤ T_j ≤ +125°C; RC4195: 0°C ≤ T_j ≤ +70°C unless otherwise specified)[1]

Parameters	Test Conditions	RC/RM4195 Min	Typ	Max	Units
Line Regulation	V_S = ±18V to ±30V		2	20	mV
Load Regulation	I_L = 1mA to 100mA		5	30	mV
Output Voltage Drift With Temperature			0.005	0.015	%/°C
Supply Current	V_S = ±30V, I_L = 0mA		±1.5	±4.0	mA
Supply Voltage		18		30	V
Output Voltage	T_j = +25°C	14.5	15.0	15.5	V
Output Voltage Tracking			±50	±300	mV
Ripple Rejection	f = 120Hz, T_j = +25°C		75		dB
Input-Output Voltage Differential	I_L = 50mA	3			V
Short Circuit Current	T_j = +25°C		220		mA
Output Voltage Noise	T_j = +25°C, f = 100Hz to 10kHz		60		μV_{RMS}
Internal Thermal Shutdown			175		°C

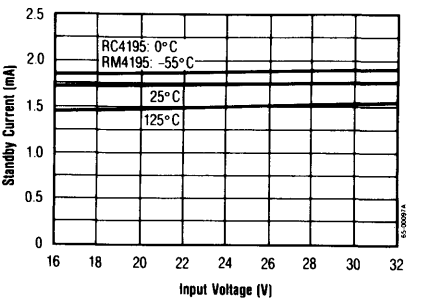
Notes: 1. The specifications above apply for the given junction temperature since pulse test conditions are used.

Typical Performance Characteristics

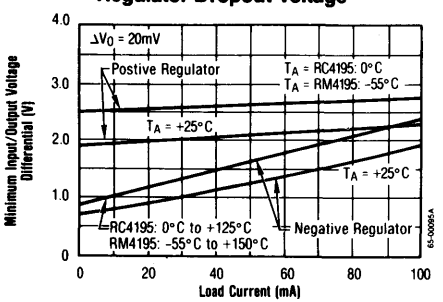
Output Load Regulation



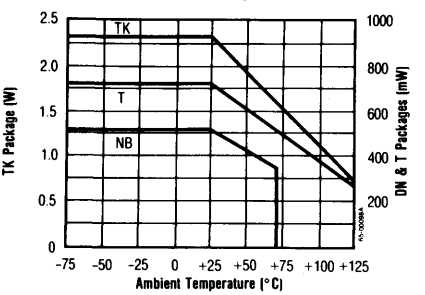
Standby Current Drain



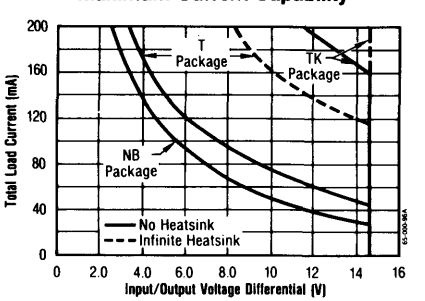
Regulator Dropout Voltage



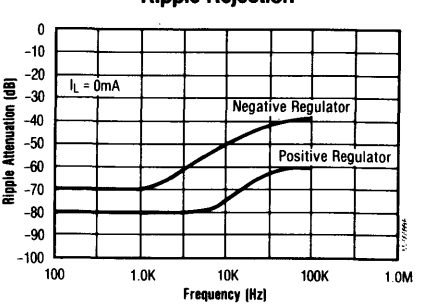
Power Dissipation



Maximum Current Capability

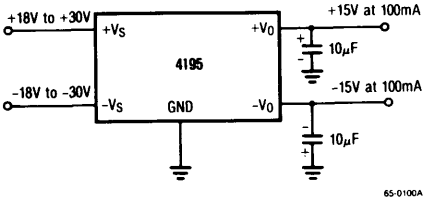


Ripple Rejection

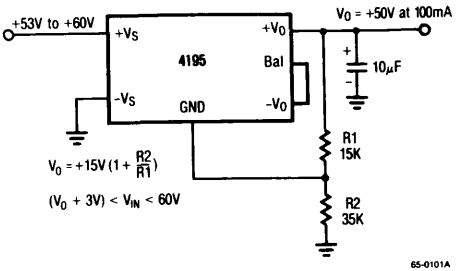


Typical Applications

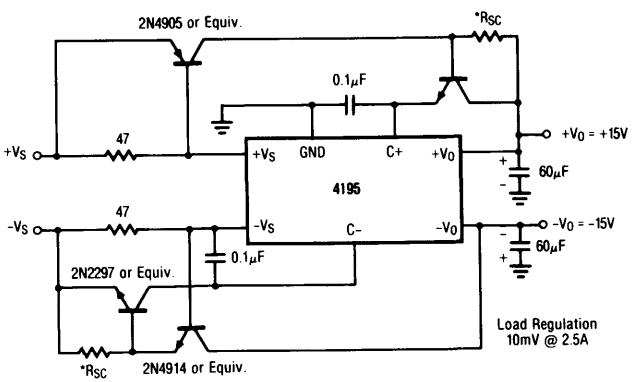
Balanced Output (V_O = ±15V)



Positive Single Supply (+15V < V_O < +50V)



High Output Current



$$*R_{SC} = \frac{0.7}{I_{SC}}$$

Raytheon

Inverting Switching Regulator

RC4391

Features

- Converts a positive voltage into a negative voltage
- Specifically designed for low power applications, including batteries
- Adjustable output voltage
- High switch current capability
- Low quiescent supply current — 175μA typical
- Eight pin mini dual in-line package
- Low battery detection circuitry
- High efficiency — 70% typical

Description

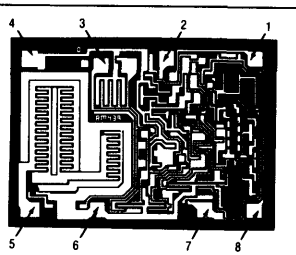
Raytheon's micropower inverting switching regulator, RC/RM4391, is a monolithic low power switching regulator specifically designed for low power inverting applications. The RC4391 contains an internal 1.25V bandgap voltage reference, switch transistor, comparator, free running oscillator, and low battery detection circuitry. These components are interconnected to minimize the number of external components required in typical inverting applications (see Figure 2). The RC4391 requires an inductor, diode, timing capacitor, and an R2, R1 network to achieve a negative output voltage. The RC4391 allows the designer flexibility in designing unconventional applications such as replacing the internal bandgap reference with an external or system reference, or using the low battery detection comparator and transistor as voltage level detectors or for signal generation.

A typical application would combine the RC4391 with the RC4193 micropower switching regulator to convert a single input voltage into a ±12V or ±15V op amp power supply. The single voltage can be from a battery, bridge rectifier or existing +5.0V bus on card for this application (see Figure 7).

Absolute Maximum Ratings

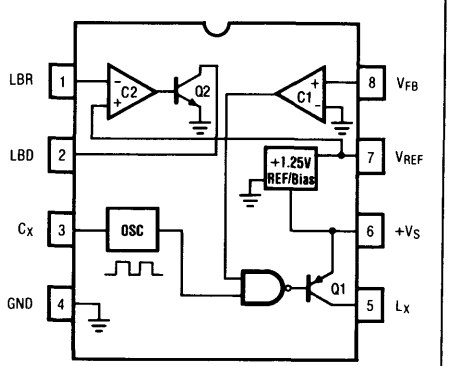
Internal Power Dissipation 500mW
Supply Voltage (Without External Series Pass Transistor) ..... +30V-|V_{OUT}|
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range
RM4391 ..... -55°C to +125°C
RV4391 ..... -40°C to +85°C
RC4391 ..... 0°C to +70°C
Switch Current (I_{SW}) ..... 375mA peak

Mask Pattern



Die Size: 69 x 50 mils
Min. Pad Dimensions: 4 x 4 mils

Functional Block Diagram



Thermal Characteristics

	8-Lead Plastic DIP	8-Lead Ceramic DIP
Max. Junction Temp.	125°C	175°C
Max. P_D T_A < 50°C	468mW	833mW
Therm. Res. θ_{JC}	—	45°C/W
Therm. Res. θ_{JA}	160°C/W	150°C/W
For T_A > 50°C Derate at	6.25mW per °C	8.33mW per °C

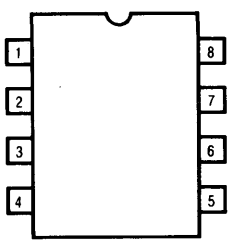
Ordering Information

Part Number	Package	Operating Temperature Range
RC4391DE	Ceramic	0°C to +70°C
RC4391NB	Plastic	0°C to +70°C
RV4391DE	Ceramic	-40°C to +85°C
RV4391NB	Plastic	-40°C to +80°C
RM4391DE	Ceramic	-55°C to +125°C
RM4391DE/883B*	Ceramic	-55°C to +125°C

*MIL-STD-883, Level B Processing

Connection Information

8-Lead
Dual In-Line Package
(Top View)



55-01612A

Pin	Function
1	Low Battery Resistor (LBR)
2	Low Battery Detector (LBD)
3	Timing Capacitor (C_X)
4	Ground
5	External Inductor (L_X)
6	+Supply Voltage (+V_S)
7	+1.25V Reference Voltage (V_{REF})
8	Feedback Voltage (V_{FB})

Cautionary Note: Care must be taken not to exceed the maximum current rating of the switch transistor. Select the inductor value and timing capacitor value carefully, and when prototyping, start with low input voltages first.

Electrical Characteristics (Circuit of Figure 2, V_S = +6.0V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Condition	RC4391 Min	RC4391 Typ	RC4391 Max	Units
Supply Current	I_S	V_S = +4.0V, No External Loads		170	250	μA
		V_S = +25V, No External Loads		300	500	
Output Voltage	V_{OUT}	$V_{OUT\ nom}$ = -5.0V	-5.35	-5.0	-4.65	V
		$V_{OUT\ nom}$ = -15V	-15.85	-15	-14.15	
Line Regulation		$V_{OUT\ nom}$ = -5.0V, C_X = 150pF, V_S = +5.8V to +15V		1.5	3.0	% V_{OUT}
		$V_{OUT\ nom}$ = -15V, C_X = 150pF, V_S = +5.8V to +15V		1.0	2.0	

Electrical Characteristics (Continued)

(Circuit of Figure 2, V_S = +6.0V over the full operating temperature range unless otherwise noted)

Parameter	Symbol	Condition	RC4391 Min	RC4391 Typ	RC4391 Max	Units
Load Regulation		$V_{OUT\ nom}$ = -5.0V, C_X = 350pF, V_S = +4.5V, P_{LOAD} = 0mW to 75mW		0.2	0.4	% V_{OUT}
		$V_{OUT\ nom}$ = -15V, C_X = 350pF, V_S = +4.5V, P_{LOAD} = 0mW to 75mW		0.07	0.14	
Reference Voltage	V_{REF}		1.18	1.25	1.32	V
Switch Current	I_{SW}	Pin 5 = 5.5V	75	100		mA
Switch Leakage Current	I_{CO}	Pin 5 = -24V		0.01	5.0	μA
Timing Pin Current	I_{CX}	Pin 3 = 0V	6.0	10	14	μA
LBD Leakage Current		Pin 1 = 1.5V, Pin 2 = 6.0V		0.01	5.0	μA
LBD on Current		Pin 1 = 1.1V, Pin 2 = 0.4V	210	600		μA
LBR Bias Current		Pin 1 =1.5V		0.7		μA

Electrical Characteristics (Continued)

(Circuit of Figure 2, V_S = +6.0V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Condition	RC4391 Min	RC4391 Typ	RC4391 Max	Units
Supply Voltage	$+V_S$		+4.0		+30-|V_{OUT}|	V
Supply Current	I_{IN}	V_S = +25V		300	500	μA
Reference Voltage	V_{REF}		1.13	1.25	1.36	V
Output Voltage	V_{OUT}	$V_{OUT\ nom}$ = -5.0V	-5.5	-5.0	-4.5	V
		$V_{OUT\ nom}$ = -15V	-16.5	-15	-13.5	
Line Regulation		$V_{OUT\ nom}$ = -5.0V, C_X = 150pF, V_S = +5.8V to +15V		2.0	4.0	% V_{OUT}
		$V_{OUT\ nom}$ = -15V, C_X =150pF, V_S = +5.8V to +15V		1.5	3.0	
Load Regulation		$V_{OUT\ nom}$ = -5.0V, C_X = 350pF, V_S = +4.5V, P_{LOAD} = 0mW to 50mW		0.2	0.5	% V_{OUT}
		$V_{OUT\ nom}$ = -15V, C_X = 350pF, V_S = +4.5V, P_{LOAD} = 0mW to 50mW		0.2	0.6	
Switch Leakage Current	I_{CO}	Pin 5 = -24V		0.1	30	μA

Principles of Operation

The basic switching inverter circuit is the building block on which the complete inverting application is based.

A simplified diagram of the voltage inverter circuit with ideal components and no feedback circuitry is shown in Figure 1. When the switch S is closed, charging current from the battery flows through the inductor L, which builds up a magnetic field, increasing as the switch is held closed. When the switch is opened, the magnetic field collapses, and the energy stored in the magnetic field is converted into a current which flows through the inductor in the same direction as the charging current. Because there is no path for this current to flow through the switch, the current must flow through the diode to charge the capacitor C. The key to the inversion is the ability of the inductor to become a source when the charging current is removed.

The equation V = (L) (di/dt) gives the maximum possible voltage across the inductor; in the actual application, feedback circuitry and the output capacitor will decrease the output voltage to a regulated fixed value.

A complete schematic for the standard inverting application is shown in Figure 2. The ideal switch in the simplified diagram is replaced by the PNP transistor switch between pins 5 and 6. C_F functions as the output filter capacitor, and D1 and L_X replace D and L.

When power is first applied, the ground sensing comparator (Pin 8) compares the output voltage to the +1.25V voltage reference. Because C_F is initially discharged a positive voltage is applied to the comparator, and the output of the comparator gates the squarewave oscillator. This gated squarewave signal turns on, then off, the PNP output transistor. This turning on and off of the output transistor performs the same function as opening and closing the ideal switch in the simplified diagram; i.e., it stores energy in the inductor during the on time and releases it into the capacitor during the off time.

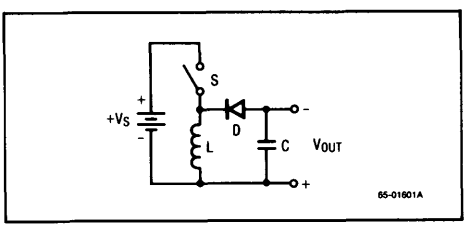
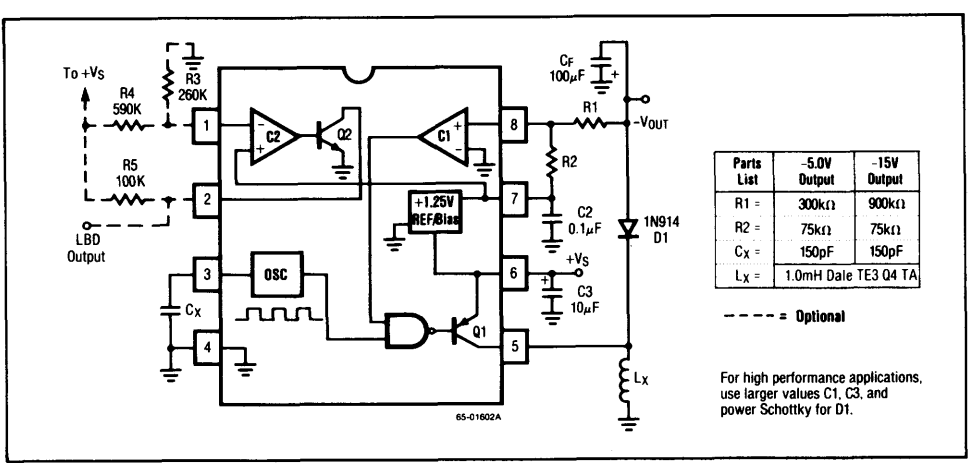


Figure 1. Simplified Voltage Inverter



Parts List	-5.0V Output	-15V Output
R1 =	300kΩ	900kΩ
R2 =	75kΩ	75kΩ
Cx =	150pF	150pF
Lx =	1.0mH Dale TE3 Q4 TA	

---- = Optional

For high performance applications, use larger values C1, C3, and power Schottky for D1.

Figure 2. 4391 Standard Application Circuit

The comparator will continue to gate the oscillator to the switch transistor until enough energy has been stored in the output capacitor to make the comparator input voltage decrease to less than 0V. The voltage applied to the comparator is set by the output voltage, the reference voltage, and the ratio of R1 to R2.

Design Equations

The inductor value and timing capacitor value must be carfully tailored to the ripple, input voltage range, output voltage, switch transistor maximum current, and output load current requirements of the application. The key to the problem is to select the correct inductor value to meet the load current requirement, without selecting values of C_X and L_X that cause excessive inductor current (which may saturate the inductor or burn up the switch transistor). Following are design equations to help select values for C_X and L_X under the most difficult conditions, where the absolute value of the output voltage is greater than the supply voltage ($|V_{OUT}| > +V_S$).

(1) $$C_X(pF) \approx \frac{3.0 \times 10^6}{F_O(Hz)}$$

Select an operating frequency and calculate a value for C_X from equation (1).

(2) $$L_X \text{ (Henries)} = \frac{(+V_S - V_{SW})^2}{(I_{OUT(avg)})(8.0)(f_O)(|V_{OUT}| + V_D)}$$

where L = Inductor value in Henrys
f_O = Switching frequency
V_{SW} = Satauration voltage of switching transistor
V_D = Diode voltage

Then find a value for L_X based on the minimum supply voltage to be applied.

(3) $$I_{MAX} = \frac{+V_S - V_{SW}}{(2)(L_X)(f_O)}$$

Check and see if the maximum inductor current (I_{MAX}) is greater than the 375mA rating of the switch transistor. If I_{MAX} is too high, then an external switch transistor must be used in place of Q1.

As an alternative to using the design equations, the following process can be used to optimize circuit performance.

1. Select an operating frequency based on efficiency and capacitor size requirements (frequencies from 10kHz to 50kHz are typical).
2. Build the circuit and apply the worst case conditions to it, i.e., the lowest battery voltage and the highest load current at the desired output voltage.
3. Adjust the inductor value down until the desired output voltage is achieved, then go a little lower (approximately 15%) to cover manufacturing tolerances.
4. Check the output voltage with an oscilloscope for ripple, at high supply voltages, at voltages as high as are expected. Also check for efficiency by monitoring supply and output voltages and currents (eff = $(V_{OUT})(I_{OUT})/(+V_S)(I_{SY})$ x 100%).
5. If the efficiency is poor, go back to (1) and start over. If the ripple is excessive, then increase the output filter capacitor value or start over.

Timing

The oscillator creates a squarewave using a method similar to the 555 timer IC, with a current steering flip-flop controlled by two voltage sensing comparators. The value of the timing capacitor is set according to the following equation:

$$f_{OP}(Hz) \approx \frac{3.0 \times 10^{-6}}{C_X}$$

The squarewave output of the oscillator is internal and cannot be directly measured, but is equal in frequency to the triangle waveform measurable at pin 3. The switch transistor is normally on when the triangle waveform is ramping up and off when ramping down. Capacitor selection depends on the application; higher operating frequencies will reduce the output voltage ripple while trading off efficiency and load regulation. Keep the capacitor lead length short.

Inductors

Efficiency and load regulation will improve if a quality high Q inductor is used. A ferrite pot core is recommended; the wind-yourself type with an air gap adjustable by washers or spacers is very useful for bread boarding prototypes. Care must be taken to choose a permeable enough core to

handle the magnetic flux produced at I_{MAX}; if the core saturates then efficiency and output current capability are severely degraded and excessive current will flow through the switch transistor. An isolated AC current probe for an oscilloscope is an excellent tool for saturation problems; with it the inductor current can be monitored for nonlinearity at the peaks (a sign of saturation).

Low Battery Detector

An open collector signal transistor Q2 with comparator C2 provides the designer with a method of signaling a display or computer whenever the battery voltage falls below a programmed level. This level is determined by the +1.25V reference level and by the selection of two external resistors according to the equation:

$$V_{TH} = V_{REF}\left(\frac{R4}{R3} + 1\right)$$

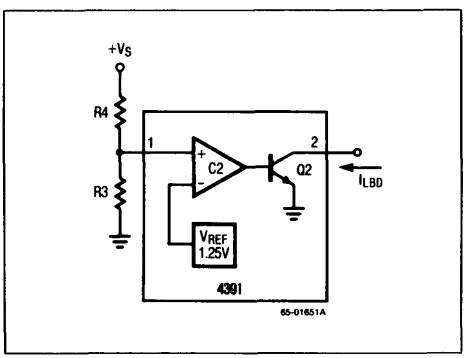


Figure 3. Low Battery Detector

When the battery voltage drops below this threshold Q2 will turn on and sink over 600μA typically. The low battery detector circuitry may also be used for other, less conventional applications.

Device Shutdown

The entire device may be shut down to an extremely low current non-operating condition by disconnecting the ground (pin 4). This can be easily done by putting an NPN transistor in series with the ground pin and switching it with an external signal. This switch will not affect the efficiency of operation, but will add to and increase the reference voltage by an amount equal to the saturation voltage of the transistor used.

External Switch Transistors

Figure 4 is a schematic of an inverting power supply using an external PNP switch transistor. Supply voltage is applied to the IC via the 1kΩ resistor; when the internal switch transistor is turned on current through the 50Ω resistor is also drawn through the 1kΩ resistor, creating a voltage drop from base to emitter of the external switch transistor. This drop turns on the external transistor. In place of the standard 1N914 diode a Schottky diode is used to increase efficiency.

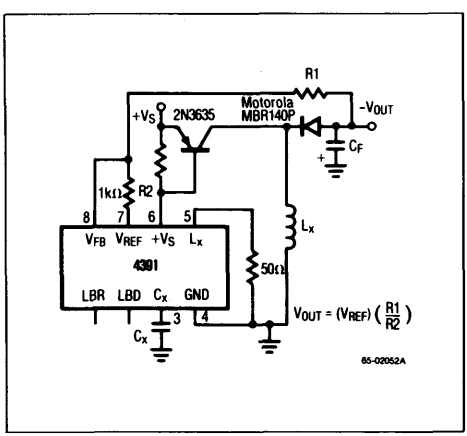


Figure 4. High Current, High Efficiency Supply

Another external transistor circuit is shown in Figure 5. This circuit uses an NPN transistor in place of the PNP of Figure 4. Use of the NPN allows for a greater switch current capability but reduces efficiency. An optional zener diode allows for higher input voltages than the 4391 can tolerate alone. Note than even though the addition of the zener raises the maximum allowable supply voltage, it does not alter the maximum change of supply voltage, which equals the maximum supply voltage minus the minimum supply voltage (ΔV = 30V - 4.0V = 26V). So, with a 10V zener diode, the supply voltage range will be 14V to 40V.

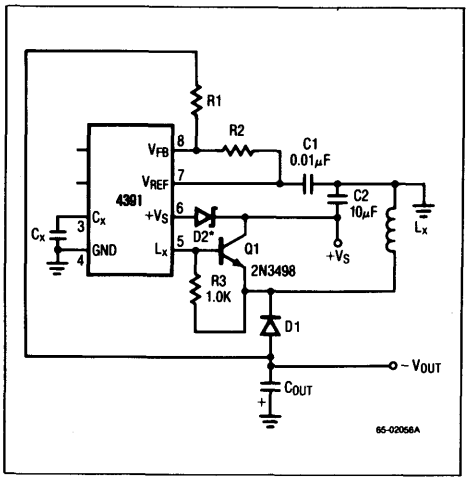


Figure 5. High Voltage/High Power Application Circuit

Voltage Dependent Oscillator

The 4391's ability to supply load current at low battery voltages depends on the inductor value and the oscillator frequency. Low values of inductance or a low oscillator frequency will cause a higher peak inductor current and therefore increase the load current capability. A large inductor current is not necessarily best, however, because the large amount of energy delivered with each cycle will cause a large voltage ripple at the output, especially at high input voltages. This tradeoff between load current capability and output ripple can be improved with the circuit connection shown in Figure 6. This circuit uses the low battery detector to sense for a low battery voltage condition and will decrease the oscillator frequency after a pre-programmed threshold is reached.

The threshold is programmed exactly as the normal low battery detector connection:

$$V_{TH} = V_{REF}\left(\frac{R4}{R3}\right) = 1$$

When the battery voltage reaches this threshold the comparator will turn on the open collector transistor at pin 2, effectively putting C_Y in parallel

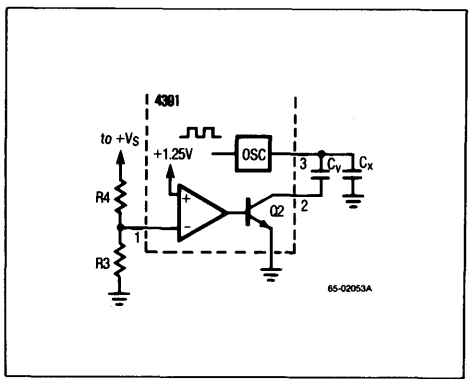


Figure 6. Voltage Dependent Oscillator

with C_X. This added capacitance will reduce the oscillator frequency according to the following equation:

$$F_O \approx \frac{3.0 \times 10^{-6}}{C_x + C_y}$$

Dual Tracking Power Supply

A schematic of a power supply that will provide positive and negative voltages from a single battery is shown in Figure 7. The circuit uses a 4391 to generate a negative voltage and uses a 4193 to generate a positive voltage. The resistor values given will set the outputs at ±15V. Both output voltages can be adjusted simultaneously by changing a single resistor value, but note that, because the 4193 is in a step-up mode, the battery voltage must always be less than the programmed positive output voltage. The inductor and timing capacitor values shown were chosen to optimize circuit performance for the following application specifications:

V_{OUT} = ±15V
V_{BAT} = +12V
V_{BAT} Range = +12V to +5V
I_{OUT} = +45mA and -15mA
Output ripple less than 100m$V_{p\text{-}p}$
Efficiency ≈ 75%

The output power levels shown above represent the highest practical power levels using the internal switch transistors. Higher power supplies

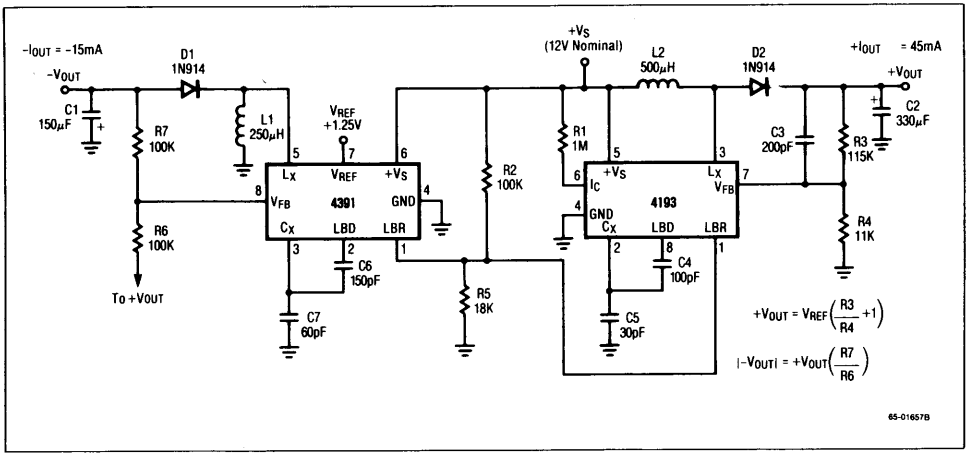


Figure 7. RC4391/RC4193 Power Supply (±15.0V With Values Given)

will probably have to use external switch transistors to avoid overheating and drawing excessive switch current.

The timing capacitors are set up as in the voltage dependent oscillator application (Figure 6), so that the operating frequency will decrease at low battery voltages, thus allowing a greater load current capability. The values of R2, R5, C4, and C6 were chosen to optimize for the +12V to +5V battery conditions, setting the threshold for frequency change at +8.5V. For more information on designing with the RC4193, refer to the RC4191/2/3 data sheet.

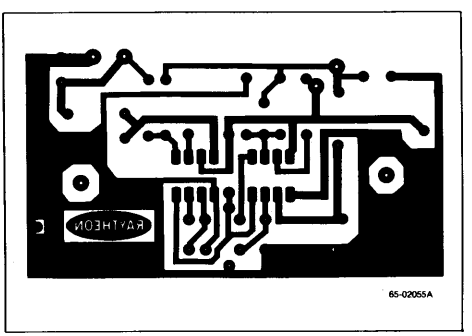


Figure 8. Dual Power Supply PC Layout (Component Side View)

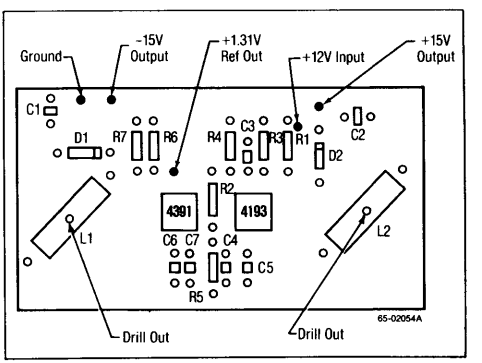


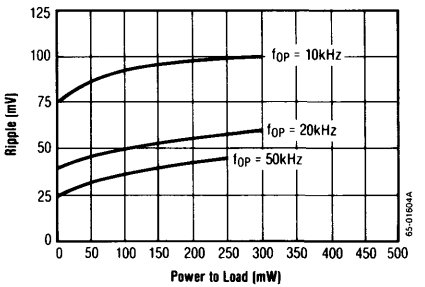
Figure 9. Dual Power Supply Component Placement Diagram

Troubleshooting Chart for Circuit of Figure 2

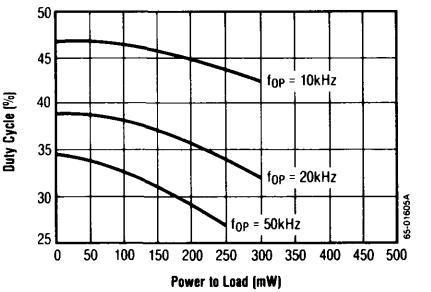
Symptom	Possible Problems
Device draws excessive current when power is applied.	Excessive supply voltage. Leakage or short on pin 3.
Excessive current pulses during normal operation (motorboating) or excessive output ripple.	Operating frequency too low. Excessive supply voltage. Inadequate V_{REF} bypass. Inadequate output filtering.
Slightly positive output voltage no current pulses.	Feedback loop disconnected (R1, R2). Pin 5 disconnected. Supply voltage too low. Bad rectifier diode. Bad grounding.
Excessively negative output voltage.	Feedback loop disconnected (R1, R2).
Poor load regulation and/or poor efficiency.	Bad rectifier diode. Excessive inductor resistance. Excessive switch resistance. Operating frequency too high. Inductor saturating.

Typical Performance Characteristics

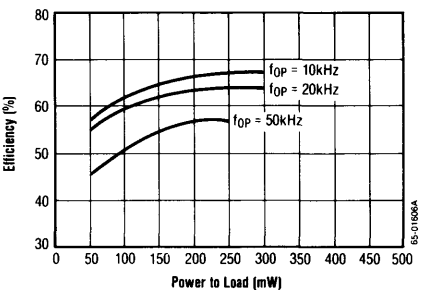
Power vs. Ripple



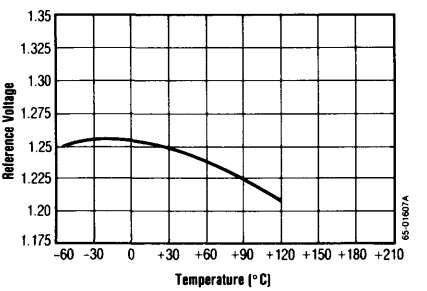
Power vs. Duty Cycle



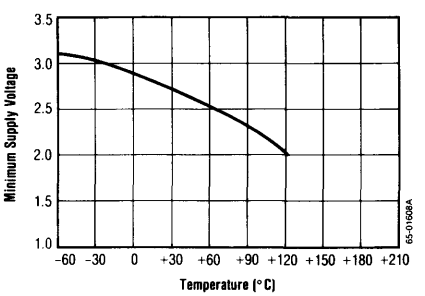
Power vs. Efficiency



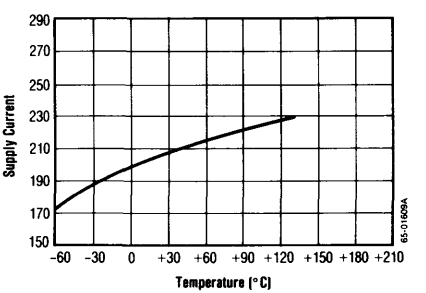
Reference Voltage vs. Temperature



Minimum Supply Voltage vs. Temperature



Supply Current vs. Temperature



Section 12
Special Functions

RC555/556 Timers
Time delay or free running squarewave oscillators with precision accuracy operation.

RC4200 Analog Multiplier
Performs analog computer operations with voltages and currents.

RC4260 Synchronous Detector
Amplifier with phase reversal under control of external logic.

RC4444 Crosspoint Array
SCR matrix for telephone switching applications.

RV4143 Ground Fault Interrupter
Controls a relay in AC outlet safety devices.

XR-2207 Voltage Controlled Oscillator
Frequency programmable sawtooth or squarewave oscillator for FSK generation.

XR-2211 PLL
Phase-locked loop designed for FSK demodulators.

Raytheon

Timer RC555

Features

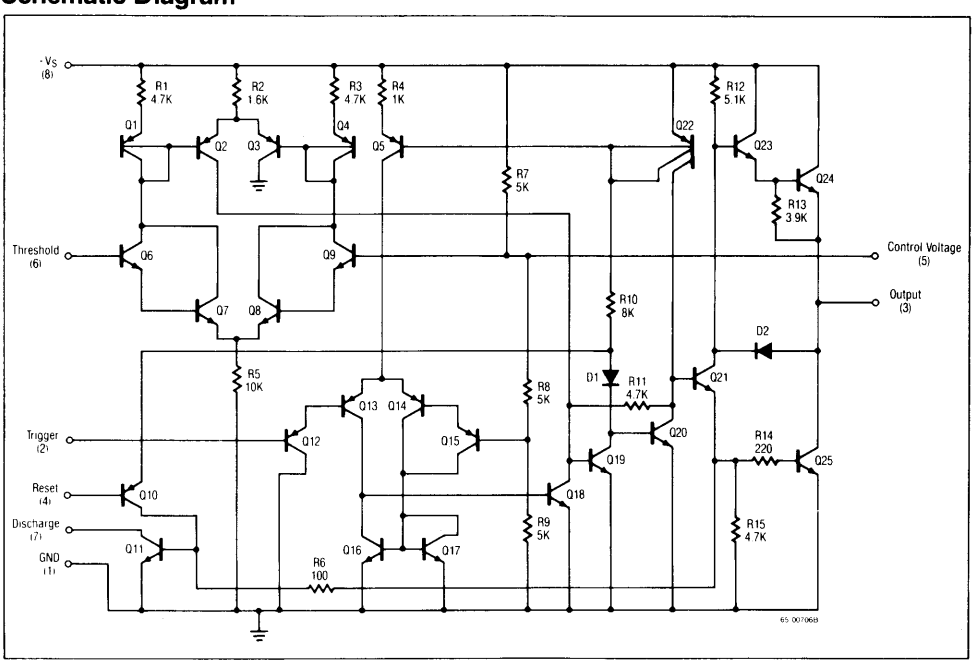
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output drives TTL
- High current output can source or sink 200mA
- Temperature stability of 0.005%/° C
- Normally on and normally off output

Description

The RC/RM555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. In the time delay mode, delay time is precisely controlled by only two external parts: a resistor and a capacitor. For operation as an oscillator, both the free running frequency and the duty cycle are accurately controlled by two external resistors and a capacitor.

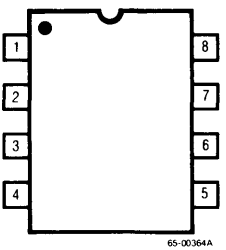
Terminals are provided for triggering and resetting. The circuit will trigger and reset on falling waveforms. The output can source or sink up to 200mA or drive TTL circuits.

Schematic Diagram



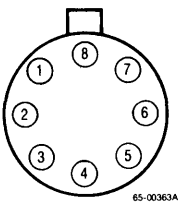
Connection Information

8-Lead
Dual In-Line Package
(Top View)



65-00364A

8-Lead
TO-99 Metal Can
(Top View)



65-00363A

Pin	Function
1	Ground
2	Trigger
3	Output
4	Reset
5	Control Voltage
6	Threshold
7	Discharge
8	$+V_S$

Thermal Characteristics

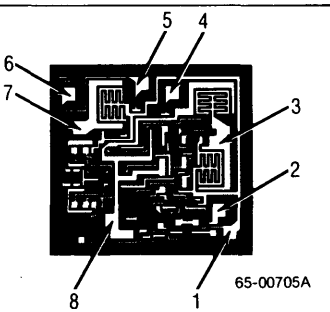
	8-Lead Plastic DIP	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can
Max. Junction Temp.	125°C	175°C	175°C
Max. P_D $T_A < 50°C$	468mW	833mW	658mW
Therm. Res. θ_{JC}	—	45°C/W	50°C/W
Therm. Res. θ_{JA}	160°C/W	150°C/W	190°C/W
For $T_A > 50°C$ Derate at	6.25mW per °C	8.33mW per °C	5.26mW per °C

Ordering Information

Part Number	Package	Operating Temperature Range
RC555DE	Ceramic	0°C to +70°C
RC555NB	Plastic	0°C to +70°C
RC555T	TO-99	0°C to +70°C
RV555NB	Plastic	-40°C to +85°C
RM555DE	Ceramic	-55°C to +125°C
RM555DE/883B*	Ceramic	-55°C to +125°C
RM555T	TO-99	-55°C to +125°C
RM555T/883B*	TO-99	-55°C to +125°C

*MIL-STD-883, Level B Processing

Mask Pattern



65-00705A

Die Size: 56 x 53 mils
Min. Pad Dimensions: 4 x 4 mils

Absolute Maximum Ratings

Supply Voltage ..... +18V
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
RC555 ..... 0°C to +70°C
RV555 ..... -40°C to +85°C
RM555 ..... -55°C to +125°C
Lead Soldering Temperature
(60 Sec) ..... +300°C

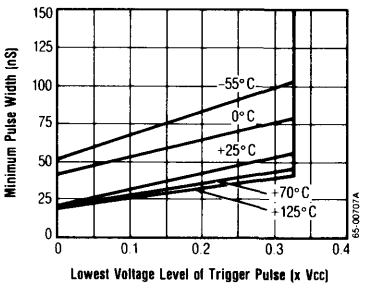
Electrical Characteristics (V_S = +5V to +15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	RM555			RV/RC555			Units
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage		4.5		18	4.5		16	V
Supply Current[1]	V_S = +5V, R_L = ∞		3.0	5.0		4.0	6.0	mA
	V_S = +15V, R_L = ∞ Low State		10	12		10	15	
Timing Error[2] Initial Accuracy	R_A, R_B = 1kΩ to 100kΩ C = 0.1μF		0.5	2.0		1.0		%
V_S Temperature			30	100		50		ppm/°C
V_S Supply Voltage			0.05	0.2		0.1		%/V
Threshold Voltage			2/3			2/3		x V_S
Trigger Voltage	V_S = +15V	4.8	5.0	5.2		5.0		V
	V_S = +5V	1.45	1.67	1.9		1.67		
Trigger Current			0.5			0.5		μA
Reset Voltage		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current			0.1			0.1		mA
Threshold Current[3]			0.1	0.25		0.1	0.25	μA
Control Voltage Level	V_S = +15V	9.6	10	10.4	9.0	10	11	V
	V_S = +5V	2.9	3.33	3.8	2.6	3.33	4.0	
Output Voltage Drop (Low)	V_S = +15V, I_{SINK} = 10mA		0.1	0.15		0.1	0.25	V
	I_{SINK} = 50mA		0.4	0.5		0.4	0.75	
	I_{SINK} = 100mA		2.0	2.2		2.0	2.5	
	I_{SINK} = 200mA		2.5			2.5		
	V_S = +5V, I_{SINK} = 8mA		0.1	0.25				
	I_{SINK} = 5mA					0.25	0.35	
Output Voltage Drop (High)	I_{SOURCE} = 200mA V_S = +15V		12.5			12.5		V
	I_{SOURCE} = 100mA V_S = +15V	13	13.3		12.75	13.3		
	V_S = +5V	3.0	3.3		2.75	3.3		
Rise Time of Output			100			100		nS
Fall Time of Output			100			100		nS

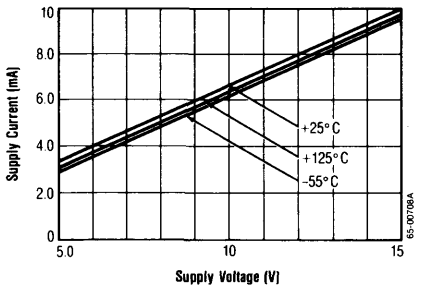
Notes: 1. Supply current when output high typically 1mA less.
2. Tested at V_S = +5V and V_S = +15V.
3. This will determine the maximum value of R_A + R_B. For +15V operation, the maximum total R = 20MΩ.

Typical Performance Characteristics

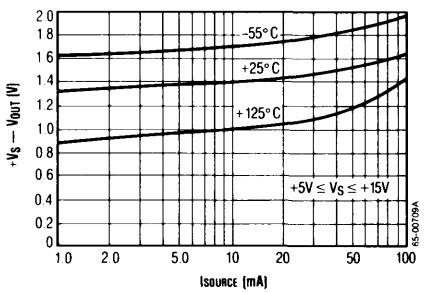
Minimum Pulse Width Required for Triggering



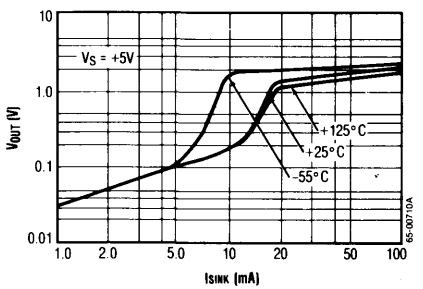
Supply Current vs. Supply Voltage



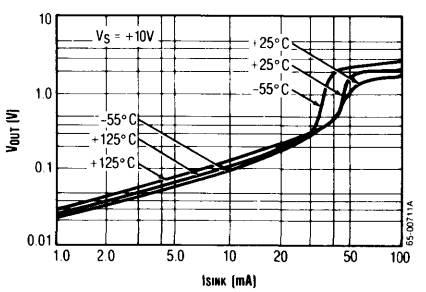
High Output Voltage vs. Output Source Current



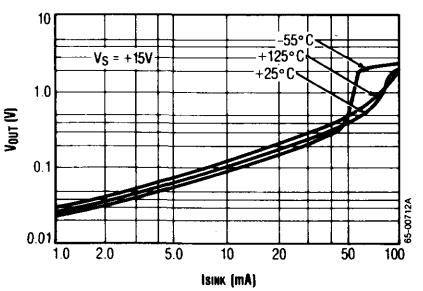
Low Output Voltage vs. Output Sink Current



Low Output Voltage vs. Output Sink Current

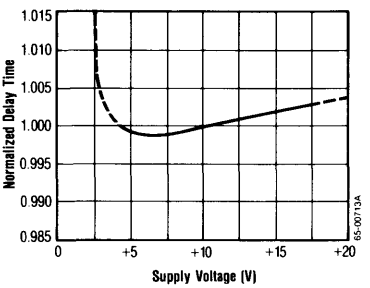


Low Output Voltage vs. Output Sink Current

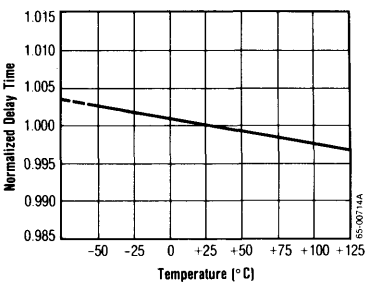


Typical Performance Characteristics (Continued)

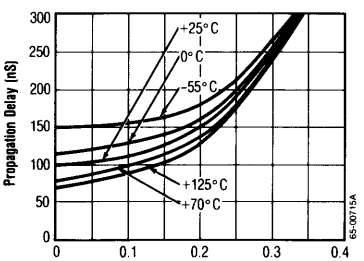
Delay Time vs. Supply Voltage



Delay Time vs. Temperature



Propagation Delay vs. Voltage Level of Trigger Pulse



Typical Applications

Missing Pulse Detector

With the RC/RM555 connected as shown, the timing cycle will be continuously reset by the input pulse train. A change in frequency, or a missing pulse, allows the timing cycle to go to completion and change the output level. For proper operation the time delay should be set slightly longer than the normal time between pulses.

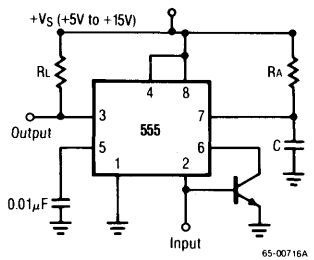
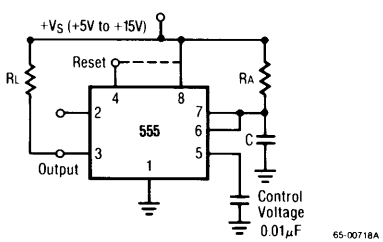


Figure 1. Missing Pulse Detector

Monostable Operation

In this mode, the timer functions as a one-shot. The external capacitor is initially held discharged by a transistor internal to the timer. Applying a negative trigger pulse to Pin 2 sets the flip-flop, driving the output high and releasing the short-circuit across the external capacitor. The voltage across the capacitor increases with time constant $r = R_AC$ to 2/3 V_S, where the comparator resets the flip-flop and discharges the external capacitor. The output is now in the low state.

Circuit triggering takes place when the negative-going trigger pulse reaches 1/3 V_S and the circuit stays in the output high state until the set time elapses. The time the output remains in the high state is $1.1R_AC$ and can be determined by the graph. A negative pulse applied to Pin 4 (reset) during the timing cycle will discharge the external capacitor and start the cycle over again beginning on the positive-going edge of the reset pulse. If reset function is not used, Pin 4 should be connected to V_S to avoid false resetting.



Time Delay vs. R_A, R_B and C

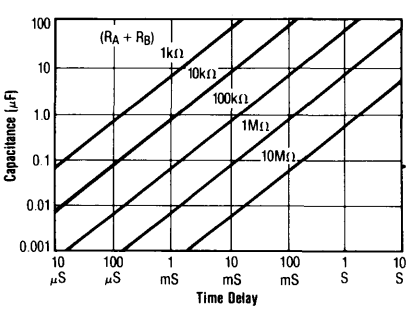
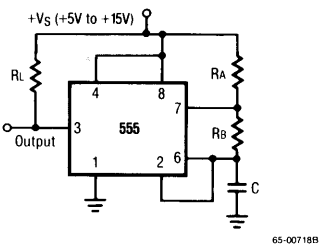


Figure 2. Monostable Operation

Typical Applications (Continued)

Free Running Operation (Astable)

With the circuit connected as shown, it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A and R_B and discharges through R_B only. Thus the duty cycle is set by the ratio of these two resistors, and the capacitor charges and discharges between 1/3 V_S and 2/3 V_S. Charge and discharge times, and therefore frequency, are independent of supply voltage. The free running frequency versus R_A, R_B and C is shown in the graph.



Free Running Frequency vs. R_A, R_B and C

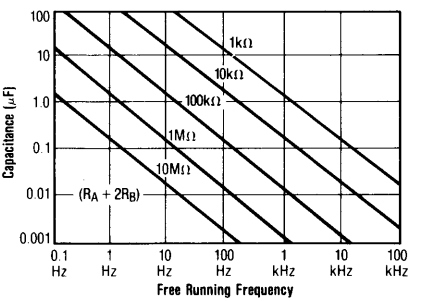


Figure 3. Free Running Operation

Raytheon

Dual Timer RC556

Features

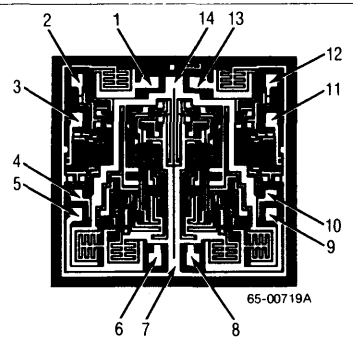
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output drives TTL
- High current output can source or sink 200mA
- Temperature stability of 0.005%/°C
- Normally on and normally off output

Description

The RC556 dual monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. In the time delay mode, delay time is precisely controlled by only two external parts: a resistor and a capacitor. For operation as an oscillator, both the free running frequency and the duty cycle are accurately controlled by two external resistors and a capacitor.

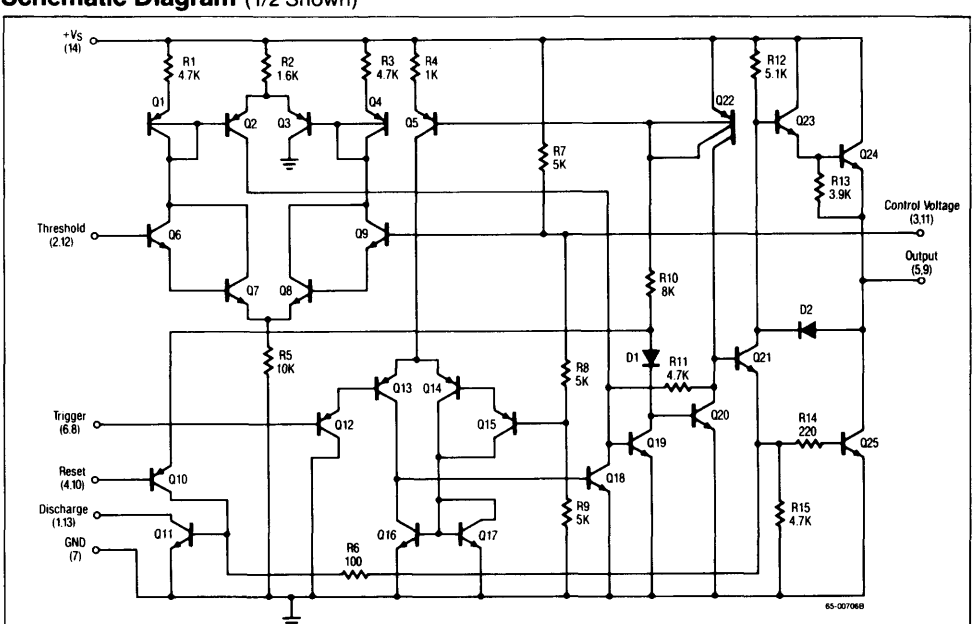
Terminals are provided for triggering and resetting. The circuit will trigger and reset on falling waveforms. The output can source or sink up to 200mA or drive TTL circuits.

Mask Pattern



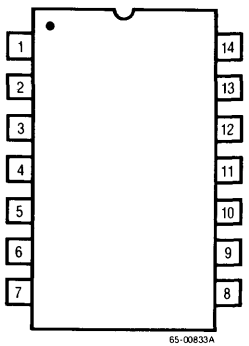
Die Size: 80 x 76 mils
Min. Pad Dimensions: 4 x 4 mils

Schematic Diagram (1/2 Shown)



Connection Information

14-Lead
Dual In-Line Package
(Top View)



Pin	Function
1	Discharge A
2	Threshold A
3	Control A
4	Reset A
5	Output A
6	Trigger A
7	Ground
8	Trigger B
9	Output B
10	Reset B
11	Control B
12	Threshold B
13	Discharge B
14	$+V_S$

Absolute Maximum Ratings

Supply Voltage ..... +18V
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
RC556 ..... 0°C to +70°C
RM556 ..... -55°C to +125°C
RV556 ..... -40°C to +85°C
Lead Soldering Temperature
(60 Sec) ..... +300°C

Thermal Characteristics

	14-Lead Plastic DIP	14-Lead Ceramic DIP
Max. Junction Temp.	125°C	175°C
Max. P_D $T_A < 50°C$	468mW	1042mW
Therm. Res. θ_{JC}	—	60°C/W
Therm. Res. θ_{JA}	160°C/W	120°C/W
For $T_A > 50°C$ Derate at	6.25mW per °C	8.38mW per °C

Ordering Information

Part Number	Package	Operating Temperature Range
RC556DB	Plastic	0°C to +70°C
RC556DC	Ceramic	0°C to +70°C
RV556DB	Plastic	-40°C to +85°C
RM556DC	Ceramic	-55°C to +125°C
RM556DC/883B*	Ceramic	-55°C to +125°C

*MIL-STD-883, Level B Processing

Electrical Characteristics (V_S = +5V to +15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	RM556			RC/RV556			Units
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage		4.5		18	4.5		16	V
Supply Current[1]	V_S = +5V, R_L = ∞		3.0	5.0		4.0	6.0	mA
	V_S = +15V, R_L = ∞ Low State		10	11		10	14	
Timing Error[2] (Free Running) Initial Accuracy	R_A, R_B = 2kΩ to 100kΩ C = 0.1μF		1.5			2.25		%
V_S Temperature			90			150		ppm/°C
V_S Supply Voltage			0.15			0.2		%/V
Timing Error[2] (Monostable) Initial Accuracy	R_A, R_B = 2kΩ to 100kΩ C = 0.1μF		0.5	1.5		0.75		%
V_S Temperature			30	100		50		ppm/°C
V_S Supply Voltage			0.05	0.2		0.1		%/V
Threshold Voltage			2/3			2/3		x V_S
Trigger Voltage	V_S = +15V	4.8	5.0	5.2		5.0		V
	V_S = +5V	1.45	1.67	1.9		1.67		
Trigger Current			0.5			0.5		μA
Reset Voltage		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current			0.1			0.1		mA
Threshold Current[3]			0.03	0.1		0.03	0.1	μA
Control Voltage Level	V_S = +15V	9.6	10	10.4	9.0	10	11	V
	V_S = +5V	2.9	3.33	3.8	2.6	3.33	4.0	
Output Voltage Drop (Low)	V_S = +15V, I_{SINK} = 10mA		0.1	0.15		0.1	0.25	V
	I_{SINK} = 50mA		0.4	0.5		0.4	0.75	
	I_{SINK} = 100mA		2.0	2.25		2.0	2.75	
	I_{SINK} = 200mA		2.5			2.5		
	V_S = +5V, I_{SINK} = 8mA		0.1	0.25				
	I_{SINK} = 5mA					0.25	0.35	

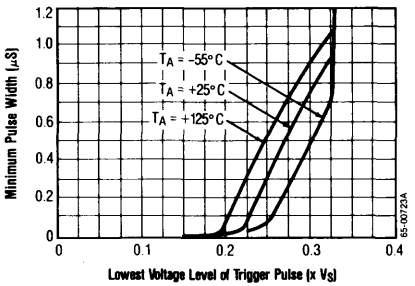
Notes: 1. Supply current when output high typically 2mA less.
2. Tested at V_S = +5V and V_S = +15V.
3. This will determine the maximum value of R_A + R_B. For +15V operation, the maximum total R = 20MΩ.

Electrical Characteristics (Continued) (V_S = +5V to +15V and T_A = +25° C unless otherwise noted)

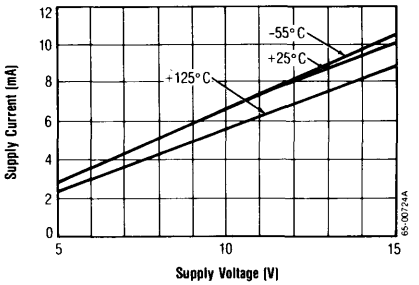
Parameters	Test Conditions	RM556			RC/RV556			Units
		Min	Typ	Max	Min	Typ	Max	
Output Voltage Drop (High)	I_{SOURCE} = 200mA V_S = +15V		12.5			12.5		V
	I_{SOURCE} = 100mA V_S = +15V	13	13.3		12.75	13.3		
	V_S = +5V	3.0	3.3		2.75	3.3		
Rise Time of Output			100			100		nS
Fall Time of Output			100			100		nS
Matching Characteristics Between Each Section Initial Timing Accuracy			0.3	0.6		0.5	1.0	%
V_S Temperature			±10			±10		ppm/°C
V_SSupply Voltage			0.1	0.2		0.2	0.5	%/V

Typical Performance Characteristics

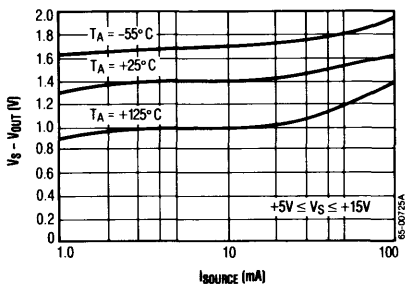
Minimum Pulse Width Required for Triggering



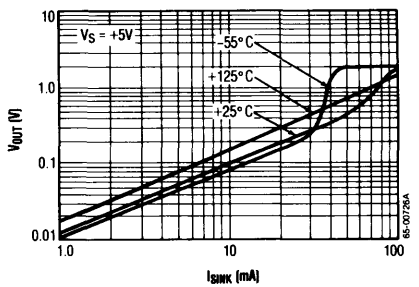
Supply Current vs. Supply Voltage (Each Section)



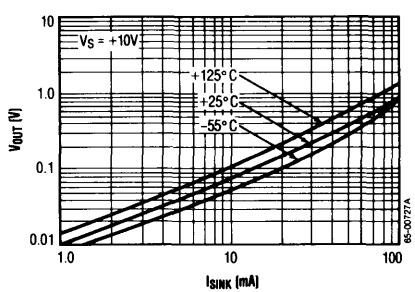
High Output Voltage vs. Output Source Current



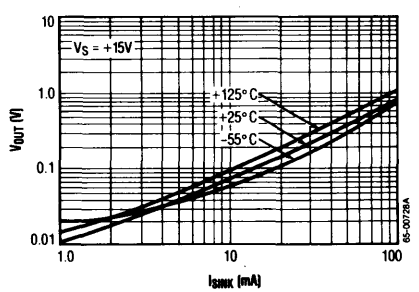
Low Output Voltage vs. Output Sink Current



Low Output Voltage vs. Output Sink Current

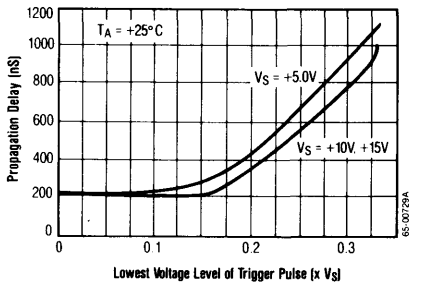


Low Output Voltage vs. Output Sink Current

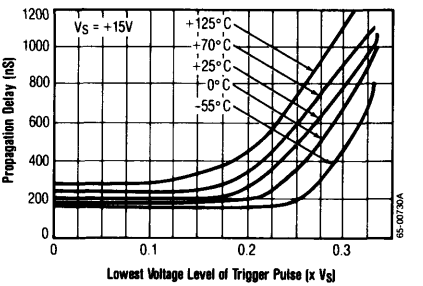


Typical Performance Characteristics (Continued)

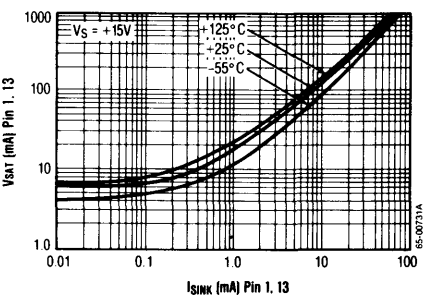
Output Propagation Delay vs. Voltage Level of Trigger Pulse



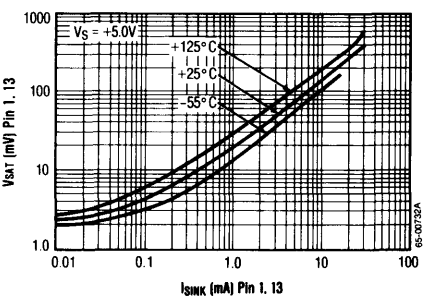
Output Propagation Delay vs. Voltage Level of Trigger Pulse



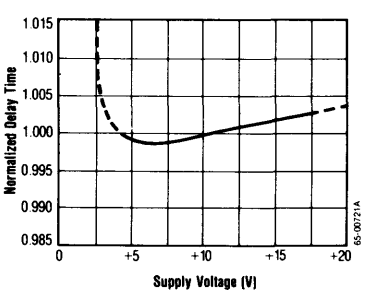
Discharge Transistor (Pin 1, 13) Voltage vs. Sink Current



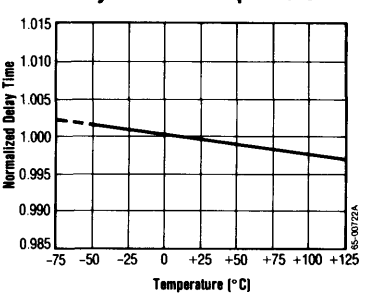
Discharge Transistor (Pin 1, 13) Voltage vs. Sink Current



Delay Time vs. Supply Voltage



Delay Time vs. Temperature



Basic Operational Modes

Monostable Operation

In this mode the timer functions as a one-shot. The external capacitor is initially held discharged by a transistor internal to the timer. Applying a negative trigger pulse to Pin 2 sets the flip-flop, driving the output high and releasing the short-circuit across the external capacitor. The voltage across the capacitor increases with time constant $r = R_AC$ to 2/3 V_S, where the comparator resets the flip-flop and discharges the external capacitor. The output is now in the low state.

Circuit triggering takes place when the negative-going trigger pulse reaches 1/3 V_S and the circuit stays in the output high state until the set time elapses. The time the output remains in the high state is $1.1R_AC$ and can be determined by the graph. A negative pulse applied to Pin 4 (reset) during the timing cycle will discharge the external capacitor and start the cycle over again beginning on the positive-going edge of the reset pulse. If reset function is not used, Pin 4 should be connected to V_S to avoid false resetting.

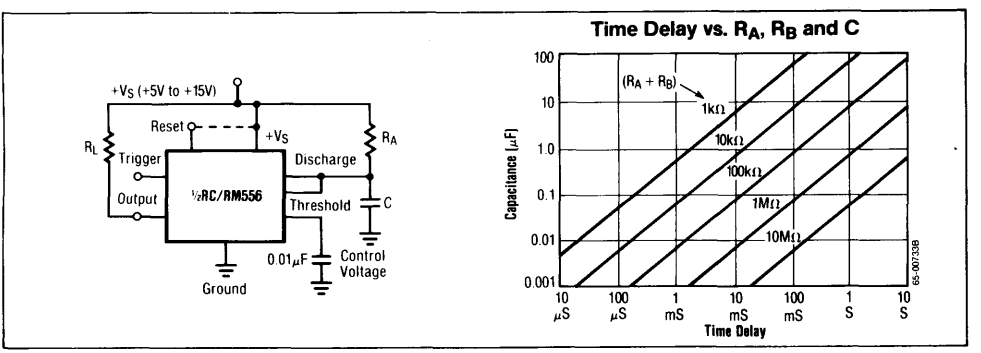


Figure 1. Monostable Operation

Free Running Operation (Astable)

With the circuit connected as shown in Figure 2, it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A and R_B and discharges through R_B only. Thus the duty cycle is set by the ratio of these two resistors, and the capacitor charges and discharges between 1/3 V_S and 2/3 V_S. Charge and discharge times, and therefore frequency, are independent of supply voltage. The free running frequency versus R_A, R_B and C is shown in the graph.

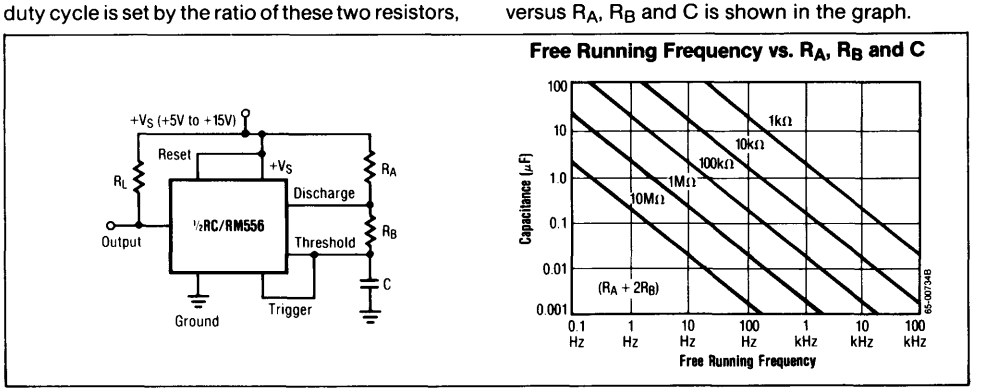


Figure 2. Free Running Operation

Raytheon Analog Multiplier RC4200

Features

- High accuracy
  Non-linearity — 0.1% maximum
  Temperature coefficient — 0.005%/° C maximum
- Multiple functions
  Multiply, divide square, square root, RMS-to-DC conversion, AGC, and modulate/demodulate
- Wide bandwidth — 4MHz
- Signal-to-noise ratio — 94dB

Description

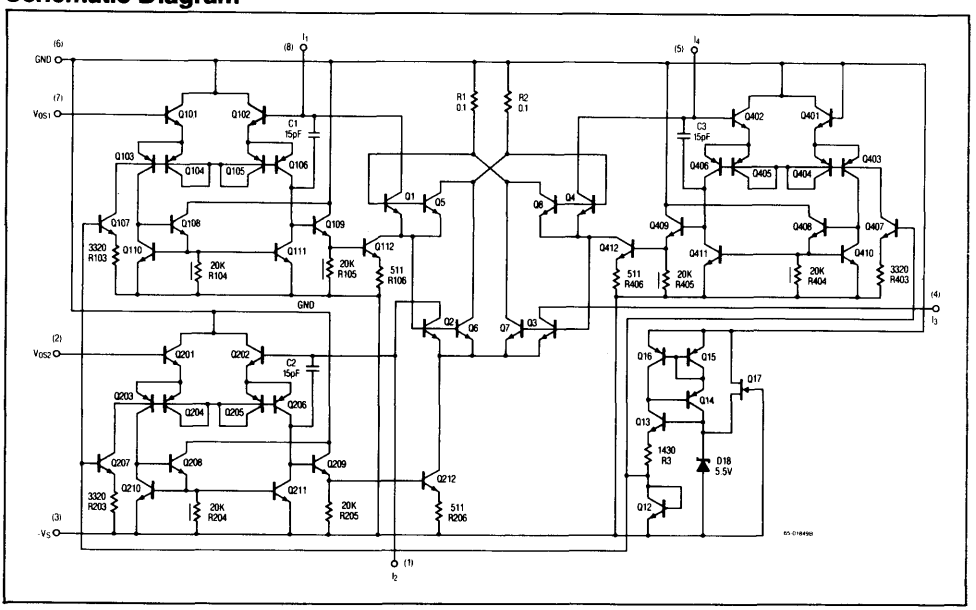
The Raytheon RC4200 is the industry's first integrated circuit multiplier to have complete compensation for nonlinearity, the primary source of error and distortion. This is also the first IC multiplier to have three on-board operational amplifiers designed specifically for use in multiplier logging circuits. These specially designed amplifiers are frequency compensated for optimum AC response in a logging circuit, the heart of a multiplier, and can therefore provide superior AC response in comparison to other analog multipliers.

Versatility is unprecedented; this is the first IC multiplier that can be used in a wide variety of applications without sacrificing accuracy. Four-quadrant multiplication, two-quadrant division, square-rooting, squaring and RMS conversion can all be easily implemented with predictable accuracy. The nonlinearity compensation is not just trimmed at a single temperature, it is designed to provide compensation over the full temperature range. This nonlinearity compensation combined with the low gain and offset drift inherent in a well designed monolithic chip provides a very low accuracy tempco.

The excellent linearity and versatility were achieved through circuit design rather than special grading or trimming, and therefore unit cost is very low. Analog multipliers can now be used in applications where price was previously an inhibiting factor.

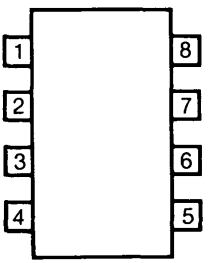
The Raytheon RC4200 is ideal for use in low distortion audio modulation circuits, voltage-controlled active filters, and precision oscillators.

Schematic Diagram



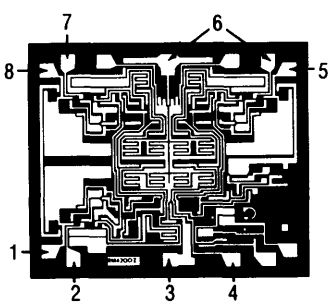
Connection Information

8-Lead
DE and NB
Dual In-Line Package
(Top View)



Pin	Function
1	I_2
2	V_{OS2}
3	$-V_S$
4	I_3 (Output)
5	I_4
6	GND
7	V_{OS1}
8	I_1

Mask Pattern



Die Size: 78 x 66 mils
Min. Pad Dimensions: 4 x 4 mils

Absolute Maximum Ratings

Supply Voltage ..... -22V
Internal Power Dissipation 500mW
Input Current ..... -5mA
Storage Temperature Range
RM4200/4200A ..... -65°C to +150°C
RV4200/4200A ..... -55°C to +125°C
RC4200/4200A ..... -55°C to +125°C
Operating Temperature Range
RM4200/4200A ..... -55°C to +125°C
RV4200/4200A ..... -40°C to +85°C
RC4200/4200A ..... 0°C to +70°C

Thermal Characteristics

	8-Lead Plastic DIP	8-Lead Ceramic DIP
Max. Junction Temp.	125°C	175°C
Max. P_D $T_A < 50°C$	468mW	833mW
Therm. Res. θ_{JC}	—	45°C/W
Therm. Res. θ_{JA}	160°C/W	150°C/W
For $T_A > 50°C$ Derate at	6.25mW per °C	8.33mW per °C

Ordering Information

Part Number	Package	Operating Temperature Range
RC4200DE	Ceramic	0°C to +70°C
RC4200ADE	Ceramic	0°C to +70°C
RC4200NB	Plastic	0°C to +70°C
RC4200ANB	Plastic	0°C to +70°C
RV4200NB	Plastic	-40°C to +85°C
RV4200ANB	Plastic	-40°C to +85°C
RV4200DE	Ceramic	-40°C to +85°C
RV4200ADE	Ceramic	-40°C to +85°C
RM4200DE	Ceramic	-55°C to +125°C
RM4200ADE	Ceramic	-55°C to +125°C

Electrical Characteristics (Over Operating Temperature Range, $V_S = -15V$ unless otherwise noted)

Parameters	Test Conditions	4200A			4200			Units
		Min	Typ	Max	Min	Typ	Max	
Input Current Range (I_1, I_2 and I_4)	(Note 1)	1.0		1000	1.0		1000	μA
Total Error as Multiplier Untrimmed	$T_A = +25°C$			±2.0			±3.0	%
With External Trim	(Note 2)			±0.2			±0.5	%
Versus Temperature			±0.005			±0.005		%/°C
Versus Supply (-9 to -18V)			±0.1			±0.1		%/V
Nonlinearity	$50\mu A \leq I_{1,2,4} \leq 250\mu A$, $T_A = +25°C$			±0.1			±0.3	%
Input Offset Voltage	$I_1 = I_2 = I_4 = 150\mu A$, $T_A = +25°C$			±5.0			±10	mV
Input Bias Current	$I_1 = I_2 = I_4 = 150\mu A$, $T_A = +25°C$			300			500	nA
Average Input Offset Voltage Drift	$I_1 = I_2 = I_4 = 150\mu A$			±50			±100	μV/°C
Output Current Range (I_3)	(Note 3)	1.0		1000	1.0		1000	μA
Frequency Response, -3dB point			4.0			4.0		MHz
Supply Voltage		-18	-15	-9.0	-18	-15	-9.0	V
Supply Current	$I_1 = I_2 = I_4 = 150\mu A$, $T_A = +25°C$			4.0			4.0	mA

Notes:
1. [1]The input circuits tend to become unstable at I_1, I_2, $I_4 < 50\mu A$ and linearity decreases when I_1, I_2, $I_4 > 250\mu A$ (eg. @ $I_1 = I_2 = 500\mu A$, non-linearity error ≈ 0.5%).
2. Refer to Figure 6 for example.
3. These specifications apply with output (I_3) connected to an op amp summing junction. If desired, the output (I_3) at pin 4 can be used to drive a resistive load directly. The resistive load should be less than 700Ω and must be pulled up to a positive supply such that the voltage on pin 4 stays within a range of 0 to +5V.

Functional Description

The RC4200 multiplier is designed to multiply two input currents (I_1 and I_2) and to divide by a third input current (I_4). The output is also in the form of a current (I_3). A simplified circuit diagram is shown in Figure 1. The nominal relationship between the three inputs and the output is:

$$I_3 = \frac{I_1 I_2}{I_4} \qquad (1)$$

The three input currents must be positive and restricted to a range of 1μA to 1mA. These currents go into the multiplier chip at op-amp summing junctions which are nominally at zero volts. Therefore, an input voltage can be easily converted to an input current by a series resistor. Any number of currents may be summed at the inputs. Depending on the application, the output current can be converted to a voltage by an external op amp or used directly. This capability of combining input currents and voltages in various combinations provides great versatility in application.

Inside the multiplier chip, the three op amps make the collector currents of transistors Q1, Q2, and Q4 equal to their respective input currents (I_1, I_2, and I_4). These op amps are designed with current-source outputs and are phase-compensated for optimum frequency response as a multiplier. Power drain of the op amps was minimized to prevent the introduction of undesired thermal gradients on the chip. The three op amps operate on a single supply voltage (nominally -15V) and total quiescent current drain is less than 4mA. These special op amps provide significantly improved performance in comparison to 741-type op amps.

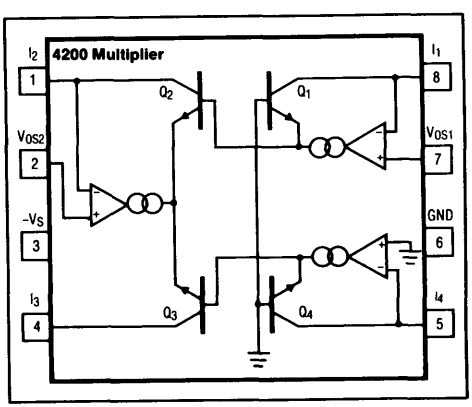


Figure 1. Functional Diagram

The actual multiplication is done within the log-antilog configuration of the Q1-Q4 transistor array. These four transistors, with associated proprietary circuitry, were specially designed to precisely implement the relationship

$$V_{BEN} = \frac{kT}{q} \ln \frac{I_{CN}}{I_{SN}} \qquad (2)$$

Previous multiplier designs have suffered from an additional undesired linear term in the above equation; the collector current times the emitter resistance. This $I_C r_E$ term introduces a parabolic nonlinearity even with matched transistors. Raytheon has developed a unique and proprietary means of inherently compensating for this undesired $I_C r_E$ term. Furthermore, this Raytheon-developed circuit technique compensates linearity error over temperature changes. The nonlinearity versus temperature is significantly improved over earlier designs.

From equation (2) and by assuming equal transistor junction temperatures, summing base-to-emitter voltage drops around the transistor array yields:

$$\frac{kT}{q}\left[\ln \frac{I_1}{I_{S1}} = \ln \frac{I_2}{I_{S2}} - \ln \frac{I_3}{I_{S3}} - \ln \frac{I_4}{I_{S4}}\right] = 0 \qquad (3)$$

This equation reduces to:

$$\frac{I_1 I_2}{I_3 I_4} = \frac{I_{S1} I_{S2}}{I_{S3} I_{S4}} \qquad (4)$$

The ratio of reverse saturation currents, $I_{S1}I_{S2}/I_{S3}I_{S4}$, depends on the transistor matching. In a monolithic multiplier this matching is easily achieved and the ratio is very close to unity, typically 1.0 ±1%. The final result is the desired relationship:

$$I_3 = \frac{I_1 I_1}{I_4} \quad (5)$$

The inherent linearity and gain stability combined with low cost and versatility makes this new circuit ideal for a wide range of nonlinear functions.

Basic Circuits

Current Multiplier/Divider

The basic design criteria for all circuit configurations using the 4200 multiplier is contained in equation (1):

$$\text{i.e.} \qquad I_3 = \frac{I_1 I_2}{I_4}$$

The current-product-balance equation restates this as:

$$I_1 I_2 = I_3 I_4 \quad (6)$$

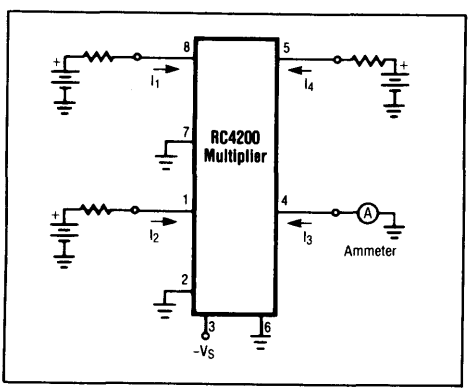
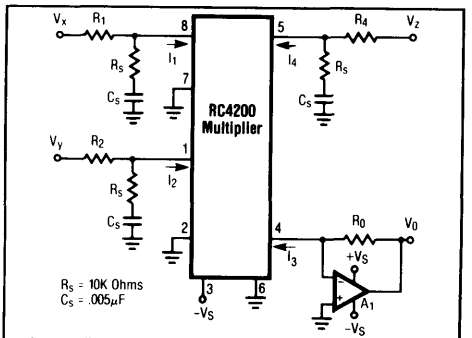


Figure 2

Dynamic Range and Stability

The precision dynamic range for the 4200 is from +50μA to +250μA inputs for I_1, I_2 and I_4. Stability and accuracy degrade if this range is exceeded.

To improve the stability for input currents less than 50μA, filter circuits ($R_S C_S$) are added to each input (see Figure 3).



Amplifier A_1 is used to convert the I_3 current to an output voltage.
Multiplier: V_z = constant ≠ 0
Divider: V_y = constant ≠ 0

Figure 3

Voltage Multiplier/Divider

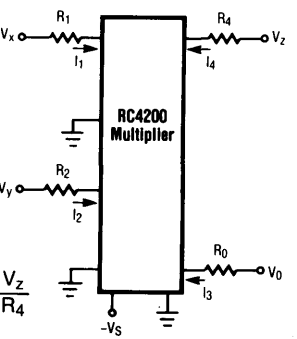
$$I_1 = \frac{V_x}{R_1}$$

$$I_2 = \frac{V_y}{R_2}$$

$$I_3 = \frac{V_0}{R_0}$$

$$I_4 = \frac{V_z}{R_4}$$

$$\frac{V_x}{R_1}\frac{V_y}{R_2} = \frac{V_0}{R_0}\frac{V_z}{R_4}$$



Solving for V_0: $V_0 = \frac{V_x V_y}{V_z}\frac{R_0 R_4}{R_1 R_2}$

For a multiplier circuit $V_z = V_R$ = constant

Therefore: $V_0 = \frac{V_x}{V_z} K$ where $K = \frac{V_R R_0 R_4}{R_1 R_2}$

For a divider circuit $V_y = V_{REF}$ = constant

Therefore: $V_0 = V_x V_y K$ where $K = \frac{R_0 R_4}{V_R R_1 R_2}$

Figure 4

Extended Range

The input and output voltage ranges can be extended to include 0 and negative voltage signals by adding bias currents. The R_SC_S filter circuits are eliminated when the input and biasing resistors are selected to limit the respective currents to 50μA min. and 250μA max.

Extended Range Multiplier

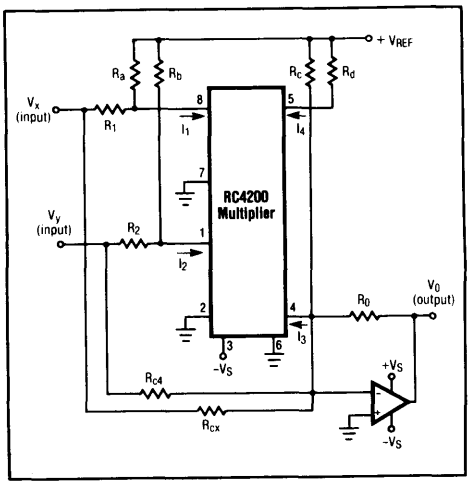


Figure 5

Resistors R_a and R_b extend the range of the V_x and V_y inputs by picking values such that:

$$I_1(\text{min.}) = \frac{V_x(\text{min.})}{R_1} + \frac{V_{REF}}{R_a} = 50\mu A,$$

$$\text{and } I_1(\text{max.}) = \frac{V_x(\text{max.})}{R_1} + \frac{V_{REF}}{R_a} = 250\mu A;$$

$$\text{also } I_2(\text{min.}) = \frac{V_y(\text{min.})}{R_2} + \frac{V_{REF}}{R_b} = 50\mu A,$$

$$\text{and } I_2(\text{max.}) = \frac{V_y(\text{max.})}{R_2} + \frac{V_{REF}}{R_b} = 250\mu A.$$

Resistor R_c supplies bias current for I_3 which allows the output to go negative.

Resistors R_{cx} and R_{cy} permit equation (6) to balance, i.e.:

$$\left(\frac{V_x}{R_1} + \frac{V_{REF}}{R_a}\right)+\left(\frac{V_y}{R_2} = \frac{V_{REF}}{R_b}\right) = \left(\frac{V_0}{R_0} + \frac{V_{REF}}{R_c} + \frac{V_x}{R_{cx}} + \frac{V_y}{R_{cy}}\right)\left(\frac{V_{REF}}{R_d}\right)$$

$$\frac{V_xV_y}{R_1R_2} + \frac{V_xV_{REF}}{R_1R_b} + \frac{V_yV_{REF}}{R_2R_a} + \frac{V_{REF}^2}{R_aR_b} =$$

$$\frac{V_0V_{REF}}{R_0R_d} + \frac{V_xV_{REF}}{R_{cx}R_d} + \frac{V_yV_{REF}}{R_{cy}R_d} + \frac{V_{REF}^2}{R_cR_d}$$

Cross-Product Cancellation

Cross-products are a result of the V_xV_{REF} and V_yV_{REF} terms. To the extent that:

$$R_1R_b = R_{cx}R_d \text{ and } R_2R_a = R_{cy}R_d,$$

cross-product cancellation will occur.

Arithmetic Offset Cancellation

The offset caused by the V_{REF}^2 term will cancel to the extent that: $R_aR_b = R_cR_d$, and the result is:

$$\frac{V_xV_y}{R_1R_2} = \frac{V_0V_{REF}}{R_0R_d} \quad \text{or } V_0 = V_xV_y\,K$$

$$\text{where } K = \frac{R_0R_d}{V_{REF}R_1R_2}$$

Resistor Values

Inputs:

$$V_x(\text{min.}) \le V_x \le V_x(\text{max.})$$

$$\Delta V_x = V_x(\text{max.}) - V_x(\text{min.})$$

$$V_y(\text{min.}) \le V_y \le V_y(\text{max.})$$

$$\Delta V_y = V_y(\text{max.}) - V_y(\text{min.})$$

$$V_{REF} = \text{Constant (+7V to +18V)}$$

$$K = \frac{V_0}{V_xV_y} \text{ (Design Requirement)}$$

$$R_1 = \frac{\Delta V_x}{200\mu A},\ R_2 = \frac{\Delta V_y}{200\mu A},\ R_d = \frac{V_{REF}}{250\mu A}$$

$$R_a = \frac{\Delta V_xV_{REF}}{250\mu A\ \Delta V_x - 200\mu A\ V_x(\text{max.})}$$

$$R_b = \frac{\Delta V_yV_{REF}}{250\mu A\ \Delta V_y - 200\mu A\ V_y(\text{max.})}$$

$$R_c = \frac{R_aR_b}{R_d},\ R_{cx} = \frac{R_1R_b}{R_d},\ R_{cy} = \frac{R_2R_a}{R_d}$$

$$R_0 = \frac{\Delta V_x\ \Delta V_y\ K}{160\mu A}$$

Multiplying Circuit Offset Adjust

$$10K \leq R_5 = R_9 = R_{16} \leq 50K$$

$$R_7 = R_{11} = R_{14} = 100\Omega$$

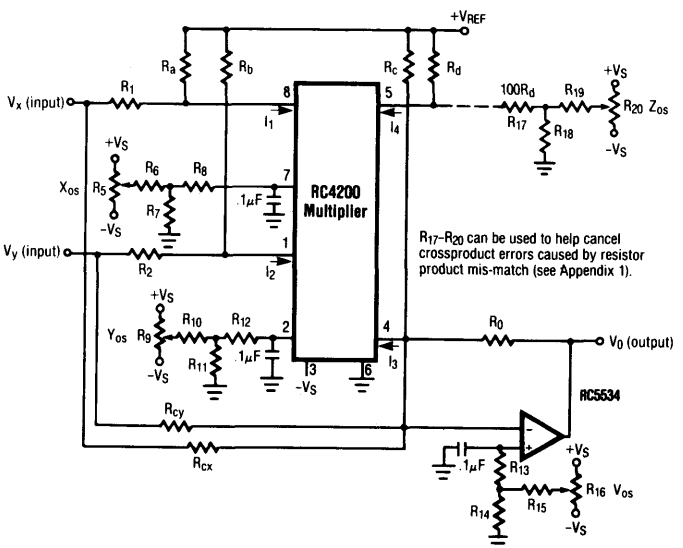
$$R_6 = R_{10} = 100\Omega \frac{V_S}{.05}$$

$$R_{14} = 100\Omega \frac{V_S}{.10}$$

$$R_8 = R_1 || R_a$$

$$R_{12} = R_2 || R_b$$

$$R_{13} = R_0 || R_c || R_{cx} || R_{cy}$$



Procedure:

1. Set all trimmer pots to 0V on the wiper.
2. Connect V_x input to ground. Put in a full scale square wave on V_y input. Adjust $X_{OS}(R_5)$ for no square wave on V_0 output (adjust for 0 feedthrough).
3. Connect V_y input to ground. Put in a full scale square wave on V_x input. Adjust $Y_{OS}(R_9)$ for no square wave on V_0 output (adjust for 0 feedthrough).
4. Connect V_x and V_y to ground. Adjust $V_{OS}(R_{16})$ for 0V on V_0 output.

Figure 6

Extended Range Divider

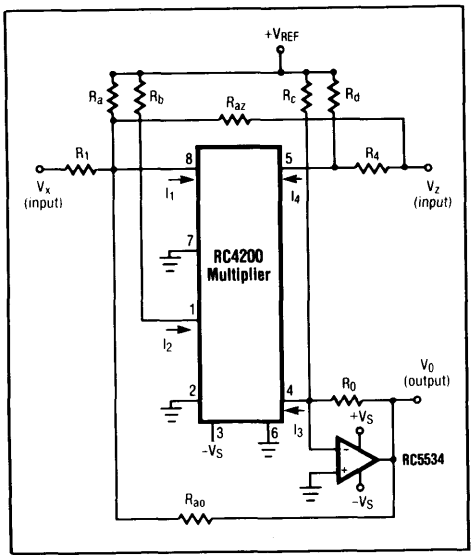


Figure 7

As with the extended range multiplier, resistors R_{az} and R_{ao} are added to cancel the cross-product error caused by the biasing resistors, i.e.,

$$\left(\frac{V_x}{R_1}+\frac{V_0}{R_{ao}}+\frac{V_z}{R_{az}}+\frac{V_{REF}}{R_a}\right)\left(\frac{V_{REF}}{R_b}\right)=\left(\frac{V_0}{R_0}+\frac{V_{REF}}{R_c}\right)\left(\frac{V_z}{R_4}+\frac{V_{REF}}{R_d}\right)$$

$$\frac{V_xV_{REF}}{R_1R_b}+\frac{V_0V_{REF}}{R_{ao}R_b}+\frac{V_zV_{REF}}{R_{az}R_b}+\frac{V_{REF}^2}{R_aR_b}=\frac{V_0V_z}{R_0R_4}+\frac{V_0V_{REF}}{R_0R_d}+\frac{V_zV_{REF}}{R_4R_c}+\frac{V_{REF}^2}{R_cR_d}$$

To cancel cross-product and arithmetic offset:

$R_{ao}R_b = R_0R_d$, $R_{az}R_b = R_4R_c$ and $R_aR_b = R_cR_d$

and the result is:

$$\frac{V_xV_{REF}}{R_1R_b}=\frac{V_0V_z}{R_0R_4} \quad \text{or } V_0 = V_x/V_y\,K$$

$$\text{where } K=\frac{V_{REF}R_0R_4}{R_1R_b}$$

NOTE: It is necessary to match the resistor cross-products above to within the amount of error tolerable in the output offset, i.e., with a 10V F.S. output, 0.1% resistor cross-product match will give 0.1% x 10V = 10mV untrimmable output offset voltage.

Resistor Values

Inputs:

$$V_x(\text{min.}) \le V_x \le V_x(\text{max.})$$

$$\Delta V_x = V_x(\text{max.}) - V_x(\text{min.})$$

$$V_z(\text{min.}) \le V_z \le V_z(\text{max.})$$

$$\Delta V_z = V_z(\text{max.}) - V_z(\text{min.})$$

$$V_{REF} = \text{Constant (+7V to +18V)}$$

Outputs:

$$V_0(\text{min.}) \le V_0 \le V_0(\text{max.})$$

$$\Delta V_0 = V_0(\text{max.}) - V_0(\text{min.})$$

$$K=\frac{V_0V_z}{V_x}\ \text{(Design Requirement)}$$

$$R_0=\frac{\Delta V_0}{750\mu A},\ R_b=\frac{V_{REF}}{250\mu A},\ R_4=\frac{\Delta V_z}{200\mu A}$$

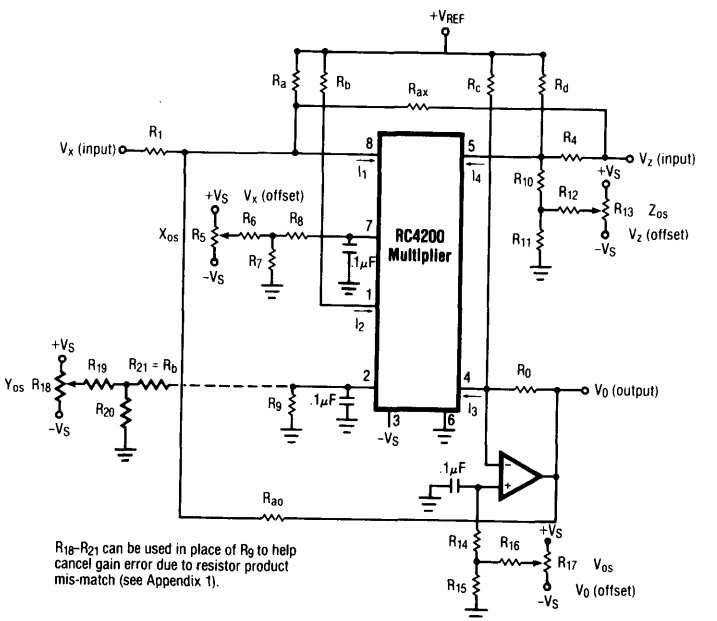
$$R_c=\frac{\Delta V_0 V_{REF}}{750\mu A\ \Delta V_0 - 700\mu A\ V_0(\text{max.})}$$

$$R_d=\frac{\Delta V_z V_{REF}}{250\mu A\ \Delta V_z - 200\mu A\ V_z(\text{max.})}$$

$$R_a=\frac{R_cR_d}{R_b},\ R_{az}=\frac{R_cR_4}{R_b},\ R_{ao}=\frac{R_0R_d}{R_b}$$

$$R_1=\frac{\Delta V_0\ \Delta V_z}{600\mu AK}$$

Divider Circuit with Offset Adjustment



R_{18}–R_{21} can be used in place of R_9 to help cancel gain error due to resistor product mis-match (see Appendix 1).

General

$10K \leq R_5 = R_{13} = R_{17} \leq 50K$

$R_7 + R_8 \approx R_1 || R_a || R_{az} || R_{ao}$

$R_6 \approx \frac{V_S}{.05} R_7$

$R_9 = R_b$

$R_{10} \approx 100 \times R_4$

$R_{11} = 20K$

$R_{12} = 100K$

$R_{14} + R_{15} \approx R_o || R_c$

$R_{16} \approx \frac{V_S}{.10} R_{15}$

Example: Two-Quad Divider

$V_0 = K \frac{V_x}{V_z}$, K = k, $V_{REF} = +V_S = +15V$

$-10 \leq V_x \leq +10$, therefore $\Delta V_x = 20$
$0 \leq V_z \leq +10$, therefore $\Delta V_z = 10$
$-10 \leq V_0 \leq +10$, therefore $\Delta V_0 = 20$

$R_0 = 26.7K$
$R_b = 60K$
$R_4 = 50K$
$R_c = 37.5K$
$R_d = 300K$
$R_a = 187.5K$
$R_{az} = 31.25K$
$R_{ao} = 133K$

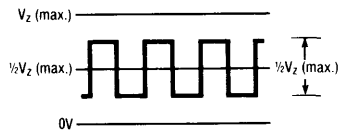
$R_1 = 333K$
$R_5, R_{13}, R_{17} = 10K$
$R_7, R_{15} = 1K$
$R_8, R_{11} = 20K$
$R_6, R_9, R_{16} = 300K$
$R_{10} = 4.7M$
$R_{12} = 100K$

Figure 8

Divider Circuit Offset Adjustment Procedure

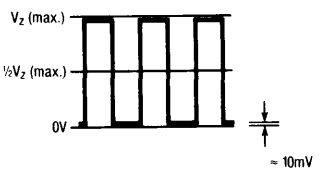
1. Set each trimmer pot to 0V on the wiper.

2. Connect V_X (input) to ground. Put a DC voltage of approximately ½V_Z (max.) DC on the V_Z (input) with an AC (squarewave is easiest) voltage of ½V_Z (max.) peak-to-peak superimposed on it. Adjust $X_{OS}(R_5)$ for zero feedthrough. (No AC at V_O)



3. Connect V_X (input to V_Z (input) and put in the ½V_Z (max.) DC with an AC of approximately 20mV less than V_Z (max.).

   Adjust $Z_{OS}(R_{13})$ for zero feedthrough.

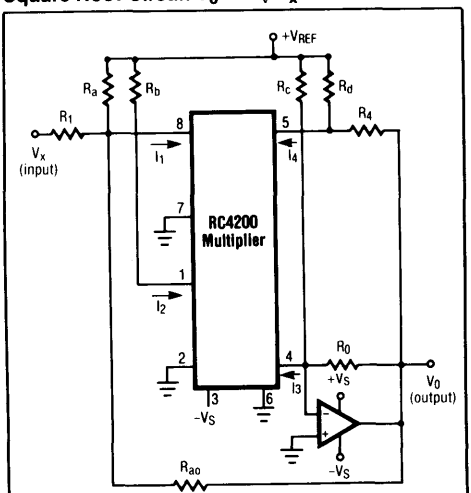


4. Return V_X (input) to ground and connect V_Z (max.) DC on V_Z (input). Adjust output $V_{OS}(R_{17})$ for V_O =

5. Connect V_X (input) to V_Z (input) and put in V_Z (max.) DC. (The output will equal K.) Decrease the input slowly until the output (V_O = K) deviates beyond the desired accuracy. Adjust Z_{OS} to bring it back into tolerance and return to Step 4. Continue Steps 4 and 5 until V_Z reduces to the lowest value desired.

NOTE: As the input to V_X and V_Z gets closer to zero (an illegal state) the system noise will predominate so much that an integrating voltmeter will be very helpful.

Square Root Circuit $V_O = N\sqrt{V_X}$



$$\frac{V_X V_{REF}}{R_1 R_b} + \frac{V_{REF}^2}{R_a R_b} + \frac{V_O V_{REF}}{R_{ao} R_b} = \frac{V_O^2}{R_O R_4} + \frac{V_O V_{REF}}{R_c R_4} + \frac{V_O V_{REF}}{R_O R_d} + \frac{V_{REF}^2}{R_c R_d}$$

If $R_a R_b = R_c R_d$ and $R_{ao} R_b R_O R_d + R_{ao} R_b R_c R_4 = R_c R_d R_O R_4$

Then $\frac{V_O^2}{R_O R_4} = \frac{V_X V_{REF}}{R_1 R_b}$ or $V_O = V_X K$ where $K = \frac{V_{REF} R_O R_4}{R_1 R_b}$

and $V_O = N\sqrt{V_X}$ where $N = \sqrt{K}$

$0 \le V_X \le V_X$ (max) and V_O (max) $= N\sqrt{V_X}$ (max)

$$N = \frac{V_O}{\sqrt{V_X}} \text{ (Design Requirement)}$$

$$R_1 = \frac{V_O(max)^2}{75\mu A\, N^2}$$

$$R_a = R_d = \frac{V_{REF}}{50\mu A}$$

$$R_b = R_c = \frac{V_{REF}}{150\mu A}$$

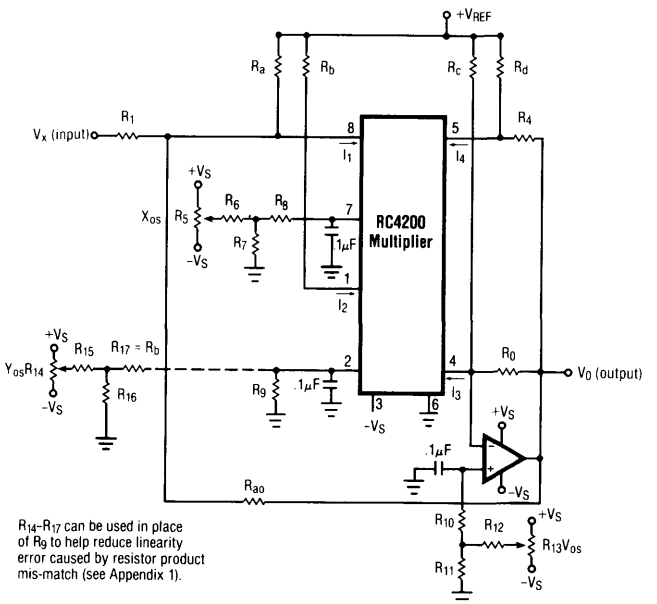
$$R_4 = \frac{V_O(max)}{50\mu A}$$

$$R_{ao} = \frac{V_O(max)}{125\mu A}$$

$$R_O = \frac{V_O(max)}{225\mu A}$$

Figure 9

Square Root Circuit Offset Adjust



$$10K \leq R_5 = R_{13} \leq 50K$$

$$R_7 = 100\Omega$$

$$R_6 = R_7 \frac{V_S}{.05}$$

$$R_8 = R_1 || R_a || R_{ao}$$

$$R_9 = R_b$$

$$R_{10} = R_0 || R_c$$

$$R_{11} = 100\Omega$$

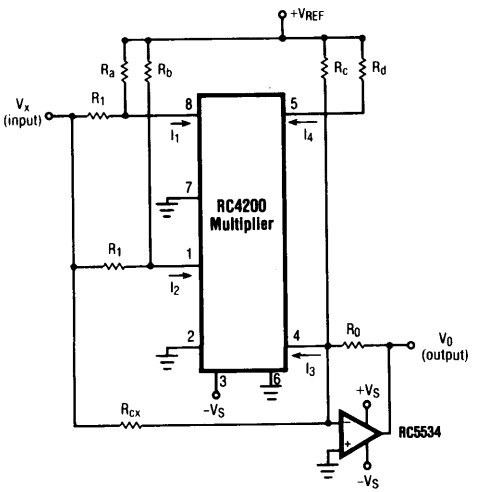
$$R_{12} = R_{11} \frac{V_S}{.1}$$

Procedure

1. Set both trimmer pots to 0V on the wiper.
2. Put in a full scale (0 to V_x(max.)) squarewave on V_x input. Adjust $X_{ox}(R_5)$ for proper peak-to-peak amplitude on V_0 output. (Scaling adjust)
3. Connect V_x input to ground. Adjust $V_{os}(R_{13})$ for 0V on V_0 output.

Figure 10

Squaring Circuits $V_0 = K V_x^2$



$$\frac{V_x^2}{R_1^2} + \frac{2V_xV_{REF}}{R_1R_a} + \frac{V_{REF}^2}{R_a^2} = \frac{V_0V_{REF}}{R_0R_d} + \frac{V_{REF}^2}{R_cR_d} + \frac{V_xV_{REF}}{R_{cx}R_d}$$

if $R_a^2 = R_cR_d$ and $R_1R_a = 2R_{cx}R_d$

then $\frac{V_0V_{REF}}{R_0R_d} = \frac{V_x^2}{R_1^2}$ or $V_0 = KV_x^2$ where $K = \frac{R_0R_d}{V_{REF}R_1^2}$

$V_x(min.) \leq V_x \leq V_x(max.)$ $\quad \Delta V_x = V_x(max.) - V_x(min.)$

$$K = \frac{V_0}{V_x^2} \text{ (Design Requirement)}$$

$$R_1 = \frac{\Delta V_x}{200\mu A}$$

$$R_a = \frac{\Delta V_x V_{REF}}{250\mu A\, \Delta V_x - 200\mu A\, V_x(max.)}$$

$$R_d = \frac{V_{REF}}{250\mu A}$$

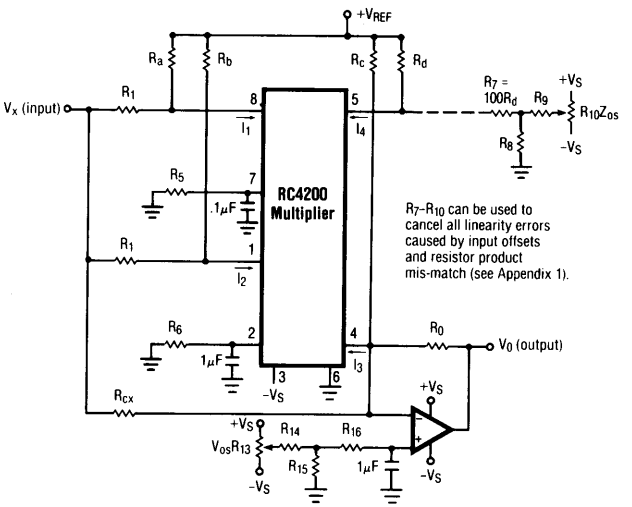
$$R_c = \frac{R_a^2}{R_d}$$

$$R_{cx} = \frac{R_1R_a}{2R_d}$$

$$R_0 = \frac{\Delta V_x^2 K}{160\mu A}$$

Figure 11

Squaring Circuits Offset Adjust



$$10K \leq R_{10}, R_{11} \leq 50K$$

$$R_8, R_{15} = 100\Omega$$

$$R_9, R_{14} = 100\Omega \frac{V_S}{.1}$$

$$R_5, R_6 = R_1 || R_a$$

$$R_{16} = R_0 || R_c || R_{cx}$$

Procedure

1. Set both trimmer pots to 0V on the wiper.
2. Put in a full scale ($\pm V_x$) squarewave on V_x input. Adjust $Z_{os}(R_{10})$ for uniform output.
3. Connect V_x input to ground. Adjust $V_{os}(R_{11})$ for 0V on V_0 output.

Figure 12

Appendix 1 — System Errors

There are four types of accuracy errors which effect overall system performance. They are:

1. Nonlinearity — Incremental deviation from absolute accuracy.(1)
2. Scaling Error — Linear deviation from absolute accuracy.
3. Output Offset — Constant deviation from absolute accuracy.
4. Feedthrough(2) — Crossproduct errors caused by input offsets and external circuit limitations.

The nonlinearity error in the transfer function of the 4200 is ±0.1% max. (±0.03% max. for 4200A).

$$\text{i.e., } I_3 = \frac{I_1 I_2}{I_4} \pm 0.1\% \text{ F.S.}(4)$$

The other system errors are caused by voltage offsets on the inputs of the 4200 and can be as high as ±3.0% (±2.0% for 4200A).

$$\text{i.e., } V_O = \frac{V_X V_Y}{V_Z}\frac{R_O R_4}{R_1 R_2} \pm 3.0\% \text{ F.S.}(3)(4)$$

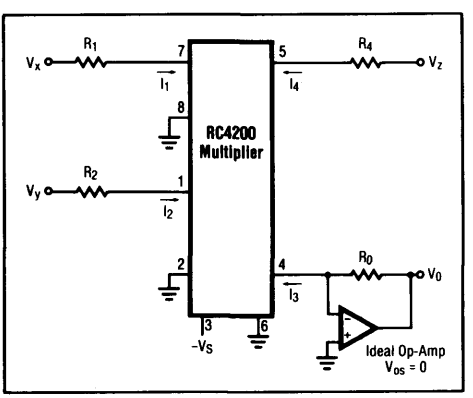


Figure 13

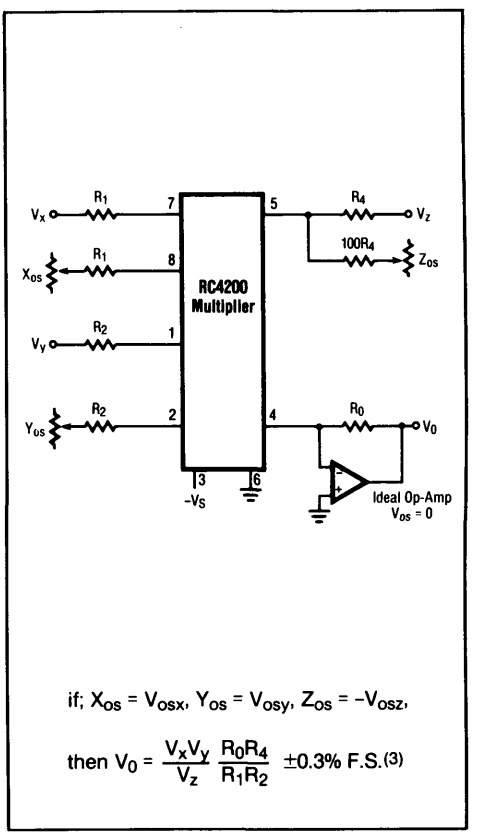
Notes: 1. The input circuits tend to become unstable at $I_1, I_2, I_4 < 50\mu A$ and linearity decreases when $I_1, I_2, I_4 > 250\mu A$ (e.g., @ $I_1 = I_2 = 500\mu A$ nonlinearity error ≈ 0.5%).
2. This section will not deal with feedthrough which is proportional to frequency of operation and caused by stray capacitance and/or bandwidth limitations. (Refer to Figure 21.)
3. Not including resistor tolerance or output offset on the op amp.
4. For $50\mu A \le I_1, I_2, I_4 \le 250\mu A$.

Errors caused by input offsets.

$$V_O = \frac{R_O R_4}{R_1 R_2}\left[\frac{V_X V_Y}{V_Z} \pm \frac{1}{V_Z} V_Y V_{OSX} \pm V_X V_{OSY} \pm V_O V_{OSZ} \pm V_{OSX} V_{OSY}\right]$$

V_Y Feedthrough
V_X Feedthrough
Scaling Error
Output Offset Error

Systems errors can be greatly reduced by ex ternally trimming the input offset voltages of the 4200. (±0.3% F.S. for 4200 and ±0.1% F.S. for 4200A.)



if; $X_{OS} = V_{OSX}$, $Y_{OS} = V_{OSY}$, $Z_{OS} = -V_{OSZ}$,

$$\text{then } V_O = \frac{V_X V_Y}{V_Z}\frac{R_O R_4}{R_1 R_2} \pm 0.3\% \text{ F.S.}(3)$$

Figure 14. 4200 With Input Offset Adjustment

Extended Range Circuit Errors

The extended range configurations have a disadvantage in that additional accuracy errors may be introduced by resistor product mis-matching.

Multiplier (Figure 6)

An error in resistor product matching will cause an equivalent feedthrough or output offset error:

1. $R_1R_b = R_{cx}R_d \pm \alpha$,
   V_x feedthrough ($V_y = 0$) = $\pm\alpha V_x$
2. $R_2R_a = R_{cy}R_d \pm \beta$,
   V_y feedthrough ($V_x = 0$) = $\pm\beta V_y$
3. $R_aR_b = R_cR_d \pm \gamma$,
   V_0 offset ($V_x = V_y = 0$) = $\pm\gamma V_{REF}$*

*Output offset errors can always be trimmed out with the output op amp offset adjust, $V_{os}(R_{16})$.

Reducing Mis-Match Errors

You need not run out and buy .01% resistors to reduce resistor product mis-match errors. Here are a couple of ways to squeeze maximum accuracy out of the extended range multiplier (Figure 6) using 1% resistors.

Method #1

V_x feedthrough, for example, occurs when $V_y = 0$ and $V_{osy} \neq 0$. This V_x feedthrough will equal $\pm V_xV_{osy}$. Also, if $V_{osz} \neq 0$, there is a V_x feedthrough equal to $\pm V_xV_{osz}$. A resistor-product error of α will cause a V_x feedthrough of $\pm \alpha V_x$. Likewise, V_y feedthrough errors are: $\pm V_yV_{osx}$, $\pm V_yV_{osz}$ and $\pm \beta V_y$.

Total feedthrough =
$\pm V_xV_{osy} \pm V_yV_{osx} \pm \alpha V_x \pm \beta V_y \pm (V_x + V_y)\, V_{osz}$

By carefully adjusting $X_{os}(R_5)$, $Y_{os}(R9)$ and $Z_{os}(R_{20})$ this equation can be made to very nearly equal zero and the feedthrough error will practically disappear.

A residual offset will probably remain which can be trimmed out with $V_{os}(R_{16})$ at the output op amp.

Method #2

Notice that the ratios of $R_1R_b : R_{cx}R_d$ and $R_2R_a : R_{cy}R_d$ are both dependent on R_d, also that R_1, R_2, R_a and R_b are all functions of the maximum input requirements. By designing a multiplier for the same input ranges on both V_x and V_y then $R_1 = R_2$, $R_{cx} = R_{cy}$ and $R_a = R_b$. (Note: It is acceptable to design a four quadrant multiplier and use only two quadrants of it.)

Select R_d to be 1% or 2% below (or above) the calculated value. This will cause α and β to both be positive (or negative) by nearly the same amount. Now the effective value of R_d can be trimmed with an offset adjustment $Z_{os}(R_{20})$ on pin 5.

This technique will cause: 1) a slight gain error which can be compensated for with the R_0 value, and 2) an output offset error that can be trimmed out with $V_{os}(R_{16})$ on the output op amp.

Extended Range Divider (Figure 8)

The only crossproduct error of interest is the V_z feedthrough ($V_x = 0$ and $V_{osx} \neq 0$) which is easily adjusted with $X_{os}(R_5)$.

Resistor product mis-match will cause scaling errors (gain) that could be a problem for very low values of V_z. Adjustments to $Y_{os}(R_{18})$ can be made to improve the high gain accuracy.

Square Root and Squaring (Figures 10 and 12)

These circuits are functions of single variables so feedthrough, as such, is not a consideration. Crossproduct errors will effect incremental accuracy that can be corrected with $Y_{os}(R_{14})$ or $Z_{os}(R_{10})$.

Appendix 2 — Applications

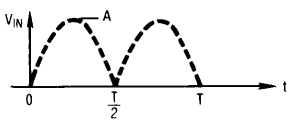
Design Considerations for RMS-to-DC Circuits

Average Value

Consider $V_{in} = A\sin\omega t$. By definition,

$$V_{AVG} \equiv \frac{2}{T}\int_0^{\frac{T}{2}} V_{in}\,dt$$

Where T = Period
$\omega = 2\pi f$
$= \frac{2\pi}{T}$



$$V_{AVG} \equiv \frac{2}{T}\int_0^{\frac{T}{2}} A\sin\omega t\,dt$$
$$= \frac{2A}{T}\left[-\frac{1}{\omega}\cos\omega t\right]_0^{\frac{T}{2}}$$
$$= \frac{2A}{2\pi}\left[-\cos(\pi) + \cos(0)\right]$$
$$= \frac{2}{\pi}A$$

Avg. Value of $A\sin\omega t$ is $\frac{2}{\pi}A$

RMS Value

Again consider $V_{in} = A\sin\omega t$

$$V_{rms} = \sqrt{V_{AVG}} = \sqrt{\frac{1}{T}\int_0^T [V_{in}]^2\,dt}$$

V_{rms} for $A\sin\omega t$:

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T A^2\sin^2\omega t\,dt}$$
$$= \sqrt{\frac{A^2}{T}\int_0^T\left(\frac{1}{2} - \frac{1}{2}\cos 2\omega t\right)dt}$$
$$= \sqrt{\frac{A^2}{2}\left(\frac{T}{2} - \frac{1}{4\omega}\sin 2\omega t\right)_0^T}$$
$$= \sqrt{\frac{A^2}{T}\left(\frac{T}{2}\right)}$$
$$= \sqrt{\frac{A^2}{2}}$$

therefore the rms value of $A\sin\omega t$ becomes:

$$V_{rms} = \frac{A}{\sqrt{2}}$$

RMS Value for Rectified Sine Wave

Consider $V_{in} = |A\sin\omega t|$, a rectified wave. To solve, integrate over each half cycle.

$$\text{i.e. } \frac{1}{T}\int_0^T V_{in}^2\,dt =$$
$$\frac{1}{T}\left[\int_0^{\frac{T}{2}} A^2\sin^2\omega t\,dt + \int_{\frac{T}{2}}^T (-A\sin\omega t)^2 dt\right]$$

This is the same as $\frac{1}{1}\int_0^T A^2\sin^2\omega t\,dt$

so, $|A\sin\omega t|_{rms} = A\sin\omega t_{rms}$

Practical Consideration: $|A\sin\omega t|$ has high-order harmonies; $A\sin\omega t$ does not. Therefore, non-ideal integrator may cause different errors for two approaches:

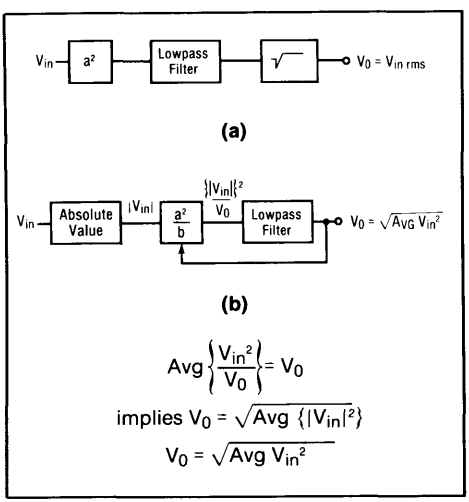


Figure 15

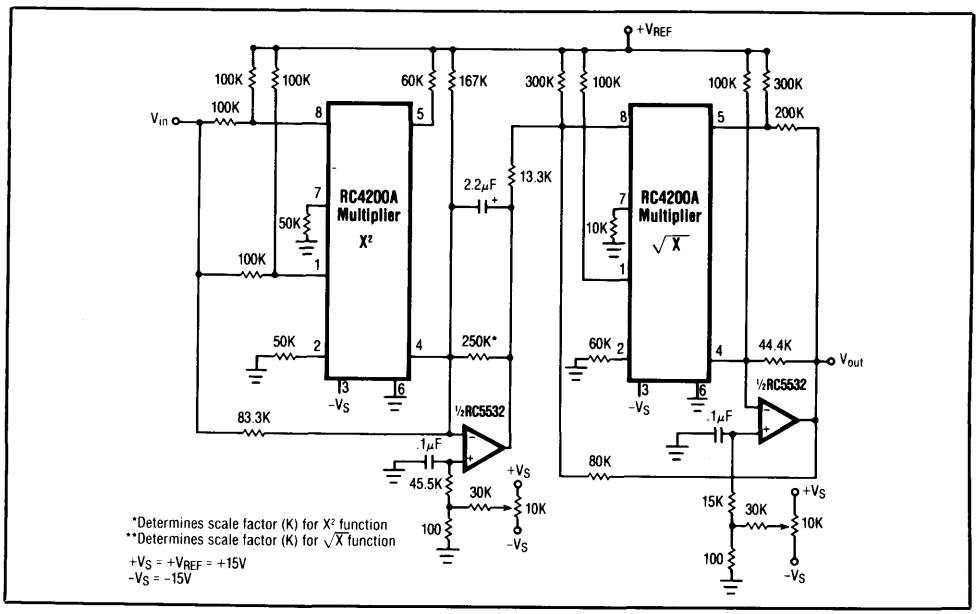


Figure 16. RMS to DC Converter $V_{out} = \sqrt{\int V_{in}^2}$

Amplitude Modulator with A.G.C. (Figure 17)

In many AC modulator applications unwanted output modulation is caused by variations in carrier input amplitude. The versatility of the RC4200 multiplier can be utilized to eliminate this undesired fluctuation. The extended range multiplier circuit (Figure 5) shows an output amplitude inversely proportional to the reference voltage V_{REF}.

$$\text{i.e., } V_0 = \frac{V_x V_y}{V_{REF}} \frac{R_0 R_d}{R_1 R_2}$$

By making V_{REF} proportional to V_y (where V_y is the carrier input) such that:

$$V_{REF} = V_H = f(|V_y|),$$

Then the denominator becomes a variable value that automatically provides constant gain, such that the modulating input (V_x) modulates the carrier (V_y) with a fixed scale factor even though the carrier varies in amplitude.

If V_H is made proportional to the average value of $A\sin\omega t$ (i.e., $2A/\pi$) and scaled by a value of $\pi/2$ then:

$$V_H = A$$

and if: V_x = Modulating input (V_M)
and: V_y = Carrier input ($A\sin\omega t$)

then: $V_0 = K V_M \sin\omega t$ where $K = \frac{R_0 R_d}{R_1 R_2}$

The resistor scaling is determined by the dynamic range of the carrier variation and modulating input.

The resistor values are solved, as with the other extended range circuits, in terms of the input voltages.

Input voltages:
Modulation Voltage (V_M): $0 \le V_M \le V_x$(max.)
Carrier (V_y: $V_y = A\sin\omega t$
Carrier amplitude fluctuation (ΔA):
$A(\text{min.})\sin\omega t \le V_y \le A(\text{max.})\sin\Omega\omega t$
Dynamic Range (N): A(max.)/A(min.)
$A(\text{max.}) = V_H(\text{max.})$ and $A(\text{min.}) = V_H(\text{min.})$

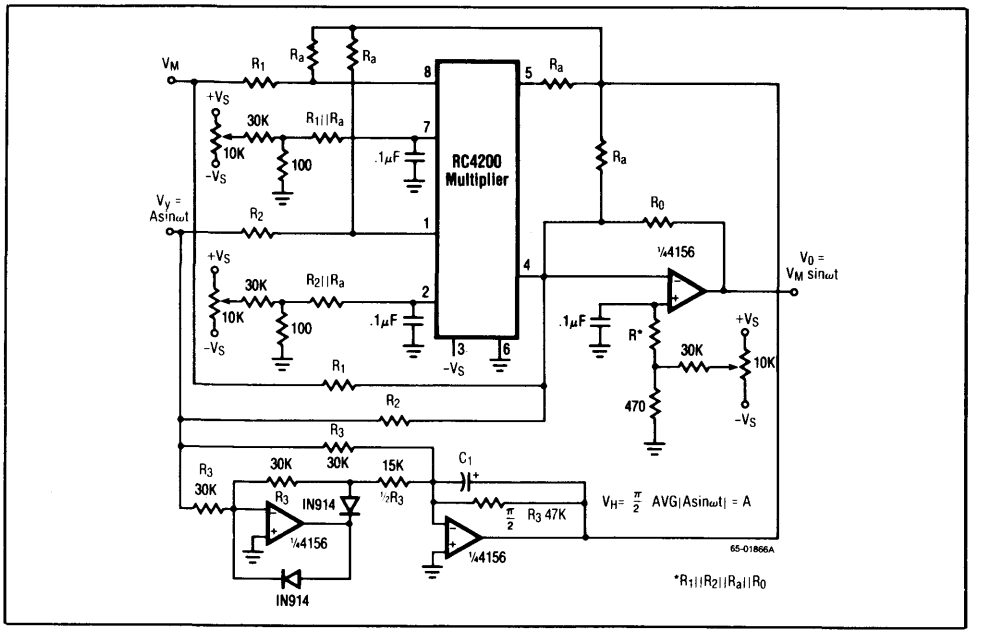


Figure 17. Amplitude Modulator with A.G.C.

The maximum and minimum values for I_1 and I_2 lead to:

$$I_1(max.) = \frac{V_x(max.)}{R_1} + \frac{V_H(max.)}{R_a} = 250\mu A$$

$$I_1(min.) = \frac{V_H(min.)}{R_a} = 50\mu A \quad V_M(min.) = 0$$

$$I_2(max.) = \frac{A(max.)}{R_2} + \frac{V_H(max.)}{R_a} = 250\mu A$$

$$I_2(min.) = \frac{V_H(min.)}{R_a} = 50\mu A$$

For a dynamic range of N, where

$$N = \frac{A(max.)}{A(min.)} < 5,$$

These equations combine to yield:

$$R_1 = \frac{V_x(max.)}{(5-N)50\mu A}, \; R_2 \frac{A(max.)}{(5-N)50\mu A},$$

$$R_a = \frac{A(min.)}{50\mu A} \text{ and } R_0 = K\,\frac{R_1R_2}{R_a}$$

Example #1

V_y = Asinωt 2.5V ≤ A ≤ 10V, therefore N = 4
0V ≤ V_M ≤ 10V, therefore V_x(max.) = 10V
K = 1, therefore $V_0 = V_M$ sinωt

$$R_1 = \frac{V_x(max.)}{50\mu A} = \frac{10V}{50\mu A} = 200K$$

$$R_2 = \frac{A(max.)}{50\mu A} = \frac{10V}{50\mu A} = 200K$$

$$R_a = \frac{A(min.)}{50\mu A} = \frac{2.5V}{50\mu A} = 50K$$

$$R_0 = K\,\frac{R_1R_2}{R_a} = 1\,\frac{200K \times 200K}{50K} = 800K$$

Example #2

V_y = Asinωt 3 ≤ A ≤ 6, therefore N = 2
0V ≤ V_M ≤ 8V, therefore V_x(max.) = 8V
K = .2, therefore $V_0 = .2V_M$sinωt
so:
R_1 = 53.3K, R_2 = 40K
R_a = 60K and R_0 = 7.11K

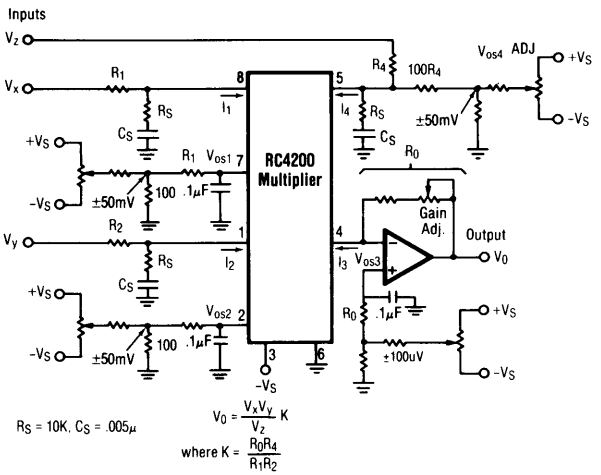


Figure 18. First Quadrant Multiplier/Divider

Limited Range, First Quadrant Applications

The following circuit has the advantage that cross-product errors are due only to input offsets and nonlinearity error is slightly less for lower input currents.

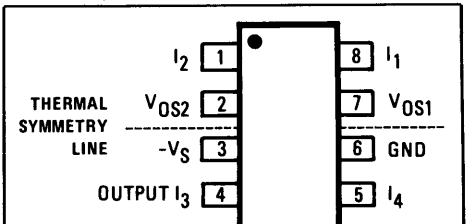
The circuit also has no standby current to add to the noise content although the signal-to-noise ratio worsens at very low input currents (1–5μA) due to the noise current of the input stages.

The $R_S C_S$ filter circuits are added to each input to improve the stability for input currents below 50μA.

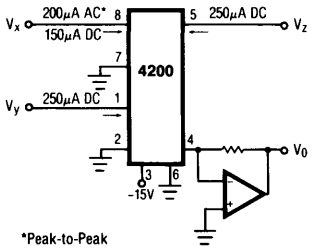
Caution

The bandpass drops off significantly for lower currents (<50μA) and non-symmetrical rise and fall times can cause second harmonic distortion.

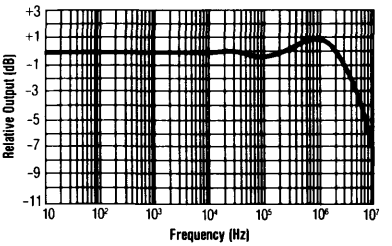
Thermal Symmetry

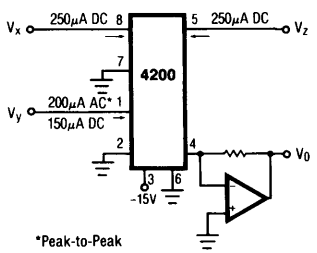


The scale factor is sensitive to temperature gradients across the chip in the lateral direction. Where possible, the package should be oriented such that sources generating temperature gradients are located physically on the line of thermal symmetry. This will minimize scale-factor error due to thermal gradients.

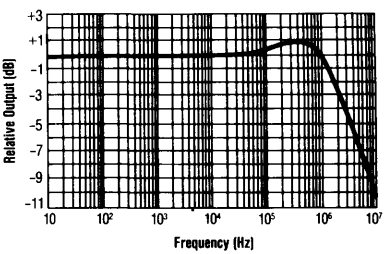


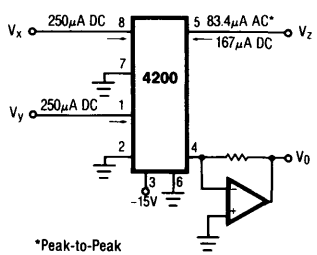
*Peak-to-Peak



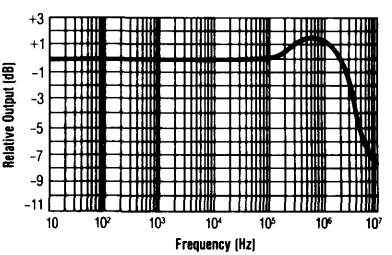


*Peak-to-Peak





*Peak-to-Peak



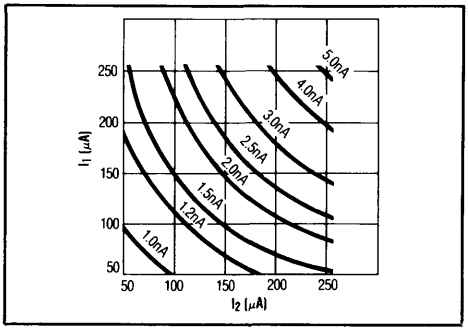


Figure 20a. Output Noise Current vs. Input Current (I_4 = 250μA)

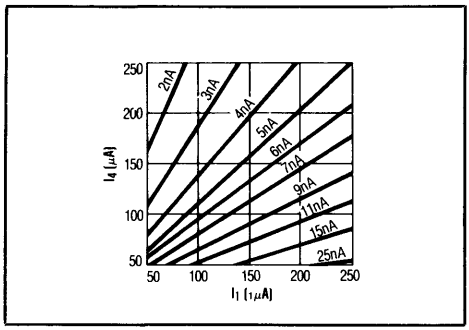


Figure 20b. Output Noise Current vs. Input Current (I_2 = 250μA)

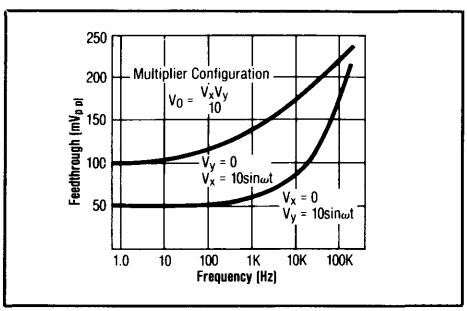


Figure 21. AC Feedthrough vs. Frequency

High Reliability Options

Part Type	Added Screening	Order Part No.
RM4200DE RM4200ADE	With MIL-STD-883 Class B processing	RM4200DE/883B RM4200ADE/883B
RV4200DE RC4200DE RV4200ADE RC4200ADE	With A + 3 processing* including burn-in and tightened AQL	RV4200DE3 RC4200DE3 RV4200ADE3 RC4200ADE3
RV4200NB RC4200NB RV4200ANB RC4200ANB	With A + 2 processing* including "Hot Rail" testing, burn-in and tightened AQL	RV4200NB2 RC4200NB2 RV4200ANB2 RC4200ANB2
RV4200NB RC4200NB RV4200ANB RC4200ANB	With A + 1 processing* including "Hot Rail" testing, and tightened AQL	RV4200NB1 RC4200NB1 RV4200ANB1 RC4200ANB1

*Full descriptions of the process steps involved are contained in the Raytheon A + Bulletin available at your local Raytheon Sales Office

Raytheon

Synchronous Detector

RC4260

Features

- 10μS switching
- TTL compatible
- Low distortion — .01% typical
- Wide supply voltage range — to ±3V typical
- Low gain differential — 1.0% maximum
- On-board op amp

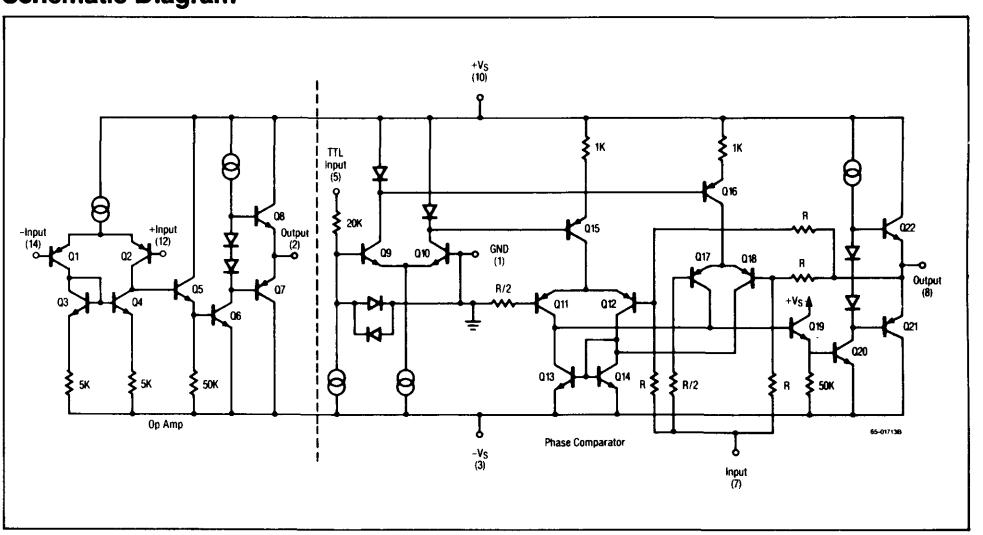
Applications

- Suppressed carrier modulation
- Synchronous detection
- Frequency doubling/chopping
- Precision rectification with switchable polarity
- Phase comparison

Description

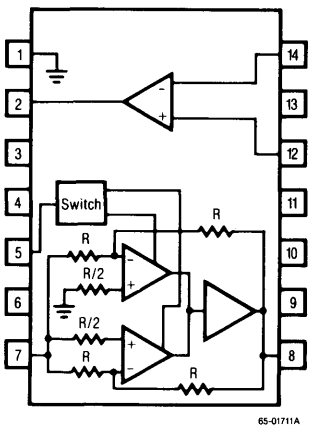
The 4260 is a unity gain amplifier with logic switchable phase inversion. A TTL high state on the reference (logic) input will force the amplifier into non-inverting operation; a TTL low state will force inverting operation. Excellent matching between inverting and non-inverting AC performance is achieved through careful design and layout. Included with the phase comparator is an uncommitted 4558 type op amp, which can be used for gain, filtering, or other applications.

Schematic Diagram



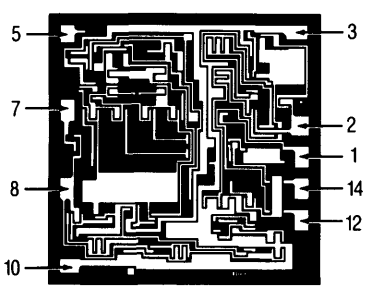
Connection Information

14-Lead
Dual In-Line Package
(Top View)



Pin	Function
1	Ground
2	Op Amp Output
3	$-V_S$
4	NC
5	Reference Input (TTL)
6	NC
7	Amplifier Input
8	Amplifier Output
9	NC
10	$+V_S$
11	NC
12	Op Amp +Input
13	NC
14	Op Amp -Input

Mask Pattern



Die Size: 00 x 00 mils
Min. Pad Dimension: 4 x 4 mils

Ordering Information

Part Number	Package	Operating Temperature Range
RC4260DB	Plastic	0°C to +70°C
RC4260DC	Ceramic	0°C to +70°C
RM4260DC	Ceramic	-55°C to +125°C
RM4260DC/883B*	Ceramic	-55°C to +125°C

*MIL-STD-883, Level B Processing

Absolute Maximum Ratings

Supply Voltage
RM4260 ..... ±22V
RC4260 ..... ±18V
Internal Power Dissipation 500mW
Differential Input Voltage 30V
Input Voltage ..... ±15V
Output Short Circuit to Ground .. Continuous
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
RM4260 ..... -55°C to +125°C
RC4260 ..... 0°C to +70°C
Lead Soldering Temperature
(10 Sec) ..... +300°C

Thermal Characteristics

	14-Lead Ceramic DIP	14-Lead Plastic DIP
Max. Junction Temp.	175°C	125°C
Max. P_D $T_A < 50°C$	1042mW	468mW
Therm. Res. θ_{JC}	60°C/W	—
Therm. Res. θ_{JA}	120°C/W	160°C/W
For $T_A > 50°C$ Derate at	8.33mW per °C	6.25mW per °C

Electrical Characteristics

(V_S = ±15V, over full operating temperature range unless otherwise noted)

Parameters	Test Conditions	RM4260			RC4260			Units
		Min	Typ	Max	Min	Typ	Max	
Supply Current	$R_L = \infty$		6.0	11		4.0		mA
Op Amp Section								
Input Offset Voltage	$R_S \leq 10k\Omega$		4.5	7.0		3.5		mV
Input Offset Current			250	500		250		nA
Input Bias Current			600	1500		600		nA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	25	100			100		V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	±10	±13			±13		V
Common Mode Rejection Ratio	V_{CM} = 24V	70	100			100		dB
Power Supply Rejection Ratio	ΔV = 20V	76	92			92		dB
Comparator Section								
Large Signal Voltage Gain	Pin 7 = ±7.5V	±0.95	±1.0	±1.05				V/V
Input Offset Voltage			5.0	12		5.0		mV
Input Resistance (Differential Mode)		10	25			25		kΩ
Output Voltage Swing	$R_L = 10k\Omega$	±12	±13.5			±13.5		V
Power Supply Rejection Ratio	ΔV = 10V	76	92			92		dB
Reference Input Threshold			1.25			1.25		V
Reference Input Current	Pin 5 = 2V		150			150		μA
Gain Differential	$\frac{A_{V(+1)} - A_{V(-1)}}{A_{V(+1)} + A_{V(-1)}} \times 100$		1.0			1.0		%

Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	RM4260			RC4260			Units
		Min	Typ	Max	Min	Typ	Max	
Supply Current	$R_L = \infty$		4.0	9.0		5.0	10	mA
Op Amp Section								
Input Offset Voltage	$R_S \leq 10k\Omega$		3.5	5.0		3.5	6.0	mV
Input Offset Current			75	200		75	200	nA
Input Bias Current			175	500		175	500	nA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_O = ±10V	50	300		20	300		V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	±10	±13		±10	±13		V
Common Mode Rejection Ratio	V_{CM} = 24V	70	100		70	100		dB
Power Supply Rejection Ratio	ΔV = 20V	76	100		76	100		dB
Slew Rate	A_V = +1		0.8			0.8		V/μS
Unity Gain Bandwidth			3.0			3.0		MHz
Comparator Section								
Large Signal Voltage Gain	Pin 7 = ±7.5V	±0.95	±1.0	±1.05	±0.95	±1.0	±1.05	V/V
Input Offset Voltage			4.0	7.0		4.0	10	mV
Input Resistance		10	25		10	25		kΩ
Output Voltage Swing	R_L = 10kΩ	±12			±12			V
Power Supply Rejection Ratio	ΔV = 10V	76	94		76	94		dB
Reference Input Threshold			1.25			1.25		V
Reference Input Current	Pin 5 = 2V		75			75		μA
Gain Differential	$\frac{A_{V(+1)} - A_{V(-1)}}{A_{V(+1)} + A_{V(-1)}} \times 100$		1.0			1.0		%
Carrier Suppression	V_{IN} = $2V_{PP}$ at 10kHz		50			50		dB
Slew Rate			1.25			1.25		V/μS
Switching Speed			10			10		μS

Principles of Operation

The 4260 is made up of two circuit functions: an op amp (pins 2,12,14), which is independent, and a synchronous detector consisting of a differential switch (Q9,10,15,16), two differential amplifiers (Q11,12 and Q17,18), an active load (Q13,14), and an output stage with gain. The switch selects between the diff amps; one diff amp (Q11,12) is inverting, the other is non-inverting. The resistors R set the gain from pin 7 to 8 at unity. When the switch changes from supplying bias current into Q11,12 to supplying bias current to Q17,18, the gain will change from -1 to +1, and the phase shift will change from 180° to 0°. Both diff amps feed the same active load and output stage; the amplifier that is switched off is isolated from the active load by reverse biased PN junctions. Aside from the switching function, the amplifier design is similar to the uncommitted 4558 type op amp.

Figure 1 shows a balanced modulator application. Figure 2 is a spectral plot of the output, depicting the sine frequency, the reference frequency, the sum of the sine and reference frequencies, and all of the harmonics for one decade.

The reference (TTL) input is attenuated typically 50dB below the sine and sum frequencies. Best suppression will be achieved at input amplitudes from 1V to 10V peak-to-peak.

Typical Applications

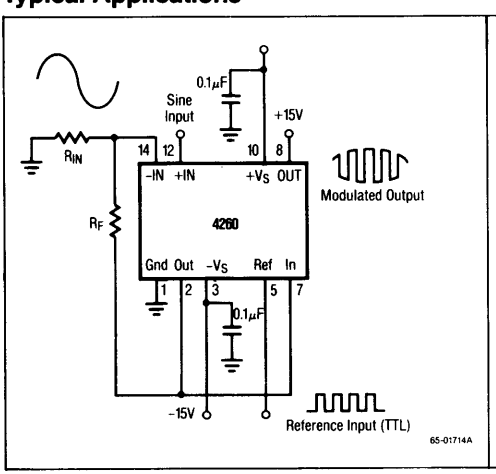


Figure 1. Suppressed Carrier Modulation

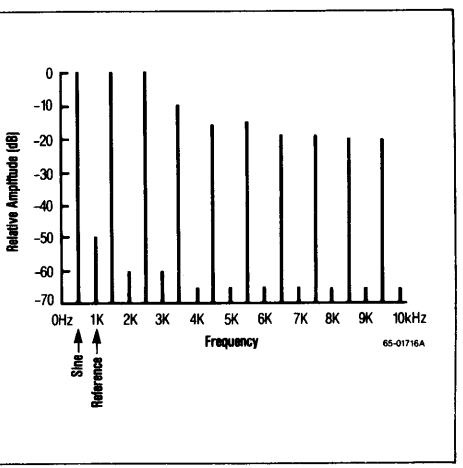


Figure 2. Spectral Plot (V_{IN} = 500Hz, TTL Ref = 1kHz)

Typical Applications (Continued)

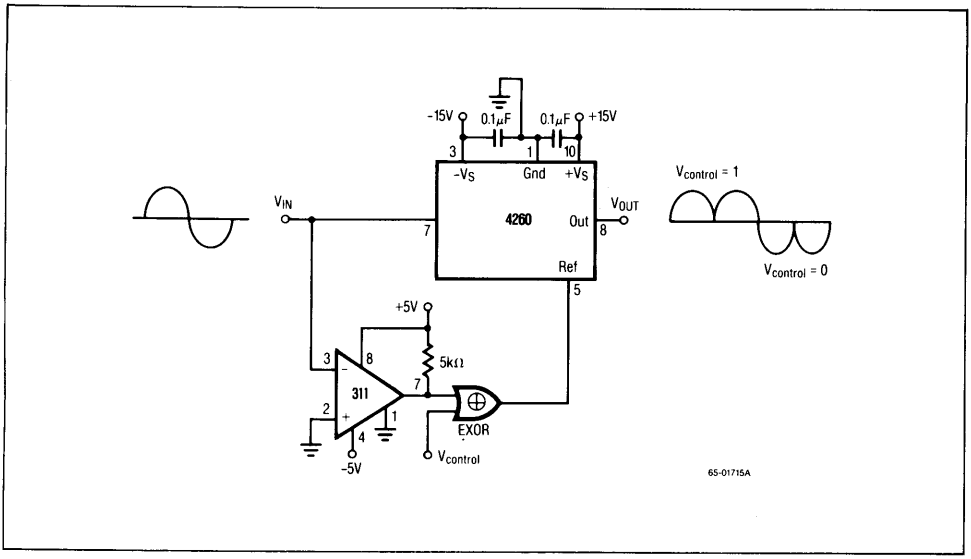


Figure 3. Precision Rectifier With Logic Switchable Output Polarity

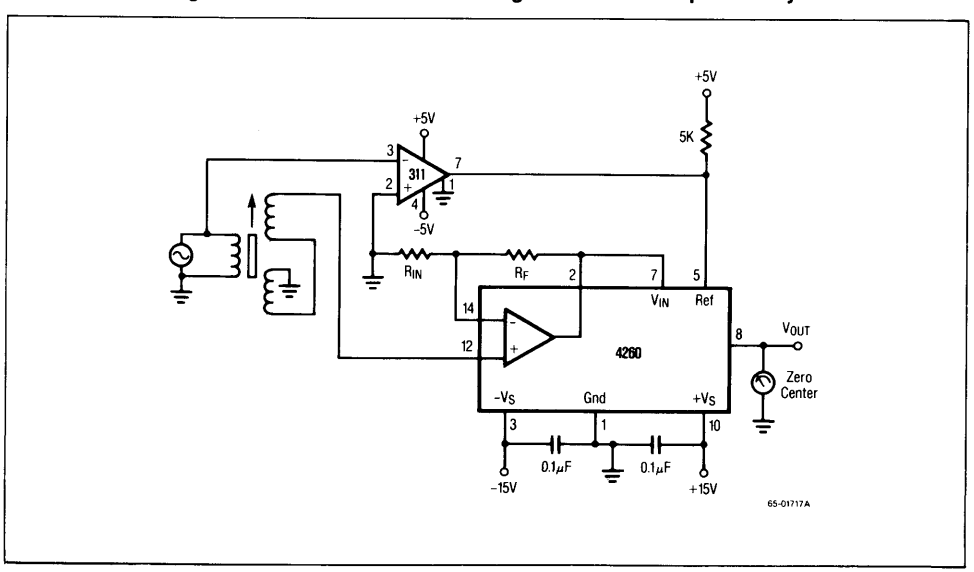


Figure 4. Linear Variable Differential Transformer With Phase Sensitive Detector

Typical Applications (Continued)

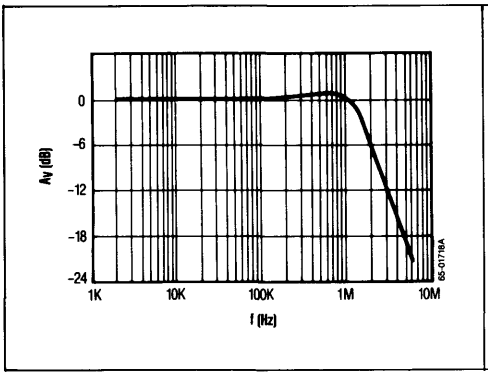


Figure 5. Gain vs. Frequency

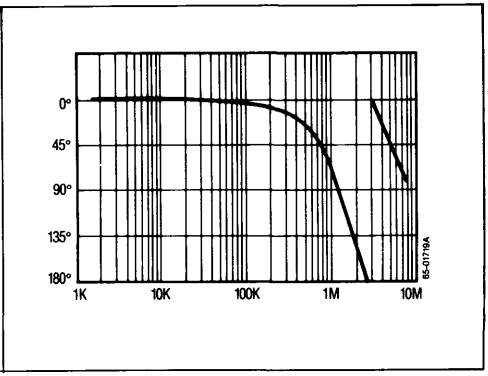


Figure 6. Phase vs. Frequency

Raytheon

4 x 4 x 2 Balanced Switching Crosspoint Array

RC4444

Features

- Low bidirectional R_{ON}
- High R_{OFF}
- Excellent matching of gates
- Low capacitance
- High rate firing
- Predictable holding current

Description

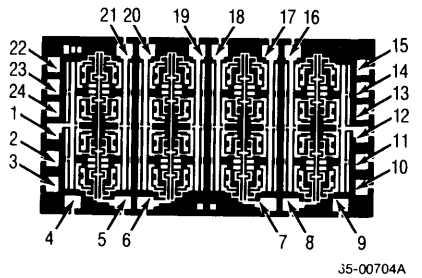
The RC4444 is a monolithic dielectrically isolated crosspoint array arranged into a 4 x 4 x 2 matrix. The primary application is for balanced switching of 600Ω transmission lines. The ring and tip are selected by selective biasing of the P+ and P- gate.

Designed to replace reed relays in telephone switchboards, it does not require a constant gate drive to keep the SCR in the "ON" condition. It is several orders faster, with no bouncing, and has a much longer operating life than its mechanical counterpart.

The 16 SCR pairs with the gating system are packaged in a 24-pin dual in-line package.

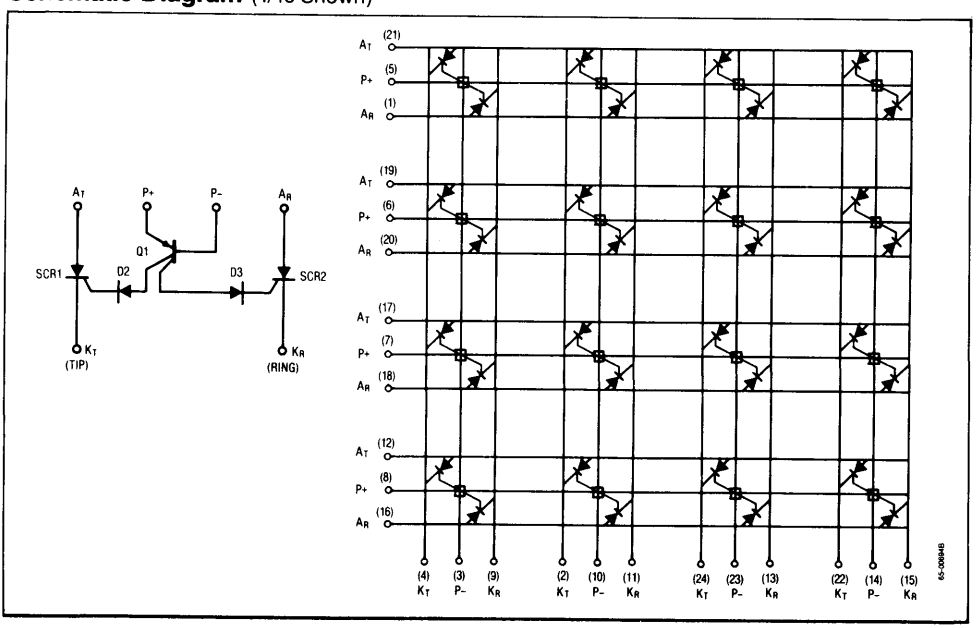
The RC4444 is a monolithic pin-for-pin replacement for the MC3416 and MCBH7601.

Mask Pattern



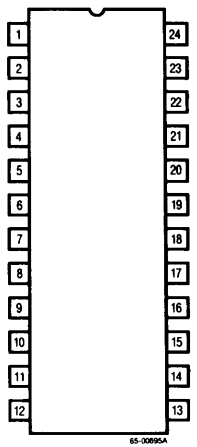
Die Size: 60 x 108 mils
Min. Pad Dimensions: 4 x 4 mils

Schematic Diagram (1/16 Shown)



Connection Information

24-Lead
Dual In-Line Package
(Top View)



Pin	Function	Pin	Function
1	Anode A_R	13	Cathode K_R
2	Cathode K_T	14	Row Select P-
3	Row Select P-	15	Cathode K_R
4	Cathode K_T	16	Anode A_R
5	P+ Column Select A	17	Anode A_T
6	P+ Column Select B	18	Anode A_R
7	P+ Column Select C	19	Anode A_T
8	P+ Column Select D	20	Anode A_R
9	Cathode K_R	21	Anode A_T
10	Row Select P-	22	Cathode K_T
11	Cathode D_R	23	Row Select P-
12	Anode A_T	24	Cathode K_T

Absolute Maximum Ratings

Operating Voltage[1] ..... +25V
Operating Current per Crosspoint 100mA
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
RC4444 ..... 0°C to +70°C
Lead Soldering Temperature
(60 Sec) ..... +300°C

Notes: 1. Maximum voltage from anode to cathode.

Thermal Characteristics

	24-Lead Plastic DIP	24-Lead Ceramic DIP
Max. Junction Temp.	125°C	175°C
Max. P_D T_A < 50°C	555mW	1042mW
Therm. Res. θ_{JC}	—	60°C/W
Therm. Res. θ_{JA}	135°C/W	120°C/W
For T_A > 50°C Derate at	7.41mW per °C	8.33mW per °C

Ordering Information

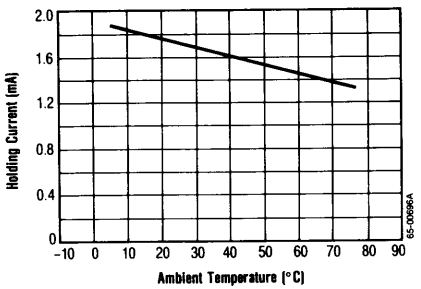
Part Number	Package	Operating Temperature Range
RC4444R	Ceramic	0°C to +70°C
RC4444PU	Plastic	0°C to +70°C

Electrical Characteristics ($0°C \leq T_A \leq +70°C$ unless otherwise noted)

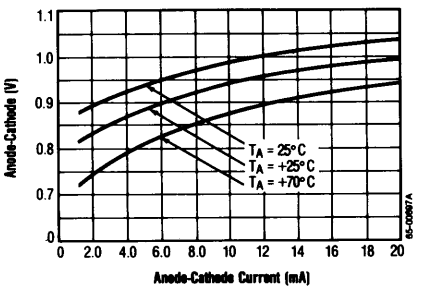
Parameters	Test Conditions	Min	Typ	Max	Units
Anode-Cathode Breakdown Voltage	$I_{AK} = 25\mu A$	25			V
Cathode-Anode Breakdown Voltage	$I_{KA} = 25\mu A$	25			V
Base-Cathode Breakdown Voltage	$I_{BK} = 25\mu A$	25			V
Cathode-Base Breakdown Voltage	$I_{KB} = 25\mu A$	25			V
Base-Emitter Breakdown Voltage	$I_{BE} = 25\mu A$	25			V
Emitter-Cathode Breakdown Voltage	$I_{EK} = 25\mu A$	25			V
OFF State Resistance	$V_{AK} = 10V$	100			MΩ
Dynamic ON Resistance	Center Current = 10mA	4.0		12	Ω
	Center Current = 20mA	2.0		10	
Holding Current		0.9		3.8	mA
Enable Current	$V_{BE} = 1.5V$	4.0			mA
Anode-Cathode ON Voltage	$I_{AK} = 10mA$			1.0	V
	$I_{AK} = 20mA$			1.1	
Gate Sharing Current Ratio at Cathodes	Under Select Conditions with Anodes Open	0.8		1.25	mA/mA
Inhibit Voltage	$V_B = 3.0V$			0.3	V
Inhibit Current	$V_B = 3.0V$			0.1	mA
OFF State Capacitance	$V_{AK} = 0V$			2.0	pF
Turn-ON Time				1.0	μS
Minimum Voltage Ramp	Which Could Fire the SCR Under Transient Conditions	800			V/μS

Typical Performance Characteristics

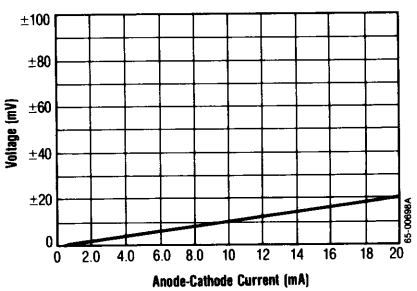
Holding Current vs. Ambient Temperature



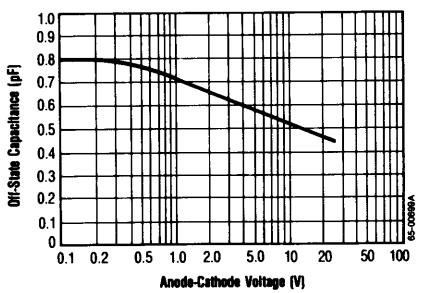
Anode-Cathode on Voltage vs. Current and Temperature



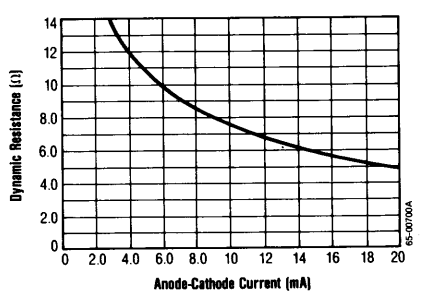
Difference in Anode-Cathode on Voltage (Between Associate Pairs of SCRs) vs. Anode-Cathode Current



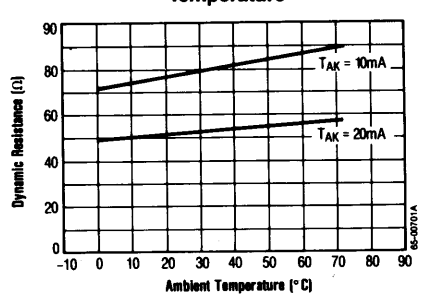
Off-Site Capacitance vs. Anode-Cathode Voltage



Dynamic on Resistance vs. Anode-Cathode Current

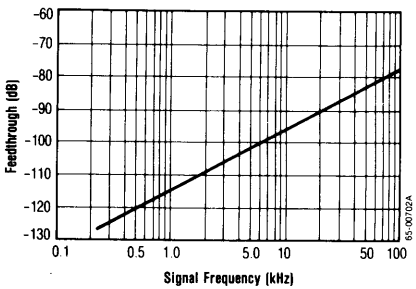


Dynamic on Resistance vs. Ambient Temperature

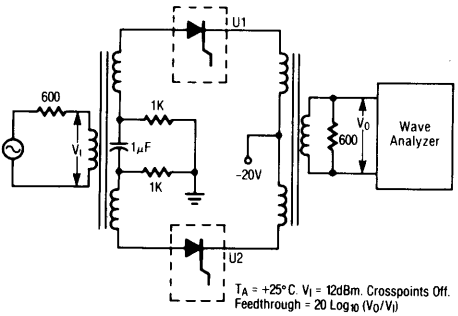


Typical Performance Characteristics (Continued)

Feedthrough vs. Signal Frequency



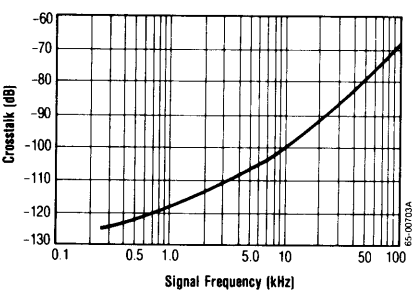
Test Circuit for Feedthrough vs. Frequency



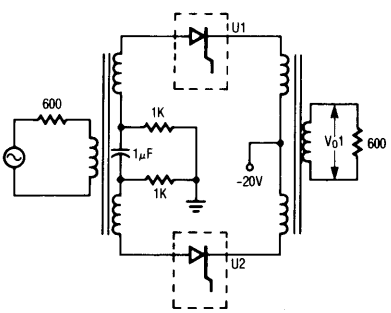
T_A = +25°C. V_I = 12dBm. Crosspoints Off.
Feedthrough = 20 Log_{10} (V_O/V_I)

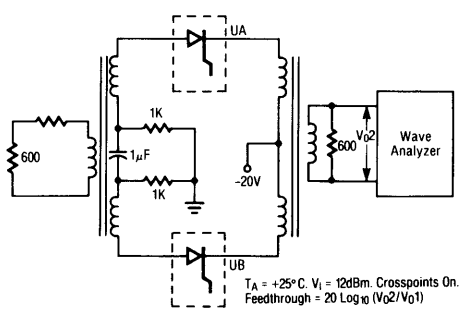
65-02049A

Crosstalk vs. Signal Frequency



Test Circuit for Crosstalk vs. Frequency





T_A = +25°C. V_I = 12dBm. Crosspoints On.
Feedthrough = 20 Log_{10} (V_{O2}/V_{O1})

65-02050A

Raytheon

Ground Fault Interrupters

RV4143, 4144

Features

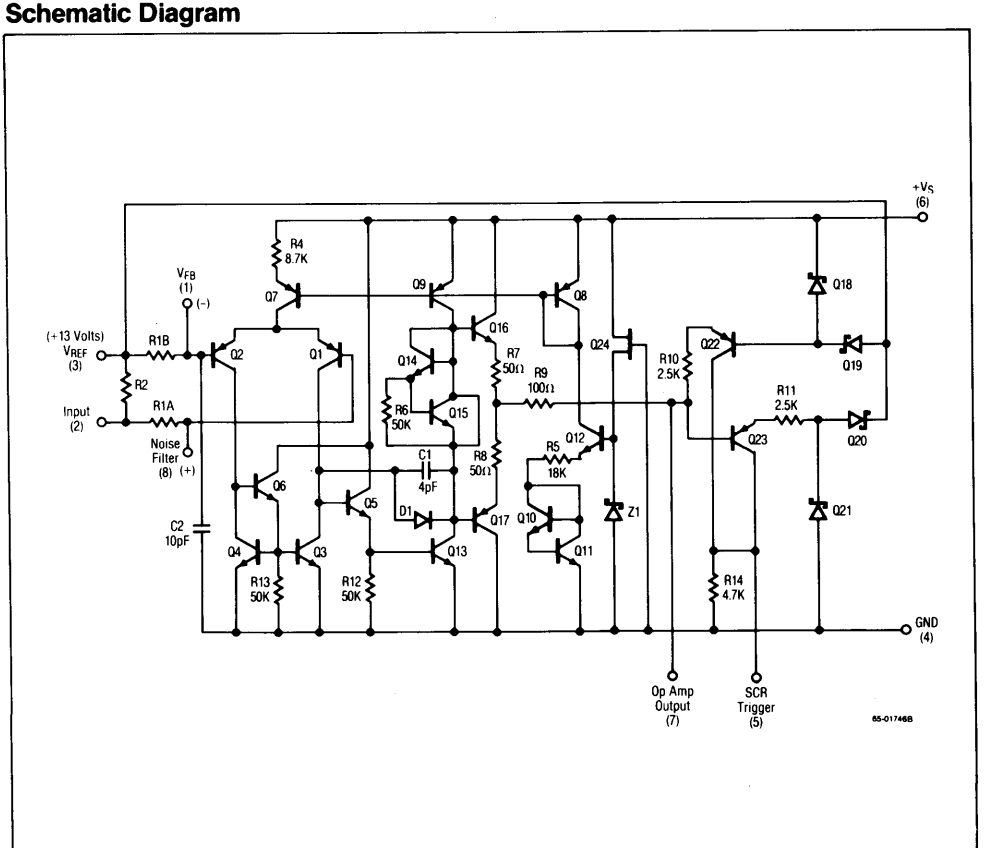
- Direct interface to SCR
- Supply voltage derived from AC line — 26V shunt
- Adjustable sensitivity
- Grounded neutral detection
- Complies with U.S. UL943

Description

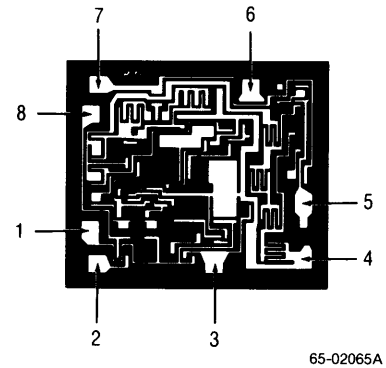
The RV4143 and RV4144 are controllers for AC outlet ground fault interrupters. These devices detect hazardous grounding conditions, such as a pool of water and equipment connected to opposite phases of the AC line, and open circuit the line before a harmful or lethal shock occurs.

Contained internally are a 26V zener shunt regulator, an op amp, and an SCR driver. With the addition of two sense coils, a bridge rectifier, an SCR, and a relay the 4143 or 4144 will detect and protect against both hot wire to ground and neutral wire to ground faults. The simple layout and conventional design ensure ease of application and long term reliability.

Schematic Diagram



Mask Pattern

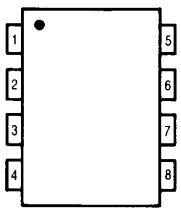


65-02065A

Die Size: 56 x 49 mils
Min. Pad Dimensions: 4 x 4 mils

Connection Information

8-Lead
NB Plastic
Dual In-Line Package
(Top View)



65-1747A

Pin	Function
1	V_{FB}
2	Input
3	V_{REF} (+13V)
4	Ground
5	SCR Trigger
6	$+V_S$
7	Op Amp Output
8	Noise Filter

Absolute Maximum Ratings

Supply Current 18mA
Internal Power Dissipation 500mW
Storage Temperature
Range ..... -65° C to +150° C
Operating Temperature
Range ..... -35° C to +80° C
Lead Soldering Temperature
(60 Sec) ..... +300° C

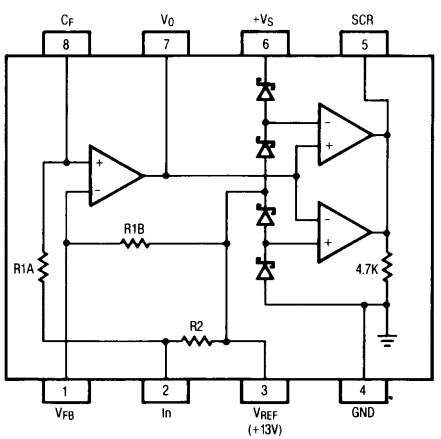
Ordering Information

Part Number	Package	Operating Temperature Range
RV4143NB	Plastic	-35° C to +80° C
RV4144NB	Plastic	-35° C to +80° C

Thermal Characteristics

	8-Lead Plastic DIP
Max. Junction Temp.	125° C
Max. P_D T_A < 50° C	468mW
Therm. Res. θ_{JC}	—
Therm. Res. θ_{JA}	160° C/W
For T_A > 50° C Derate at	6.25mW per °C

Functional Block Diagram



Input Resistor Values

R#	4143	4144
R1	1K	750Ω
R2	10K	2.5K

65-1748A

Electrical Characteristics (I_S = 5mA and T_A = +25° C)

Parameters	Test Conditions	Min	Typ	Max	Units
Shunt Regulator					
Zener Shunt Voltage	Pin 6	25	26	29.2	V
Reference Voltage	Pin 3	12.5	13	14.6	V
Op Amp					
Input Offset Voltage	Pin 2 to Pin 3	-3	±1	+3	mV
Output Voltage Swing	Pin 7 to Pin 3	±11	±13.5		V
AC Output Voltage	A_V = 500, f_{IN} = 50kHz V_{IN} = 1mV_{RMS}	50		180	mV_{RMS}
Resistors					
R14		3.8	4.7	5.7	kΩ
R1 RV4143		0.8	1.0	1.2	
R1 RV4144		0.6	0.75	0.9	
R2 RV4143		8.0	10.0	12.0	
R2 RV4144		2.0	2.5	3.0	
SCR Trigger					
V_{OH}	Across 4.7kΩ	1.5		6	V
V_{OL}				.01	

Electrical Characteristics (I_S = 5mA, over the specified temperature range)

Parameters	Test Conditions	Min	Typ	Max	Units
Shunt Regulator					
Zener Shunt Voltage	Pin 6	24	26	30	V
Reference Voltage	Pin 3	12	13	15	
Op Amp					
Input Offset Voltage	Pin 2 to Pin 3	-6	±2	+6	mV
Output Voltage Swing	Pin 7 to Pin 3	±10.5	±13		V
AC Output Voltage	A_V = 500, f_{IN} = 50kHz V_{IN} = 1mV_{RMS}	50		200	mV_{RMS}
Resistors					
R14		3.3	4.7	6.1	kΩ
R1 RV4143		0.7	1.0	1.3	
R1 RV4144		0.52	0.75	0.98	
R2 RV4143		7.0	10	13.0	
R2 RV4144		1.75	2.5	3.25	
SCR Trigger					
V_{OH}	Across 4.7kΩ	1.3		5	V
V_{OL}		1.3		.05	

Principles of Operation

The 26V shunt regulator voltage generated by the string of zener diodes is divided into three reference voltages: $\frac{3}{4}V_S$, $\frac{1}{2}V_S$, and $\frac{1}{4}V_S$. V_{REF} is at $\frac{1}{2}V_S$ and is used as a reference to create an artificial ground of +13V at the op amp non-inverting input. Fault signals from the sense coil are AC coupled into the input and are amplified according to the following equation:

$$A_V = \frac{R_F}{R_3} + 1$$

Where R_F equals the value of an external feedback resistor between pins 7 and 1.

When the output of the op amp swings above $\frac{3}{4}V_S$ or below $\frac{1}{4}V_S$ the SCR trigger output will go high and fire an external SCR.

Grounded neutral fault detection is accomplished when a short or fault closes a magnetic path between two sense coils. The resultant AC coupling through the three coils (the sense coil to the single-turn fault to the feedback coil) closes a positive feedback path around the op amp, and therefore the op amp oscillates. When the peaks of the oscillation voltage exceed the SCR trigger comparator thresholds the SCR output will go high.

Raytheon

Voltage-Controlled Oscillator

XR-2207

Features

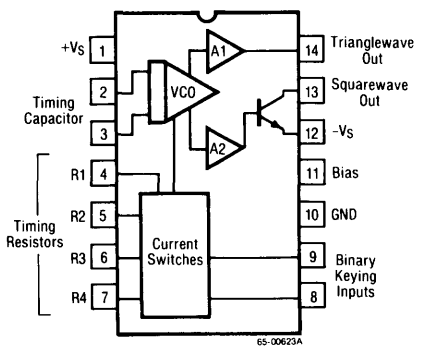
- Excellent temperature stability — 20ppm/°C
- Linear frequency sweep
- Adjustable duty cycle — 0.1% to 99.9%
- Two or four level FSK capability
- Wide sweep range — 1000:1 min
- Logic compatible input and output levels
- Wide supply voltage range — ±4V to ±13V
- Low supply sensitivity — 0.15%/V
- Wide frequency range — 0.01Hz to 1MHz
- Simultaneous triangle and squarewave outputs

Applications

- FSK generation
- Voltage and current-to-frequency conversion
- Stable phase-locked loop
- Waveform generation triangle, sawtooth, pulse, squarewave
- FM and sweep generation

Connection Information

14-Lead
Dual In-Line Package
(Top View)



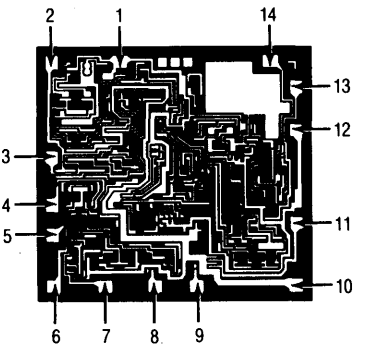
Description

The XR-2207 is a monolithic voltage-controlled oscillator (VCO) integrated circuit featuring excellent frequency stability and a wide tuning range. The circuit provides simultaneous triangle and squarewave outputs over a frequency range of 0.01Hz to 1MHz. It is ideally suited for FM, FSK, and sweep or tone generation, as well as for phase-locked loop applications.

As shown in the Schematic Diagram, the circuit is comprised of four functional blocks: a variable-frequency oscillator which generates the basic periodic waveforms; four current switches actuated by binary keying inputs; and buffer amplifiers for both the triangle and squarewave outputs. The internal switches transfer the oscillator current to any of four external timing resistors to produce four discrete frequencies which are selected according to the binary logic levels at the keying terminals (pins 8 and 9).

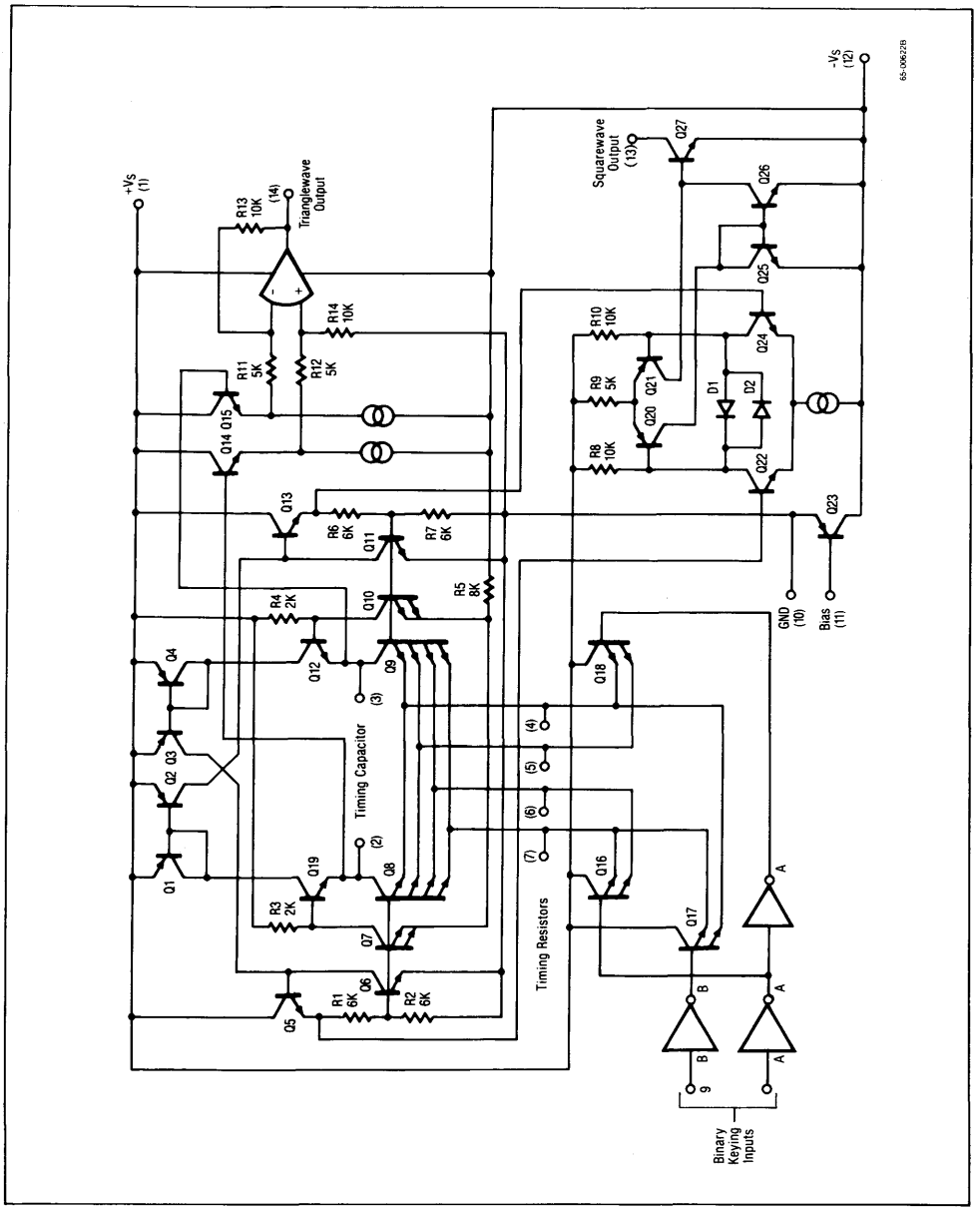
The XR-2207 has a typical drift specification of 20ppm/°C. The oscillator frequency can be linearly swept over a 1000:1 range with an external control voltage, and the duty cycle of both the triangle and the squarewave outputs can be varied from 0.1% to 99.9% to generate stable pulse and sawtooth waveforms.

Mask Pattern



Die Size: 85 x 80 mils
Min. Pad Dimensions: 4 x 4 mils

Schematic Diagram



Absolute Maximum Ratings

Supply Voltage ..... +26V
Storage Temperature
Range ..... -65°C to +150°C

Thermal Characteristics

	14-Lead Plastic DIP	14-Lead Ceramic DIP
Max. Junction Temp.	125°C	175°C
Max. P_D T_A < 50°C	468mW	1042mW
Therm. Res. θ_{JC}	—	60°C/W
Therm. Res. θ_{JA}	160°C/W	120°C/W
For T_A > 50°C Derate at	6.25mW per °C	8.33mW per °C

Ordering Information

Part Number	Package	Operating Temperature Range
XR-2207CN XR-2207CP	Ceramic Plastic	0°C to +75°C 0°C to +75°C
XR-2207N XR-2207P	Ceramic Plastic	-40°C to +85°C -40°C to +85°C
XR-2207M XR-2207M/883B*	Ceramic Ceramic	-55°C to +125°C -55°C to +125°C

*MIL-STD-883, Level B Processing

Electrical Characteristics

(Test Circuit of Figure 1, V_S = ±6V, T_A = +25°C = 5000pF, R1 = R2 = R3 = R4 = 20kΩ, R_L = 4.7kΩ, Binary inputs grounded, S1 and S2 closed unless otherwise specified)

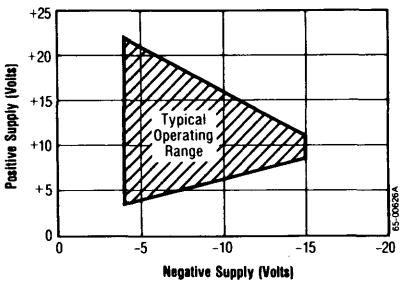
Parameters	Test Conditions	XR-2207 Min	XR-2207 Typ	XR-2207 Max	XR-2207C Min	XR-2207C Typ	XR-2207C Max	Units
General Characteristics								
Supply Voltage Single Supply Split Supplies	See Typical Performance Characteristics	 +8.0 ±4	 +12 ±6	 +26 ±13	 +8.0 ±4	 +12 ±6	 +26 ±13	V
Supply Current Single Supply Split Supplies Positive	Measured at pin 1, S1 open (See Fig. 2) Measured at pin 1, S1 open (See Fig. 1)		5.0 5.0	7.0 7.0		5.0 5.0	8.0 8.0	mA
Negative	Measured at pin 12, S1, S2 open		4.0	6.0		4.0	7.0	
Binary Keying Inputs								
Switching Threshold	Measured at pins 8 and 9. Refer to pin 10	1.4	2.2	2.8	1.4	2.2	2.8	V
Input Resistance			5.0			5.0		kΩ

Electrical Characteristics (Continued)

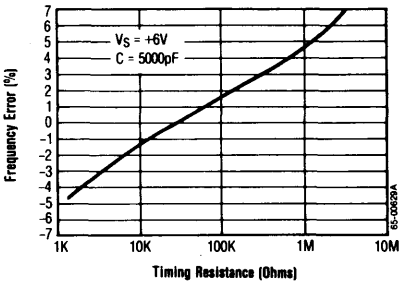
Parameters	Test Conditions	XR-2207			XR-2207C			Units
		Min	Typ	Max	Min	Typ	Max	
Oscillator Section — Frequency Characteristics								
Upper Frequency Limit	C = 500pF, R3 = 2kΩ	0.5	1.0		0.5	1.0		MHz
Lower Practical Frequency	C = 50μF, R3 = 2Ω		0.01			0.01		Hz
Frequency Accuracy			±1.0	±3.0		±1.0	±5.0	% of f_0
Frequency Matching			0.5			0.5		% of f_0
Frequency Stability Vs. Temperature	0°C < T_A < +75°C		20	50		30		ppm/°C
Vs. Supply Voltage			0.15			0.15		%/V
Sweep Range	R3 = 1.5kΩ for f_H R3 = 2MΩ for f_L	1000:1	3000:1			1000:1		f_H/f_L
Sweep Linearity 10:1 Sweep	C = 5000pF f_H = 10kHz, f_L = 1kHz		1.0	2.0		1.5		%
1000:1 Sweep	f_H = 100kHz, f_L = 100Hz		5.0			5.0		%
FM Distortion	±10% FM Deviation		0.1			0.1		%
Recommended Range of Timing Resistors	See Characteristic Curves	1.5		2000	1.5		2000	kΩ
Impedance at Timing Pins	Measured at pins 4, 5, 6 or 7		75			75		Ω
DC Level at Timing Terminals			10			10		mV
Output Characteristics								
Triangle Output Amplitude	Measured at pin 14	4	6		4	6		V_{p-p}
Impedance			10			10		Ω
DC Level	Referenced to pin 10 from 10% to 90% of swing		+100			+100		mV
Linearity			0.1			0.1		%
Squarewave Output Amplitude	Measured at pin 13, S2 Closed	11	12		11	12		V_{p-p}
Saturation Voltage	Referenced to pin 12		0.2	0.4		0.2	0.4	V
Rise Time	$C_L \leq$ 10pF		200			200		nS
Fall Time	$C_L \leq$ 10pF		20			20		nS

Typical Performance Characteristics

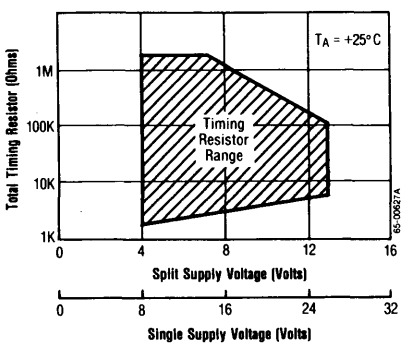
Typical Operating Range for Split Supply Voltage



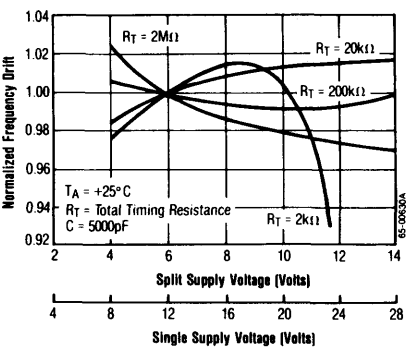
Frequency Accuracy vs. Timing Resistance



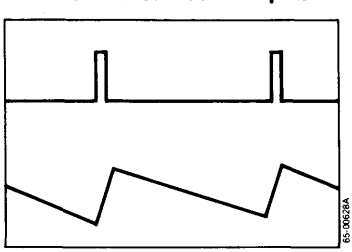
Recommended Timing Resistor Value vs. Power Supply Voltage*



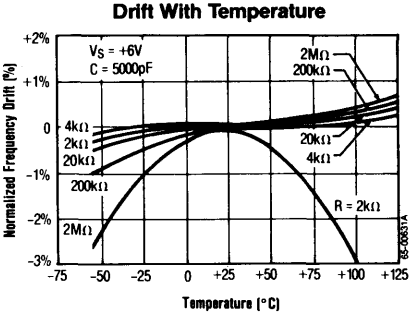
Frequency Drift vs. Supply Voltage



Pulse and Sawtooth Outputs



Normalized Frequency Drift With Temperature



* RT = Parallel Combination of Activated Timing Resistors

Description of Circuit Controls

Timing Capacitor (pins 2 and 3)
The oscillator frequency is inversely proportional to the timing capacitor, C. The minimum capacitance value is limited by stray capacitances and the maximum value by physical size and leakage current considerations. Recommended values range from 100pF to 100μF. The capacitor should be non-polarized.

Timing Resistors (pins 4, 5, 6, and 7)
The timing resistors determine the total timing current, I_T, available to charge the timing capacitor. Values for timing resistors can range from 1.5kΩ to 2MΩ; however, for optimum temperature and power supply stability, recommended values are 4kΩ to 200kΩ. To avoid parasitic pick up, timing resistor leads should be kept as short as possible. For noisy environments, unused or deactivated timing terminals should be bypassed to ground through 0.1μF capacitors. Otherwise, they may be left open.

Supply Voltage (pins 1 and 12)
The XR-2207 is designed to operate over a power supply range of $\pm$4V to $\pm$13V for split supplies, or 8V to 26V for single supplies. At high supply voltages, the frequency sweep range is reduced. Performance is optimum for $\pm$6V, or 12V single supply operation.

Binary Keying Inputs (pins 8 and 9)
The internal impedance at these pins is approximately 5kΩ. Keying levels are <1.4V for "zero" and >3V for "one" logic levels referenced to the DC voltage at pin 10.

Bias for Single Supply (pin 11)
For single supply operations, pin 11 should be externally biased to a potential between $+V_S/3V$ and $+V_S/2V$ (see Figure 1). The bias current at pin 11 is nominally 5% of the total oscillation timing current I_T.

Ground (pin 10)
For split supply operation, this pin serves as circuit ground. For single supply operation, pin 10 should be AC grounded through a 1μF bypass capacitor. During split supply operation, a ground current of 2 I_T flows out of this terminal, where I_T is the total timing current.

Squarewave Output (pin 13)
The squarewave output at pin 13 is an "open-collector" stage capable of sinking up to 20mA of load current. R_L serves as a pull-up load resistor for this output. Recommended values for R_L range from 1kΩ to 10kΩ.

Triangle Output (pin 14)
The output at pin 14 is a triangle wave with a peak swing of approximately one-half of the total supply voltage. Pin 14 has a very low output impedance of 10Ω and is internally protected against short circuits.

Note: Triangle waveform linearity is sensitive to parasitic coupling between the square and the triangle-wave outputs (pins 13 and 14). In board layout or circuit wiring care should be taken to minimize stray wiring capacitance between these pins.

Operating Instructions

Precautions
The following precautions should be observed when operating the XR-2207 family of integrated circuits:

1. Pulling excessive current from the timing terminals will adversely effect the temperature stability of the circuit. To minimize this disturbance, it is recommended that the total current drawn from pins 4, 5, 6, and 7 be limited to <6mA. In addition, permanent damage to the device may occur if the total timing current exceeds 10mA.
2. Terminals 2, 3, 4, 5, 6, and 7 have very low internal impedance and should, therefore, be protected from accidental shorting to ground or the supply voltages.
3. The keying logic pulse amplitude should not exceed the supply voltage.

Split Supply Operation
Figure 1 is the recommended circuit connection for split supply operation. The frequency of operation is determined by the timing capacitor, C, and the activated timing resistors (R1 through R4). The timing resistors are activated by the logic signals at the binary keying inputs (pins 8 and 9), as shown in Table 1. If a single timing resistor is activated, the frequency is 1/RC.

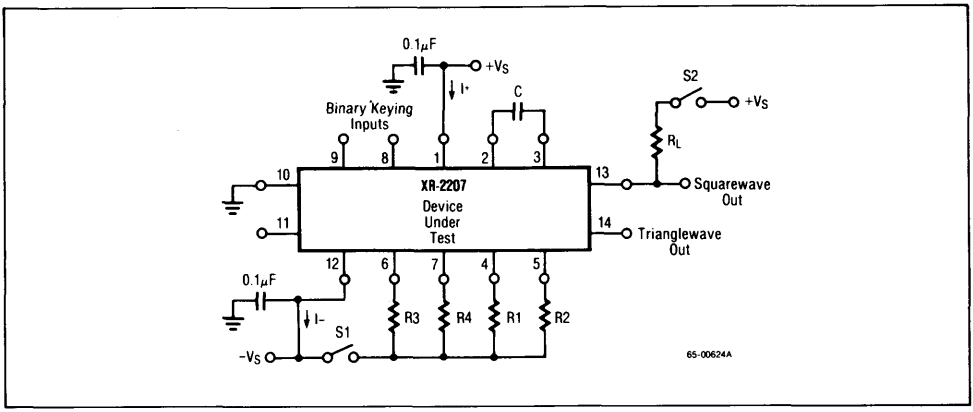


Figure 1. Test Circuit for Split Supply Operation

Table 1. Logic Table for Binary Keying Controls

Logic Level 8	Logic Level 9	Selected Timing Pins	Frequency	Definitions
0	0	6	f_1	$f_1 = 1/R3C$, $\Delta f_1 = 1/R4C$
0	1	6 and 7	$f_1 + \Delta f_1$	$f_2 = 1/R2C$, $\Delta f_2 = 1/R1C$
1	0	5	f_2	Logic Levels: 0 = Ground
1	1	4 and 5	$f_2 + \Delta f_2$	Logic Levels: 1 = >3V

Note: For single-supply operation, logic levels are referenced to voltage at pin 10.

Otherwise, the frequency is either 1/(R1||R2)C or 1/(R1||R4)C.

The squarewave output is obtained at pin 13 and has a peak-to-peak voltage swing equal to the supply voltages. This output is an "open-collector" type and requires an external pull-up load resistor (nominally 5kΩ) to the positive supply. The triangle waveform obtained at pin 14 is centered about ground and has a peak amplitude of $+V_S/2$.

The circuit operates with supply voltages ranging from ±4V to ±13V. Minimum drift occurs with ±6V supplies.

Single Supply Operation

The circuit should be interconnected as shown in Figure 2 for single supply operation. Pin 12 should be grounded, and pin 11 biased from $+V_S$ through a resistive divider to a value of bias voltage between $+V_S/3$ and $+V_S/2$. Pin 10 is bypassed to ground through a 0.1μF capacitor.

For single supply operation, the DC voltage at pin 10 and the timing terminals (pins 4 through 7) are equal and approximately 0.6V above V_B, the bias voltage at pin 11. The logic levels at the binary keying terminals are referenced to the voltage at pin 10.

On-Off Keying

The XR-2207 can be keyed on and off by simply activating an open circuited timing pin. Under certain conditions, the circuit may exhibit very low frequency (<1Hz) residual oscillation in the "off" state due to internal bias current. If this effect is undesirable, it can be eliminated by connecting a 10MΩ resistor from 3 to $+V_S$.

Frequency Control (Sweep and FM)

The frequency of operation is controlled by varying the total timing current, I_T, drawn from the activated timing pins 4, 5, 6, or 7. The timing current can be modulated by applying a control voltage, V_C, to the activated timing pin through a series resistor R_C as shown in Figure 3.

For split supply operation, a *negative* control voltage, V_C, applied to the circuit of Figure 3 causes the total timing current, I_T, and the frequency, to increase.

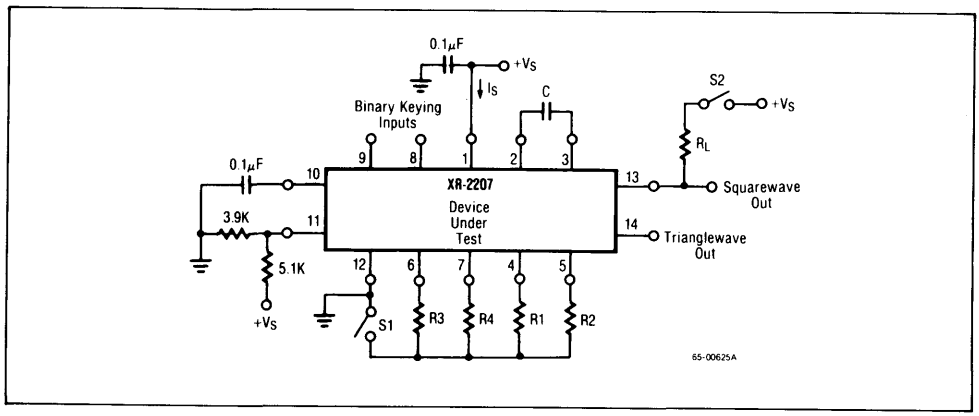


Figure 2. Test Circuit for Single Supply Operation

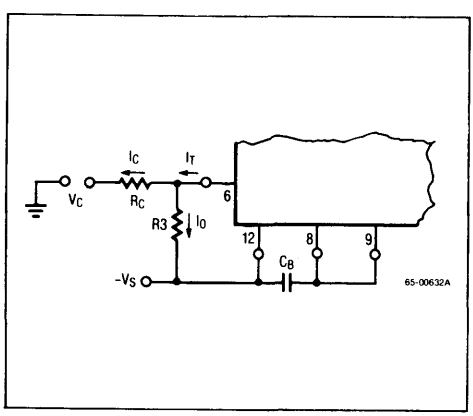


Figure 3. Frequency Sweep Operation

As an example, in the circuit of Figure 3, the binary keying inputs are grounded. Therefore, only timing pin 6 is activated.

The frequency of operation is determined by:

$$f = \frac{1}{R3C_B}\left[1 - \frac{V_C R3}{(R_C)(-V_S)}\right] Hz$$

Pulse and Sawtooth Operation

The duty cycle of the output waveforms can be controlled by frequency shift keying at the end of every half cycle of oscillator output. This is accomplished by connecting one or both of the binary keying inputs (pins 8 or 9) to the square-wave output at pin 13. The output waveforms can then be converted to positive or negative pulses and sawtooth waveforms.

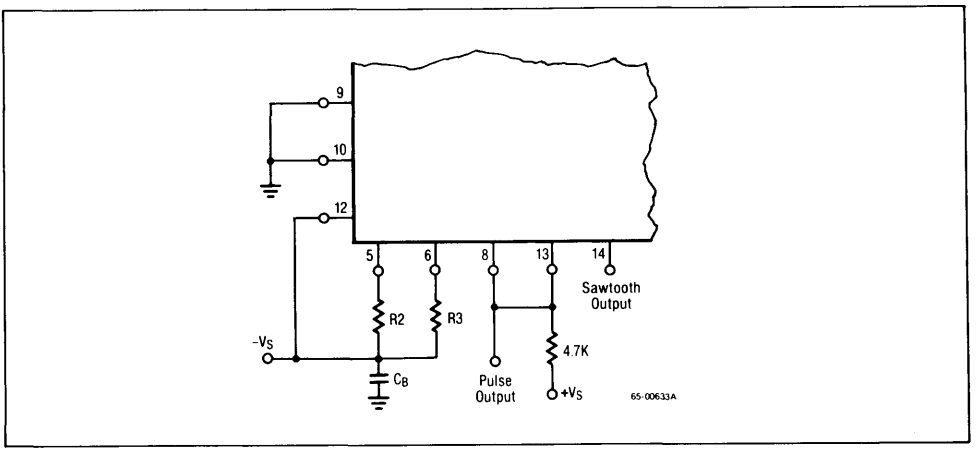


Figure 4. Pulse and Sawtooth Generation

Figure 4 is the recommended circuit connection for duty cycle control. Pin 8 is shorted to pin 13 so that the circuit switches between the "0,0" and the "1,0" logic states given in Table 1. Timing pin 5 is activated when the output is "high", and pin 6 is activated when the squarewave output goes to a "low" state.

The duty cycle of the output waveforms is given as:

$$\text{Duty Cycle} = \frac{R2}{R2 + R3}$$

and can be varied from 0.1% to 99.9% by proper choice of timing resistors. The frequency of oscillation, f, is given as:

$$f = \frac{2}{C}\left[\frac{1}{R2 + R3}\right]$$

The frequency can be modulated or swept without changing the duty cycle by connecting R2 and R3 to a common control voltage V_C instead of to $-V_S$. The sawtooth and the pulse output waveforms are shown in the Typical Performance Characteristics Graphs.

Raytheon

FSK Demodulator/ Tone Decoder

XR-2211

Features

- Wide frequency range — 0.01Hz to 300kHz
- Wide supply voltage range — 4.5V to 20V
- DTL/TTL/ECL logic compatibility
- FSK demodulation with carrier-detector
- Wide dynamic range — 2mV to $3V_{RMS}$
- Adjustable tracking range — ±1% to ±80%
- Excellent temperature stability — 20ppm/°C typical

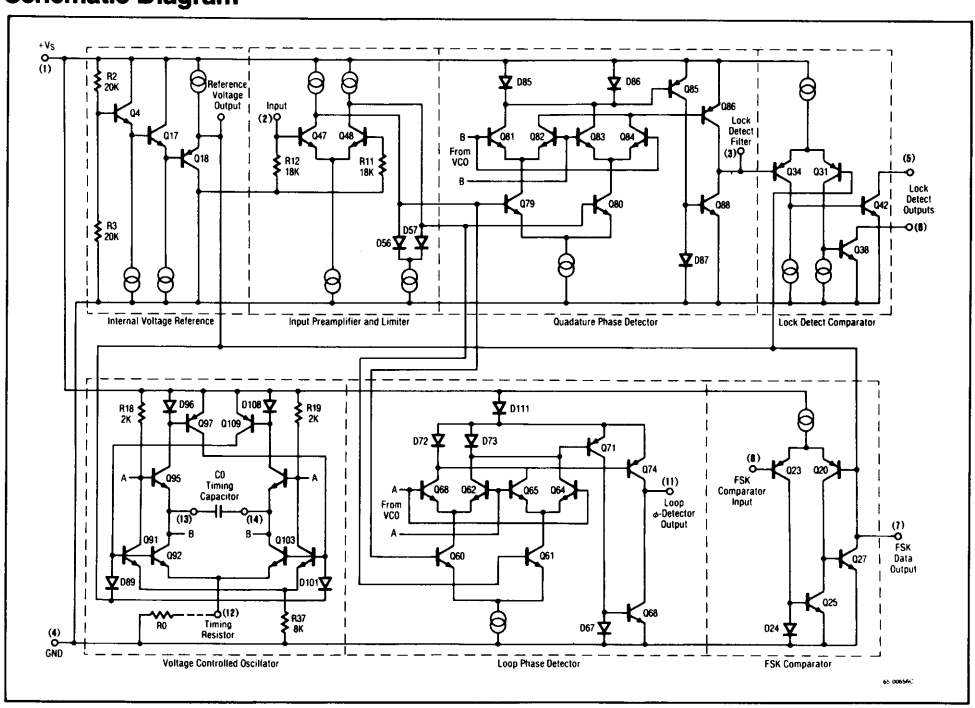
Applications

- FSK demodulation
- Data synchronization
- Tone decoding
- FM detection
- Carrier detection

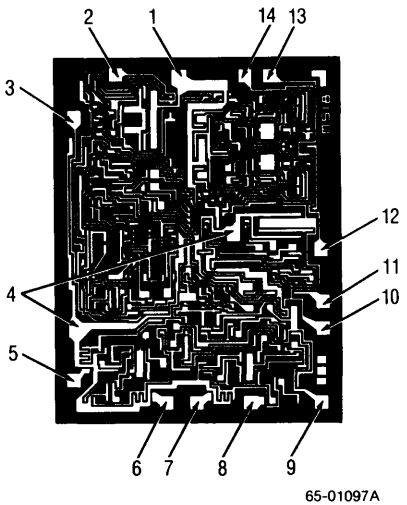
Description

The XR-2211 is a monolithic phase-locked loop (PLL) system especially designed for data communications. It is particularly well suited for FSK modem applications, and operates over a wide frequency range of 0.01Hz to 300kHz. It can accommodate analog signals between 2mV and 3V, and can interface with conventional DTL, TTL and ECL logic families. The circuit consists of a basic PLL for tracking an input signal frequency within the passband, a quadrature phase detector which provides carrier detection, and an FSK voltage comparator which provides FSK demodulation. External components are used to independently set carrier frequency, bandwidth, and output delay.

Schematic Diagram



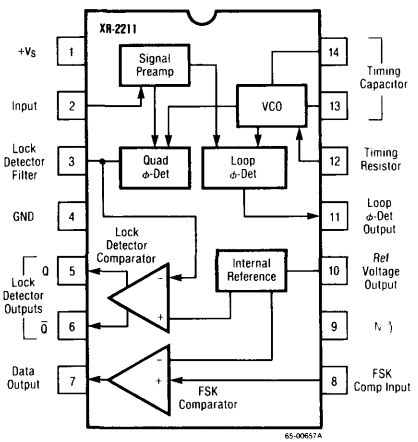
Mask Pattern



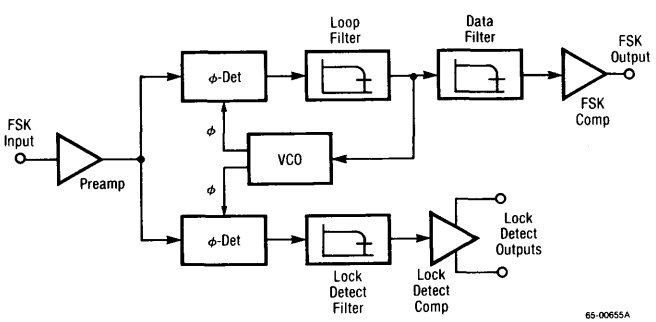
Die Size: 103 x 80 mils
Min. Pad Dimension: 4 x 4 mils

Connection Information

14-Lead
Dual In-Line Package
(Top View)



Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage ..... +20V
Input Signal Level ..... $3V_{RMS}$
Storage Temperature
Range ..... -65°C to +150°C

Operating Temperature Range
XR-2211CN/CP ..... 0°C to +75°C
XR-2211N/P ..... -40°C to +85°C
XR-2211M ..... -55°C to +125°C
Lead Soldering Temperature
(60 Sec) ..... +300°C

Thermal Characteristics

	14-Lead Plastic DIP	14-Lead Ceramic DIP
Max. Junction Temp.	125°C	175°C
Max. P_D T_A < 50°C	468mW	1042mW
Therm. Res. θ_{JC}	—	50°C/W
Therm. Res. θ_{JA}	160°C/W	120°C/W
For T_A > 50°C Derate at	6.25mW per °C	8.33mW per °C

Ordering Information

Part Number	Package	Operating Temperature Range
XR-2211CN XR-2211CP	Ceramic Plastic	0°C to +75°C 0°C to +75°C
XR-2211N XR-2211P	Ceramic Plastic	-40°C to +85°C -40°C to +85°C
XR-2211M XR-2211M/883B*	Ceramic Ceramic	-55°C to +125°C -55°C to +125°C

*MIL-STD-883, Level B Processing

Electrical Characteristics (Test Conditions $+V_S$ = +12V, T_A = +25°C, R0 = 30kΩ, C0 = 0.033μF. See Figure 1 for component designations.)

Parameters	Test Conditions	XR-2211/M			XR-2211C			Units
		Min	Typ	Max	Min	Typ	Max	
General								
Supply Voltage		4.5		20	4.5		20	V
Supply Current	R0 ≥ 10kΩ		4.0	9.0		5.0	11	mA
Oscillator								
Frequency Accuracy	Deviation from $f_0 = 1/R0C0$		±1.0	±3.0		±1.0		%
Frequency Stability Temperature Coefficient	R1 = ∞		±20	±50		±20		ppm/°C
Power Supply Rejection	$+V_S$ = 12 ±1V		0.05	0.5		0.05		%/V
	$+V_S$ = 5 ±0.5V		0.2			0.2		%/V
Upper Frequency Limit	R0 = 8.2kΩ, C0 = 400pF	100	300			300		kHz
Lowest Practical Operating Frequency	R0 = 2MΩ C0 = 50μF			0.01		0.01		Hz
Timing Resistor, R0 Operating Range		5.0		2000	5.0		2000	kΩ
Recommended Range		15		100	15		100	kΩ

Electrical Characteristics (Continued)

(V_S = +12V, T_A = +25°C, R0 = 30kΩ, C0 = 0.033μF. See Figure 1 for component designations.)

Parameters	Test Conditions	XR-2211/M			XR-2211C			Units
		Min	Typ	Max	Min	Typ	Max	
Loop Phase Detector								
Peak Output Current	Meas. at Pin 11	±150	±200	±300	±100	±200	±300	μA
Output Offset Current			±1.0			±2.0		μA
Output Impedance			1.0			1.0		MΩ
Maximum Swing	Ref. to Pin 10	±4.0	±5.0		±4.0	±5.0		V
Quadrature Phase Detector								
Peak Output Current	Meas. at Pin 3	100	150			150		μA
Output Impedance			1.0			1.0		MΩ
Maximum Swing			11			11		V_{p-p}
Input Preamp								
Input Impedance	Meas. at Pin 2		20			20		kΩ
Input Signal Voltage Required to Cause Limiting			2.0	10		2.0		mV_{RMS}
Voltage Comparator								
Input Impedance	Meas. at Pins 3 & 8		2.0			2.0		MΩ
Input Bias Current			100			100		nA
Voltage Gain	R_L = 5.1kΩ	55	70		55	70		dB
Output Voltage Low	I_C = 3mA		300			300		mV
Output Leakage Current	V_O = 12V		0.01			0.01		μA
Internal Reference								
Voltage Level	Meas. at Pin 10	4.9	5.3	5.7	4.75	5.3	5.85	V
Output Impedance			100			100		Ω

Description of Circuit Controls

Signal Input (Pin 2)
The input signal is AC coupled to this terminal. The internal impedance at pin 2 is 20kΩ. Recommended input signal level is in the range of $10mV_{RMS}$ to $3V_{RMS}$.

Quadrature Phase Detector Output (Pin 3)
This is the high-impedance output of the quadrature phase detector, and is internally connected to the input of lock-detect voltage comparator. In tone detection applications, pin 3 is connected to ground through a parallel combination of R_D and C_D (see Figure 1) to eliminate chatter at the lock-detect outputs. If this tone-detect section is not used, pin 3 can be left open circuited.

Lock-Detect Output, Q (Pin 5)
The output at pin 5 is at a "high" state when the PLL is out of lock and goes to a "low" or conducting state when the PLL is locked. It is an open collector type output and requires a pull-up resistor, R_L, to $+V_S$ for proper operation. In the "low" state it can sink up to 5mA of load current.

Lock-Detect Complement, Q (Pin 6)
The output at pin 6 is the logic complement of the lock-detect output at pin 5. This output is also an open collector type stage which can sink 5mA of load current in the low or "on" state.

FSK Data Output (Pin 7)
This output is an open collector logic stage which requires a pull-up resistor, R_L, to $+V_S$ for proper operation. It can sink 5mA of load current. When decoding FSK signals the FSK data output will switch to a "high" or off state for low input frequency, and will switch to a "low" or on state for high input frequency. If no input signal is present, the logic state at pin 7 is indeterminate.

FSK Comparator Input (Pin 8)
This is the high-impedance input to the FSK voltage comparator. Normally, an FSK post-detection or data filter is connected between this terminal and the PLL phase-detector output (pin 11). This data filter is formed by R_F and C_F of Figure 1. The threshold voltage of the comparator is set by the internal reference voltage, V_R, available at pin 10.

Reference Voltage, V_R (Pin 10)
This pin is internally biased at the reference voltage level, V_R; V_R = V+/2 - 650mV. The DC voltage level at this pin forms an internal reference

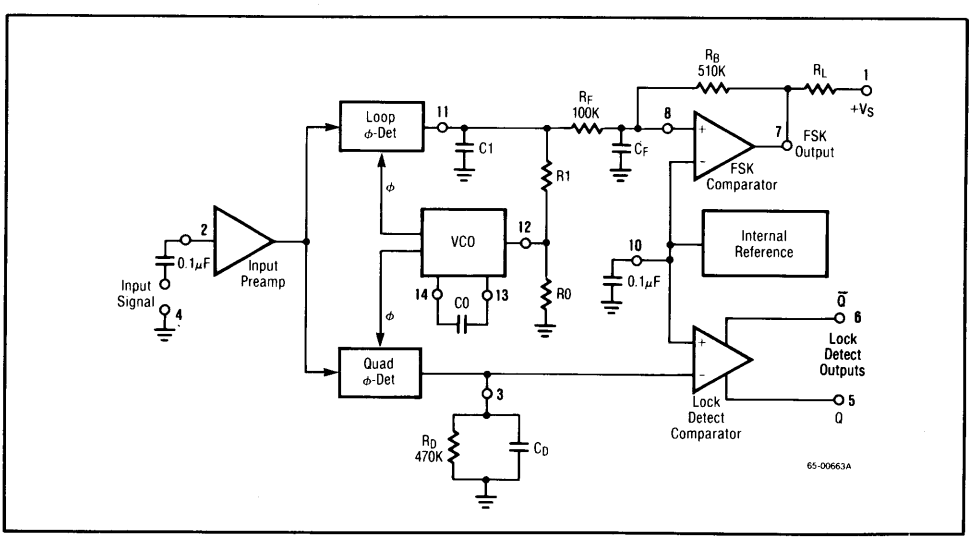


Figure 1. Generalized Circuit Connection for FSK and Tone Detection

for the voltage levels at pin 3, 8, 11, and 12. Pin 10 must be bypassed to ground with a 0.1μF capacitor.

Loop Phase Detector Output (Pin 11)
This terminal provides a high impedance output for the loop phase-detector. The PLL loop filter is formed by R1 and C1 connected to pin 11 (see Figure 1). With no input signal, or with no phase error within the PLL, the DC level at pin 11 is very nearly equal to V_R. The peak voltage swing available at the phase detector output is equal to $\pm V_R$.

VCO Control Input (Pin 12)
VCO free-running frequency is determined by external timing resistor, R0, connected from this terminal to ground. The VCO free-running frequency, f_0, is given by:

$$f_0(Hz) = \frac{1}{R0C0}$$

where C0 is the timing capacitor across pins 13 and 14. For optimum temperature stability R0 must be in the range of 10kΩ to 100kΩ (see Typical Electrical Characteristics).

This terminal is a low impedance point, and is internally biased at a DC level equal to V_R. The maximum timing current drawn from pin 12 must be limited to ≤3mA for proper operation of the circuit.

VCO Timing Capacitor (Pins 13 and 14)
VCO frequency is inversely proportional to the external timing capacitor, C0, connected across these terminals. C0 must be non-polarized, and in the range of 200pF to 10μF.

VCO Frequency Adjustment
VCO can be fine tuned by connecting a potentiometer, R_X, in series with R0 at pin 12 (see Figure 2).

VCO Free-Running Frequency, f_0
The XR-2211 does not have a separate VCO output terminal. Instead, the VCO outputs are internally connected to the phase-detector sections of the circuit. However, for setup or adjustment purposes, the VCO free-running frequency can be measured at pin 3 (with C_D disconnected) with no input and with pin 2 shorted to pin 10.

Design Equations

See Figure 1 for Definitions of Components.

1. VCO Center Frequency, f_0:

$$f_0(Hz) = \frac{1}{R0C0}$$

2. Internal Reference Voltage, V_R (measured at pin 10):

$$V_R = \left(\frac{+V_S}{2}\right) - 650mV$$

3. Loop Lowpass Filter Time Constant, τ:

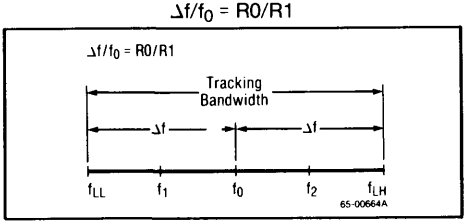
$$\tau = R1C1$$

4. Loop Damping, ζ:

$$\zeta = \left(\sqrt{\frac{C0}{C1}}\right)\left(\frac{1}{4}\right)$$

5. Loop Tracking Bandwidth, $\pm\Delta f/f_0$:

$$\Delta f/f_0 = R0/R1$$



6. FSK Data Filter Time Constant, τ_F:

$$\tau_F = R_F C_F$$

7. Loop Phase Detector Conversion Gain, K_ϕ: (K_ϕ is the differential DC voltage across pins 10 and 11, per unit of phase error at phase-detector input):

$$K\phi \text{ (in volts per radian)} = \frac{(-2)(V_R)}{\pi}$$

8. VCO Conversion Gain, K0, is the amount of change in VCO frequency per unit of DC voltage change at pin 11:

$$K0 \text{ (in Hertz per volt)} = \frac{-1}{C0R1V_R}$$

9. Total Loop Gain, K_T:

$$K_T \text{ (in radians per second per volt)} = 2\pi K\phi K0 = 4/C0R1$$

10. Peak Phase-Detector Current, I_A:

$$I_A \text{ (mA)} = \frac{V_R}{25}$$

Applications

FSK Decoding

Figure 2 shows the basic circuit connection for FSK decoding. With reference to Figures 1 and 2, the functions of external components are defined as follows: R0 and C0 set the PLL center frequency, R1 sets the system bandwidth, and C1 sets the loop filter time constant and the loop damping factor. C_F and R_F form a one pole post-detection filter for the FSK data output. The resistor R_B (= 510kΩ) from pin 7 to pin 8 introduces positive feedback across FSK comparator to facilitate rapid transition between output logic states.

Recommended component values for some of the most commonly used FSK bauds are given in Table 1.

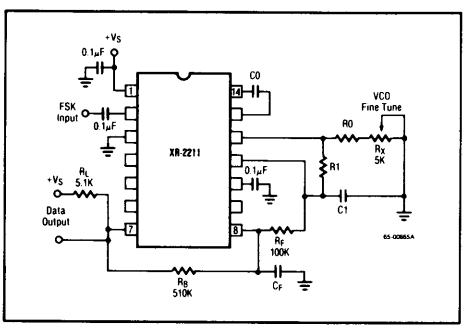


Figure 2. Circuit Connection for FSK Decoding

Table 1. Recommended Component Values for Commonly Used FSK Bands
(See Circuit of Figure 2)

FSK Band	Component Values
300 Baud	C0 = 0.039μF C_F = 0.005μF
f_1 = 1070Hz	C1 = 0.01μF R0 = 18kΩ
f_2 = 1270Hz	R1 = 100kΩ
300 Baud	C0 = 0.022μF C_F = 0.005μF
f_1 = 2025Hz	C1 = 0.0047μF R1 = 18kΩ
f_2 = 2225Hz	R1 = 200kΩ
1200 Baud	C0 = 0.027μF C_F = 0.0022μF
f_1 = 1200Hz	C1 = 0.01μF R0 = 18kΩ
f_2 = 2200Hz	R1 = 30kΩ

Design Instructions

The circuit of Figure 2 can be tailored for any FSK decoding application by the choice of five key circuit components; R0, R1, C0, C1 and C_F. For a given set of FSK mark and space frequencies, f_1 and f_2, these parameters can be calculated as follows:

1. Calculate PLL center frequency, f_0

$$f_0 = \frac{f_1 + f_2}{2}$$

2. Choose a value of timing resistor R0 to be in the range of 10kΩ to 100kΩ. This choice is arbitrary. The recommended value is R0 ≅ 20kΩ. The final value of R0 is normally fine-tuned with the series potentiometer, R_X.

3. Calculate value of C0 from Design Equation No. 1 or from Typical Performance Characteristics:

$$C0 = 1/R0f_0$$

4. Calculate R1 to give a Δf equal to the mark-space deviation:

$$R1 = R0\,[f_0/(f_1 - f_2)]$$

5. Calculate C1 to set loop damping. (See Design Equation No. 4.)
   Normally, $\zeta \approx 1/2$ is recommended
   Then: C1 = C0/4 for $\zeta = 1/2$

6. Calculate Data Filter Capacitance, C_F:
   For R_F = 100kΩ, R_B = 510kΩ, the recommended value of C_F is:

$$C_F\ (\text{in } \mu F) = \frac{3}{\text{Baud Rate}}$$

Note: All calculated component values except R0 can be rounded off to the nearest standard value, and R0 can be varied to fine-tune center frequency through a series potentiometer, R_X (see Figure 2).

Design Example

75 Baud FSK demodulator with mark/space frequencies of 1110/1170Hz:

Step 1: Calculate f_0:
f_0 = (1110 + 1170) (1/2) = 1140Hz

Step 2: Choose R0 = 20kΩ (18kΩ fixed resistor in series with 5kΩ potentiometer)

Step 3: Calculate C0 from V_{CO} Frequency vs. Timing Capacitor: C0 = 0.044μF

Step 4: Calculate R1: R1 = R0 (2240/60) = 380kΩ

Step 5: Calculate C1: C1 = C0/4 = 0.011μF

Note: All values except R0 can be rounded off to nearest standard value.

FSK Decoding With Carrier Detect

The lock-detect section of the XR-2211 can be used as a carrier detect option for FSK decoding. The recommended circuit connection for this application is shown in Figure 3. The open-collector lock-detect output, pin 6, is shorted to the data output (pin 7). Thus, the data output will be disabled at "low" state, until there is a carrier within the detection band of the PLL, and the pin 6 output goes "high" to enable the data output.

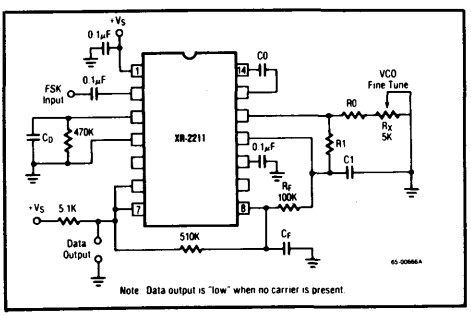


Figure 3. External Connectors for FSK Demodulation With Carrier Detect Capability

The minimum value of the lock-detect filter capacitance C_D is inversely proportional to the capture range, $\pm\Delta f_c$. This is the range of incoming frequencies over which the loop can acquire lock and is always less than the tracking range. It is further limited by C1. For most applications, $\Delta f_c < \Delta f/2$. For R_D = 470kΩ, the approximate minimum value of C_D can be determined by:

$$C_D(\mu F) \geq 16/\text{capture range in Hz}$$

With values of C_D that are too small, chatter can be observed on the lock-detect output as an incoming signal frequency approaches the capture bandwidth. Excessively large values of C_D will slow the response time of the lock-detect output.

Tone Detection

Figure 4 shows the generalized circuit connection for tone detection. The logic outputs, Q and $\overline{Q}$ at pins 5 and 6 are normally at "high" and "low" logic states, respectively. When a tone is present within the detection band of the PLL, the logic state at these outputs becomes reversed for the duration of the input tone. Each logic output can sink 5mA of load current.

Both logic outputs at pins 5 and 6 are open-collector type stages, and require external pull-up resistors R_{L1} and R_{L2} as shown in Figure 4.

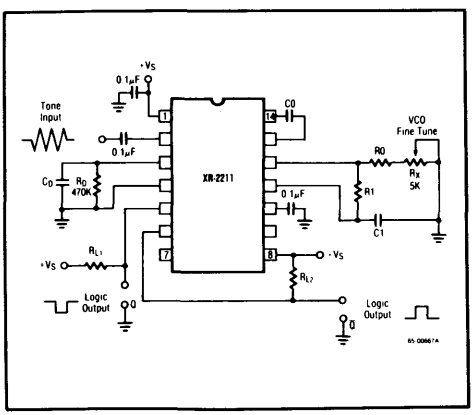


Figure 4. Circuit Connection for Tone Detection

With reference to Figures 1 and 4, the function of the external circuit components can be explained as follows: R0 and C0 set VCO center frequency, R1 sets the detection bandwidth, C1 sets the lowpass-loop filter time constant and the loop damping factor, and R_{L1} and R_{L2} are the respective pull-up resistors for the Q and $\overline{Q}$ logic outputs.

Design Instructions

The circuit of Figure 4 can be optimized for any tone-detection application by the choice of five key circuit components: R0, R1, C0, C1, and C_D. For a given input tone frequency, f_S, these parameters are calculated as follows:

1. Choose R0 to be in the range of 15kΩ to 100kΩ. This choice is arbitrary.
2. Calculate C0 to set center frequency, f_0 equal to f_S: $C0 = 1/R0f_S$.
3. Calculate R1 to set bandwidth $\pm\Delta f$ (see Design Equation No. 5): $R1 = R0(f_0/\Delta f)$

Note: The total detection bandwidth covers the frequency range of $f_0 \pm \Delta f$.

4. Calculate value of C1 for a given loop damping factor:

$$C1 = C0/16\zeta^2$$

Normally $\zeta \approx 1/2$ is optimum for most tone-detector applications, giving C1 = 0.25 C0.

Increasing C1 improves the out-of-band signal rejection, but increases the PLL capture time.

5. Calculate value of filter capacitor C_D. To avoid chatter at the logic output, with R_D = 470kΩ, C_D must be:

$$C_D(\mu F) \geq (16/\text{capture range in Hz})$$

Increasing C_D slows the logic output response time.

Design Examples

Tone detector with a detection band of 1kHz ±20Hz:

Step 1: Choose R0 = 20kΩ (18kΩ in series with 5kΩ potentiometer).

Step 2: Choose C0 for f_0 = 1kHz: C0 = 0.05μF.

Step 3: Calculate R1: R1 = (R0) (1000/20) = 1MΩ.

Step 4: Calculate C1: for ζ = 1/2, C1 = 0.25μF, C0 = 0.013μF.

Step 5: Calculate C_D: C_D = 16/38 = 0.42μF.

Step 6: Fine tune the center frequency with the 5kΩ potentiometer, R_X.

Linear FM Detection

The XR-2211 can be used as a linear FM detector for a wide range of analog communications and telemetry applications. The recommended circuit connection for the application is shown in Figure 5. The demodulated output is taken from the loop phase detector output (pin 11), through a post detection filter made up of R_F and C_F, and an external buffer amplifier. This buffer amplifier is necessary because of the high impedance output at pin 11. Normally, a non-inverting unity gain op amp can be used as a buffer amplifier, as shown in Figure 5.

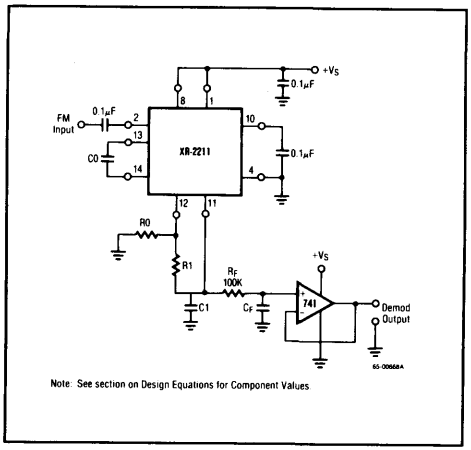


Figure 5. Linear FM Detector Using XR-2211 and an External Op Amp

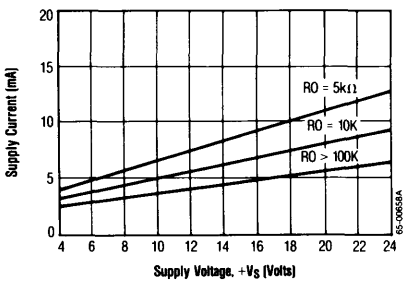
The FM detector gain, i.e., the output voltage change per unit of FM deviation, can be given as:

$$V_{OUT} = R1\ V_R/100\ R0 \text{ Volts/\% deviation}$$

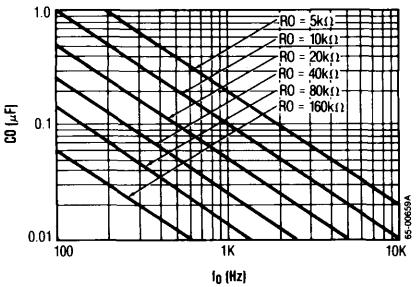
where V_R is the internal reference voltage. For the choice of external components R1, R0, C_D, C1 and C_F, see the section on Design Equations.

Typical Performance Characteristics

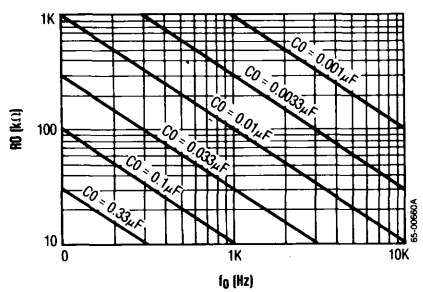
Typical Supply Current vs. $+V_S$ (Logic Outputs Open Circuited)



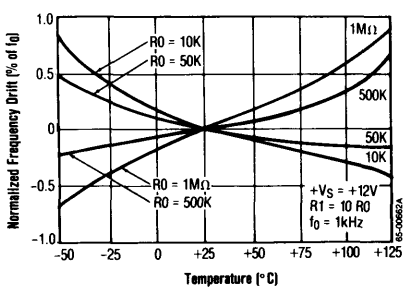
VCO Frequency vs. Timing Resistor



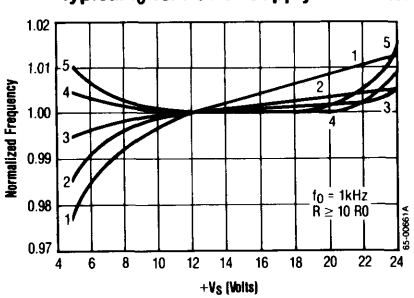
VCO Frequency vs. Timing Capacitor



Typical Center Frequency Drift vs. Temperature



Typical f_0 vs. Power Supply Characteristics



Curve	RO
1	5K
2	10K
3	30K
4	100K
5	300K

Section 13
Ordering Information & Packages

Package Descriptions

CJ 14-Pin Ceramic Flatpak
D 14, 16, 18, 20, 24 or 40-Pin Ceramic DIP
DB 14-Pin Plastic DIP
DC 14-Pin Ceramic DIP
DE 8-Pin Ceramic DIP
H 8 or 10-Pin Metal Can
J 14-Pin Ceramic DIP
M 8 or 14-Pin Micro DIP
N Plastic DIP
NB 8-Pin Plastic DIP
P Plastic DIP
PU 24-Pin Plastic DIP
R 24-Pin Ceramic DIP
T 8, or 10-Pin Metal Can
TK 9-Pin TO-66 Metal Can

LM Series

LM 148 J /883B

- Prefix
- Basic Part Type
- Package Type
- Optional Processing to MIL-STD-883, Level B

Raytheon Series

RC 4151 DE /883B

- Temperature Range
  - RC 0°C to +70°C
  - RM -55°C to +125°C
- Basic Part Type
- Package Type
- Optional Processing to MIL-STD-883, Level B

DAC Series

DAC- 6012 A D M /883B

- Prefix
  - Digital to Analog Converter
- Basic Part Type
  - Maximum 4-digits
- Electrical
  - See Data Sheet
- Package Type
  - D Ceramic
  - P Plastic
- Temperature
  - C 0°C to +70°C
  - M -55°C to +125°C
- Optional Processing to MIL-STD-883, Level B

HA Series

HA 1 4741 2

- Prefix
- Package Type
  - 1 14-Pin Ceramic DIP
  - 3 14-Pin Plastic DIP
- Basic Part Type
- Temperature Range
  - 2 -55°C to +125°C
  - 5 0°C to +70°C
  - 8 -55°C to +125°C (MIL-STD-883, Level B)

XR Series

XR 2207 CN

- Prefix
- Basic Part Type
- Package and Temperature Range
  - M Ceramic -55°C to +125°C
  - CN Ceramic 0°C to +75°C
  - CP Plastic 0°C to +75°C

Approved Assembly Plants & Brand Codes

"0" M.V.
Raytheon Semiconductor, 490 E. Middlefield Road, Mountain View, CA 94043

"T" TEPIC
ENSA Electronica Nayarit, S.A., Juan Escutia No. 122 Tepic Nayarit, Mexico

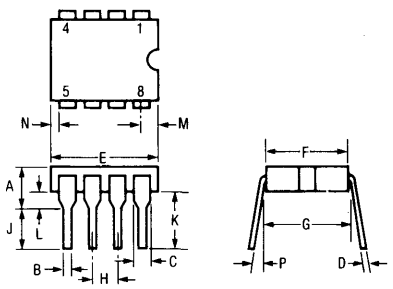
"C" Epic/M
Epic Semiconductor (Phil.) Inc.
2100 Pasong Tamo Extension, Makati, Metro Manile, Philippines

"L" N.J.R.C.
New Japan Radio, (Saga Electronics Co., Ltd.), 950 Tateno Mitagawa-Machi Kanzaki-Gun Saga Pref. Fakuoka, Japan

"P" SDPI
Semiconductor Devices (PHIL.) Inc.
GMTFM Compound, Tagoig, Rizal
P.O. Box 7438
Air Mail Exchange Office, MIA, Philippines

"F" Talent Electronics Corp., 3rd Floor No. 2, Lane 49, Chung HSIAO E. Road Section 4, Taipel, Taiwan, R.O.C.

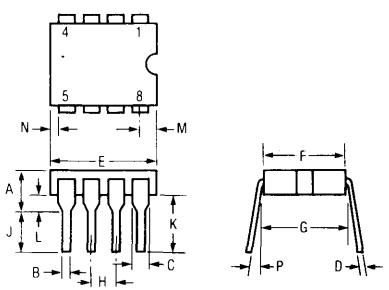
8-Lead
Plastic Dual-In Line



Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	.115	.125	2.92	3.17
B	.015	.021	0.38	0.53
C	.030	.070	0.76	1.78
D	.010	.015	0.25	0.38
E	.360	.400	9.14	10.16
F	.240	.260	6.09	6.60
G	.290	.310	7.37	7.87
H	.090	.110	2.29	2.79
J	.120	.135	3.05	3.43
K	.140	.165	3.56	4.18
L	.020	.030	0.51	0.75
M	.025	.050	0.64	1.27
N	.005		0.13	
P	0°	15°	0°	15°

65-01192B

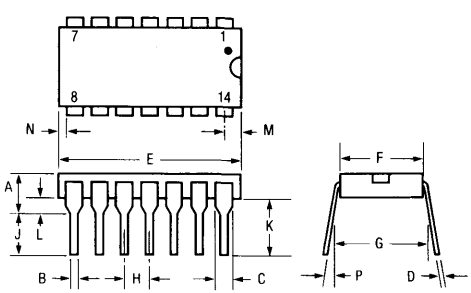
8-Lead
Ceramic
Dual-In-Line



Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A		.200		5.08
B	.014	.023	0.36	0.58
C	.030	.070	0.76	1.78
D	.008	.015	0.20	0.38
E		.390		9.91
F	.220	.310	5.59	7.87
G	.290	.320	7.37	8.13
H	.100 BSC		2.54 BSC	
J	.125	.200	3.18	5.08
K	.150		3.81	
L	.015	.060	0.38	1.52
M		.045		1.14
N	.005		0.13	
P	0°	15°	0°	15°

65-01203B

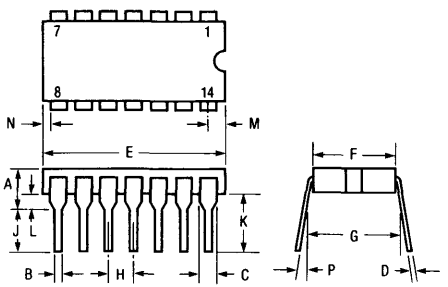
14-Lead
Plastic Dual In-Line



Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	.115	.125	2.92	3.18
B	.018	.022	0.46	0.56
C	.038	.053	0.015	0.021
D	.010	.015	0.25	0.38
E	.745	.755	18.92	19.18
F	.252	.290	6.22	6.40
G	.290	.310	7.37	7.87
H	.100BSC		2.54BSC	
J	.120	.135	3.05	3.43
K	.135		3.43	
L	.015	.035	0.38	0.89
M	.065	.085	1.65	2.16
N	.005		0.13	
P	0°	15°	0°	15°

65-01194B

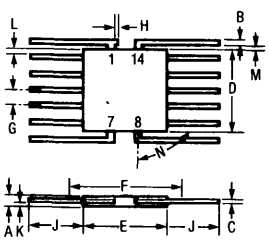
14-Lead
Ceramic Dual In-Line



Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A		.200		5.08
B	.014	.023	0.36	0.58
C	.030	.070	0.76	1.78
D	.008	.015	0.20	.38
E		.785		19.94
F	.220	.310	5.59	7.87
G	.290	.320	7.37	8.13
H	.100BSC		2.54BSC	
J	.125	.200	3.18	5.08
K	.150		3.81	
L	.015	.060	0.38	1.52
M		.098		2.49
N	.005		0.13	
P	0°	15°	0°	15°

65-01204B

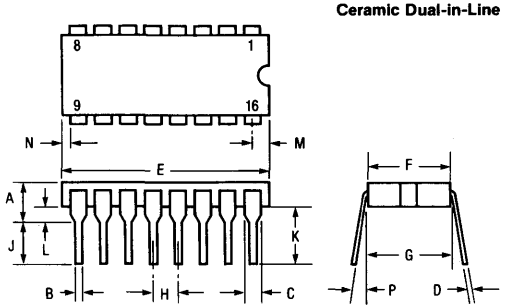
14-Lead
Ceramic Flat Package



Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	.030	.085	0.76	2.16
B	.010	.019	0.25	0.48
C	.003	.006	0.08	0.15
D		.280		7.11
E	.240	.260	6.10	6.60
F		.280		7.11
G	.050BSC		1.27BSC	
H	.008	.015	0.20	0.38
J	.250	.370	6.35	9.40
K	.010	.040	0.25	1.02
L	.005		0.13	
M	.004		0.10	
N	30°	90°	30°	90°

65-01207B

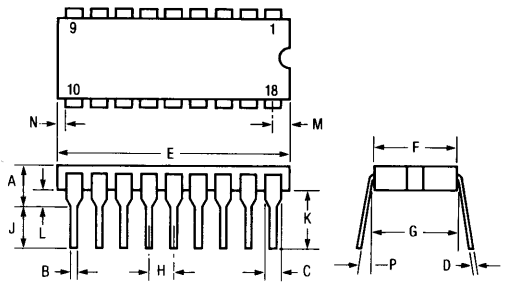
16-Lead
Ceramic Dual-in-Line



Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A		.200		5.08
B	.014	.023	.36	.58
C	.030	.070	.76	1.78
D	.008	.015	.20	.38
E		.840		21.34
F	.220	.310	5.59	7.87
G	.290	.320	7.37	8.13
H	.100BSC		2.54BSC	
J	.125	.200	3.18	5.08
K	.150		3.81	
L	.015	.060	.38	1.52
M		.080		2.03
N	.005		.13	
P	0°	15°	0°	15°

65-01208B

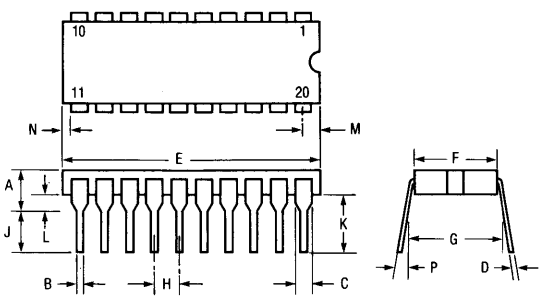
18-Lead
Ceramic Dual In-Line



Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A		.200		5.08
B	.014	.023	.36	.58
C	.030	.070	.76	1.78
D	.008	.015	.20	.38
E		.940	23.90	23.90
F		.310		7.87
G	.290	.320	7.37	8.13
H	.100BSC		2.54BSC	
J	.120	.200	3.05	5.08
K	.150		3.81	
L	.015	.060	.38	1.52
M		.080	.38	2.03
N	.005		.13	
P	0°	15°	0°	15°

65-01211B

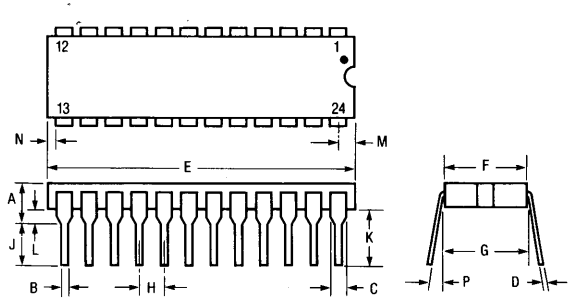
20-Lead
Ceramic Dual In-Line



Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A		.200		5.08
B	.014	.023	.36	.58
C	.030	.070	.76	1.78
D	.008	.015	.20	.38
E	.930	.975	23.60	24.80
F	.220	.310	5.59	7.87
G	.290	.320	7.37	8.13
H	.100BSC		2.54BSC	
J	.120	.200	3.05	5.08
K	.150		3.81	
L	.015	.060	.38	1.52
M		.098	.38	2.49
N	.005		.13	2.49
P	0°	15°	0°	15°

65-01214B

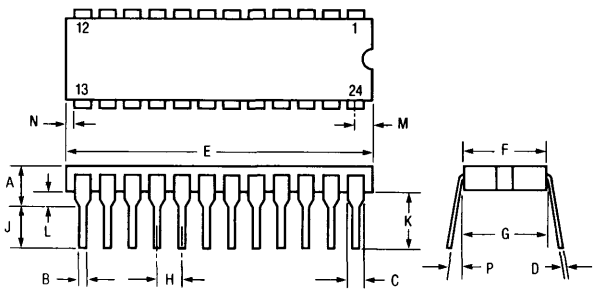
24-Lead
Plastic Dual In-Line



Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A		.225		5.72
B	.014	.023	0.36	0.58
C	.030	.070	0.76	1.78
D	.008	.015	0.20	0.38
E		1.290		32.77
F	.500	.610	12.70	15.49
G	.590	.620	14.99	15.75
H	.100BSC		2.54BSC	
J	.120	.200	3.05	5.08
K	.150		3.81	
L	.015	.075	0.38	1.91
M		.098		2.49
N	.005		0.13	
P	0°	15°	0°	15°

65-01200B

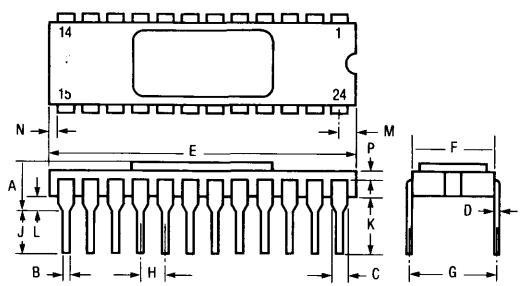
24-Lead Ceramic Dual In-Line



Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A		.225		5.72
B	.014	.023	.36	.58
C	.030	.070	.76	1.78
D	.008	.015	.20	.38
E		1.290		32.77
F	.500	.610	12.70	15.49
G	.590	.620	14.99	15.75
H	.100BSC		2.54BSC	
J	.120	.200	3.05	5.08
K	.150		3.81	
L	.015	.075	.38	1.91
M		.098		2.49
N	.005		.13	
P	0°	15°	0°	15°

65-01217B

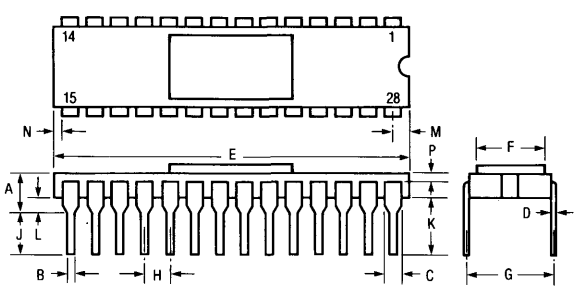
24-Lead Ceramic Side-Brazed Dual In-Line



Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A		0.200		5.08
B	0.015	0.023	0.38	0.58
C	0.045	0.060	1.14	1.52
D	0.008	0.012	0.20	0.31
E	1.150	1.220	29.20	31.01
F	0.580	0.610	7.11	7.87
G	0.580	0.620	7.37	8.13
H	0.100BSC		2.54BSC	
J	0.125		3.18	
K	0.150		3.05	5.08
L	0.015	0.060	0.38	1.52
M	0.030	0.065	0.76	1.65
N	0.005		0.13	
P	0.005		0.13	

65-01218B

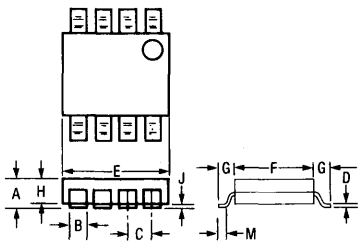
28-Lead Ceramic Side-Brazed Dual In-Line



Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A		.200		5.08
B	.015	.021	0.38	0.53
C	.045	.060	1.14	1.52
D	.008	.012	0.20	0.31
E	1.380	1.430	35.05	36.32
F	.590	.620	14.98	15.74
G	.580	.644	14.73	16.36
H	.100BSC		2.54BSC	
J	.125	.175	3.18	4.45
K	.155		3.94	
L	.030	.070	0.76	1.78
M	.030	.065	0.76	1.65
N	.005		0.13	
P	.005		0.13	

65-01223B

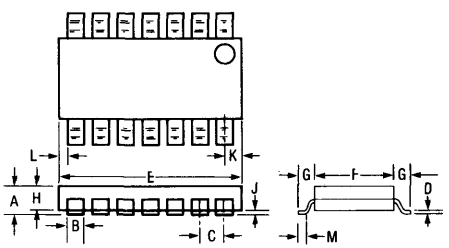
8-Lead Plastic Dual-in-Line Micro-Pak



Dimension	Inches			Millimeters		
	Min	Typ	Max	Min	Typ	Max
A		0.061	0.068		1.57	1.75
B	0.012	0.014	0.018	0.30	0.35	0.45
C		0.050			1.27	
D	0.004	0.006	0.010	0.10	0.15	0.25
E		0.197	0.203		5.00	5.15
F	0.161	0.165	0.169	4.10	4.20	4.30
G	0.031	0.037	0.043	0.80	0.95	1.10
H		0.059	0.061		1.50	1.56
J		0.004	0.008		0.07	0.20
M	0.010	0.021		0.25	0.55	

65-01193B

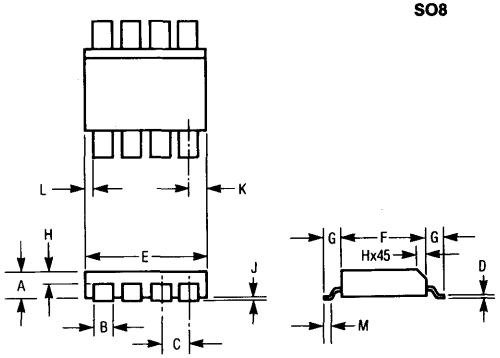
14-Lead Plastic Dual-in-Line Micro-Pak



Dimension	Inches		Millimeters	
	Typ.	Max.	Typ.	Max.
A	0.070		1.750	
B		0.018		0.450
C	0.050		1.250	
D		0.010		0.250
E		0.400		10.150
F		0.200		5.100
G	0.035		0.900	
H		0.069		1.750
J	0.006		0.150	
K	0.034		0.690	
L	0.025		0.450	
M	0.020		0.500	

65-01195B

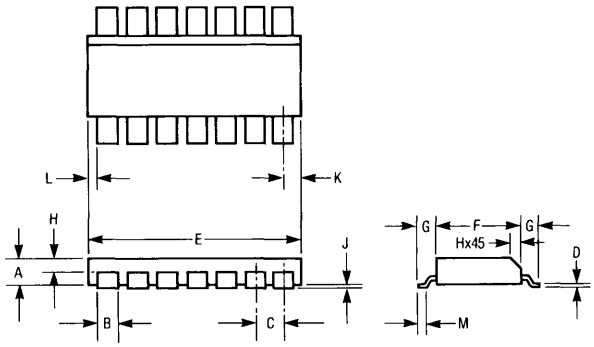
8-Lead Plastic Dual-in-Line SO8



Dimension	Inches			Millimeters		
	Min	Typ	Max	Min	Typ	Max
A	0.053		0.069	1.35	7	1.75
B	0.014		0.018	0.350		0.450
C		0.050 BSC			1.27 BSC	
D	0.007		0.009	0.190		0.220
E	0.188		0.197	4.80		5.00
F	0.150		0.158	3.80		4.00
G						
H						
J	0.004		0.008	0.100	0.200	
K						
L						
M	0.020		0.045	0.508		1.143

65-02098B

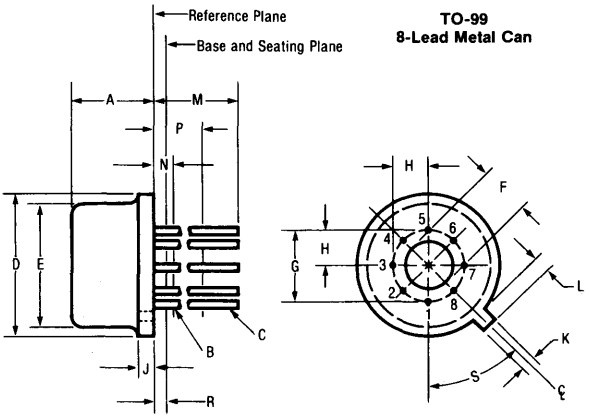
14-Lead
Plastic Dual-in-Line
SO14



Dimension	Inches			Millimeters		
	Min	Typ	Max	Min	Typ	Max
A	0.053		0.069	1.35		1.75
B	0.014		0.018	0.35		0.45
C		0.050 BSC			1.27 BSC	
D	0.007		0.009	0.19		0.22
E	0.336		0.344	8.55		8.75
F	0.150		0.158	3.80		4.00
G						
H						
J	0.004		0.008	0.100		0.200
K						
L						
M	0.021		0.045	0.508		1.143

65-02099B

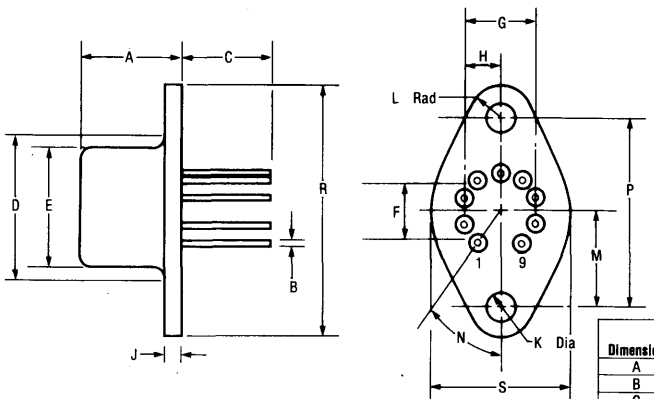
TO-99
8-Lead Metal Can



Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	.165	.185	4.19	4.70
B	.016	.019	.41	.48
C	.016	.021	.41	.53
D	.335	.370	8.51	9.40
E	.305	.335	7.75	8.51
F	.120	.160	3.05	4.06
G	.200 BSC		5.08 BSC	
H	.100 BSC		2.54 BSC	
J		.040		1.02
K	.027	.034	.69	.86
L	.027	.045	.69	1.14
M	.500	.750	12.70	19.05
N		.050		1.27
P	.250		6.35	
R	.010	.045	.25	1.14
S	45° BSC		45° BSC	

65-01189B

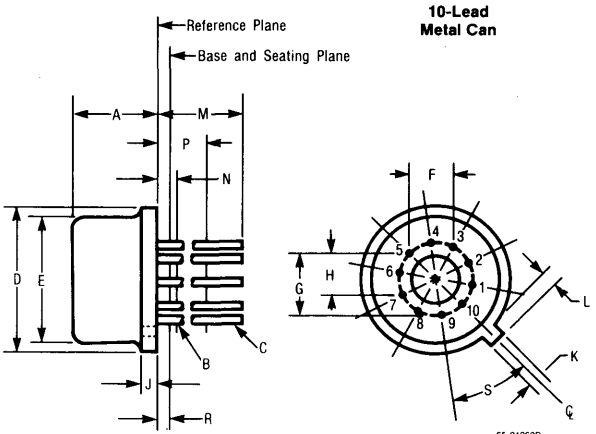
TO-66
9-Lead Metal Can



Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	.250	.340	6.35	8.63
B	.028	.034	.71	.863
C	.360		9.14	
D		.620		15.748
E	.300	.500	7.62	12.70
F	.120	.160	3.05	4.06
G	.230BSC		5.84BSC	
H	.115BSC		2.92BSC	
J	.050	.075	1.27	1.90
K	.142	.152	3.60	3.86
L		.145		3.68
M	.477	.483	12.11	12.26
N	36° Typ.		36° Typ.	
P	.958	.962	24.33	24.43
R		1.252		31.80
S		.700		17.80

65-01190B

TO-100
10-Lead
Metal Can



65-01262B

Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A	0.165	0.185	4.19	4.70
B	0.016	0.019	0.41	0.48
C	0.016	0.021	0.41	0.53
D	0.335	0.370	8.51	9.40
E	0.305	0.335	7.75	8.51
F	0.120	0.160	3.05	4.06
G	0.230 BSC		5.84 BSC	
H	0.115 BSC		2.92 BSC	
J		0.040		1.02
K	0.028	0.034	0.69	0.86
L	0.029	0.045	0.69	1.14
M	0.500	0.750	12.70	19.05
N		0.050		1.27
P	0.250		6.35	
R	0.010	0.045	0.25	1.14
S	36° BSC		36° BSC	

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